Correlation Method of Circuit-Performance and Technology Fluctuations for Improved Design Reliability

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Abstract— We propose a method of correlating circuit performance with technology fluctuations during the circuit-design phase. The method employs test circuits sensitive for technology fluctuations and a circuit simulation model which enables to interpret the correlation. We validate our proposal with a cascode-current-source test circuit and the drift-diffusion MOSFET model HiSIM. The chosen test circuit allows to separate intra-chip and inter-chip technology fluctuations and to correlate these fluctuations with circuit-performance fluctuations. One important result is that intra-chip fluctuations increase faster than inter-chip fluctuations with decreasing gate length. Quantitative modeling with HiSIM reveals random fluctuation of the effective gate length as the most likely origin for these findings.

I. Introduction

Design reliability of ICs is a requirement of increasing importance. For this purpose it is necessary to include MOSFET performance fluctuations caused by technological fluctuations into the design. Usually worst/best-case parameter sets are provided to support design reliability [1,2]. However, existing estimation methods of these parameter sets are of global statistical nature [3,4]. Especially, the correlation between circuit-performance fluctuations and technology fluctuations is still insufficient due to the conventional models for circuit simulation based on the drift approximation [5]. Furthermore, a separation between fluctuations within one IC-chip (intra-chip) and from chip to chip (inter chip) is seldom available [6]. For upgrading design reliability it is therefore essential to include the correlation between circuit-performance fluctuations and technology fluctuations in the design tools. This task requires to: (1) determine the correlation between circuit-performance and technology fluctuations, (2) separate intra- and inter-chip fluctuations, (3) model this correlation in the design phase. Here we propose a method based on:

- Test-circuits, which exploit the technologically most sensitive MOSFET characteristics near threshold, for (1) and (2).
- A drift-diffusion model, which can preserve this correlation in the design phase.

The reason for this choice is that the threshold characteristics are technologically the most sensitive, and both the drift and the diffusion components are responsible for the characteristics.

We demonstrate the validity of the method with a cascode current source and the drift-diffusion circuit-simulation model HiSIM (Hiroshima-university STARC IGFET Model) for a $0.6\mu m$ CMOS technology. An important specific result from our study is that intra-chip fluctuations increase faster than inter-chip fluctuations with decreasing gate length (L_{gate}). This is a severe concern for the design reliability of analog circuits.

II. Correlation between Circuit-Performance and Technology Fluctuations

Fig. 1 shows the investigated cascode-current-source circuit composed of 4 n-MOSFETs. The function of the cascode current source is to provide a constant current at its output terminal, which is proportional (the proportionality factor is a design task) to the current I_{in} at its input terminal and independent of the applied output voltage V_{out}. This test circuit was fabricated with a conventional $0.6\mu m$ MOSFET technology. Circuit characterization in the subthreshold region was performed by forcing I_{in}=10nA on input node N0 and measuring I_{out} (V_{out}) as well as V_{in}. Results for 9 different chips from

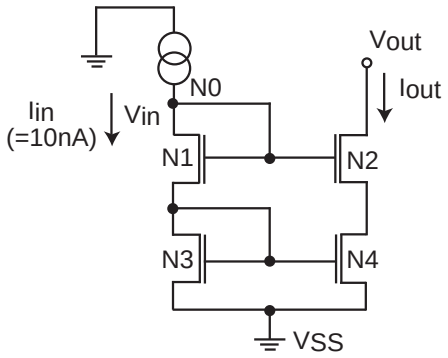

Fig. 1. Schematic of the cascode-current-source circuit used for our investigation. The output current $I_{out}(V_{out})$ is measured by forcing an input current I_{in} of 10nA on the node NO while $V_{ss} = 0V$. The input voltage V_{in} giving I_{in}=10nA is also monitored.

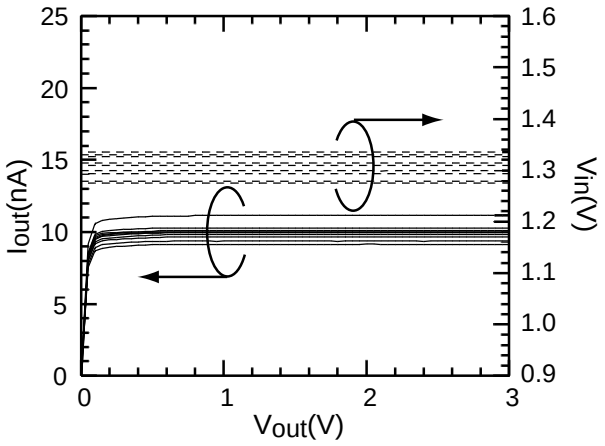

Fig. 2. Measured I_{out} characteristics of the cascode shown in Fig. 1 as a function of V_{out} with I_{in}=10nA for $L_{gate} = 2.1\mu m$. Solid lines are results of I_{out} from 9 different chips, and dashed lines are those of V_{in}.

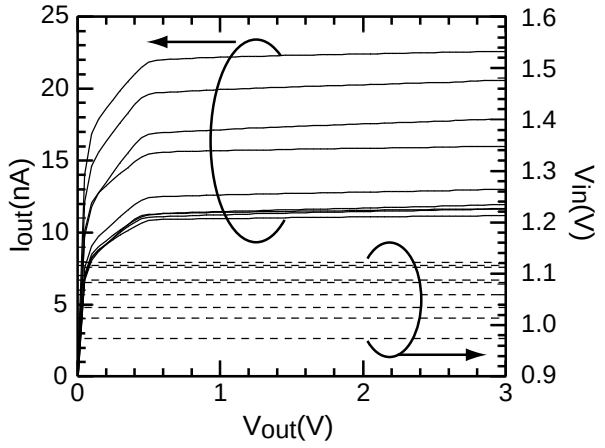

Fig. 3. The same characteristics as shown in Fig. 2 but for $L_{gate} = 0.6\mu m$.

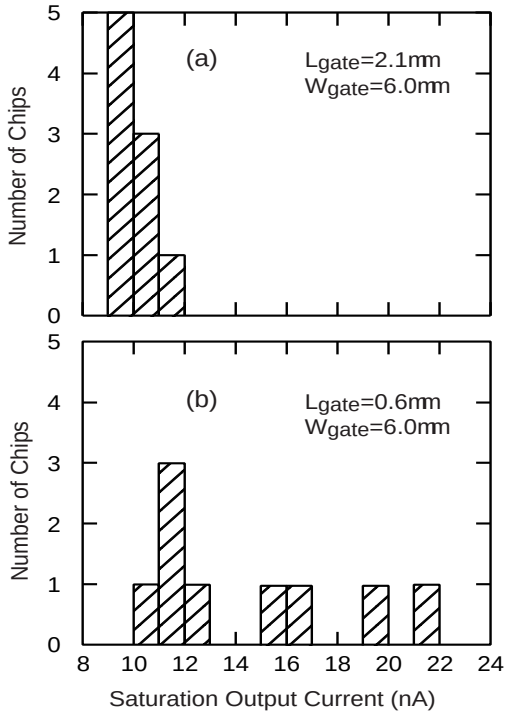

Fig. 4. Distribution of measured saturation output currents of (a) Fig.2 and (b) Fig. 3.

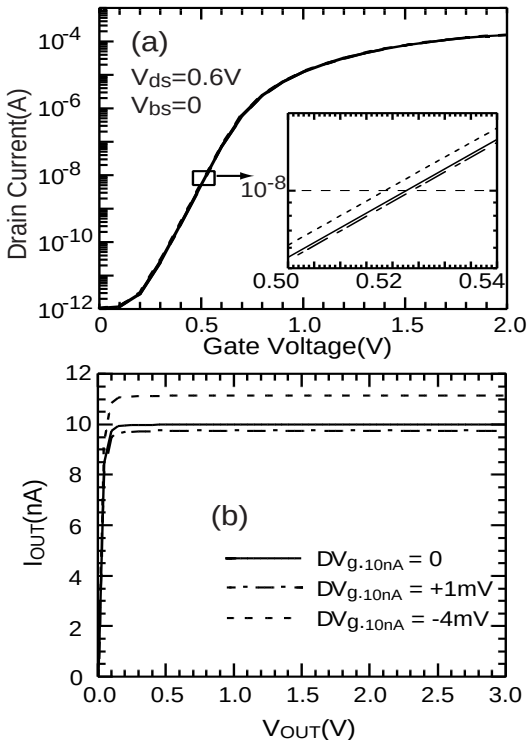

Fig. 5. Simulation results with $L_{gate} = 2.1\mu m$. (a) The original I-V characteristics (solid line) is modified by changing device parameter values to give different $V_{g.10nA}$ (dotted-dashed line and dotted line). (b) The output current I_{out} of the cascode with the $I - V$ characteristics of the original $V_{g.10nA}$ for both N3 and N4 transistors(solid line). The dotted-dashed line is the result with $+1mV$ shift(dotted-dashed line in Fig. 5a) for N4 and the dotted line is that with $-4mV$(dotted line in Fig. 5a).

the same lot are shown in Figs. 2 and 3 for L_{gate} of 2.1μm and 0.6μm, respectively. Statistics of measured saturation I_{out} are depicted in Figs. 4 for both channel lengths. The saturation I_{out} is expected to be 10nA, if the characteristics of the 4 n-MOSFETs of the cascode (N1-N4) are equivalent. However, fluctuation in I_{out} is clear, and it is much larger for L_{gate}=0.6μm than for L_{gate}=2.1μm. Though the fluctuation for L_{gate}=2.1μm occurs around I_{out}=10nA, that for the 0.6μm case is shifted to a higher value. The origin of the I_{out} fluctuation can be attributed to a mismatch of the threshold voltage (V_{th}) between transistors N3 and N4 as demonstrated in Fig. 5 for L_{gate}=2.1μm. Fig. 5a depicts 3 simulated I-V characteristics with different device parameters resulting in different $V_{g.10nA}$ (the gate voltage giving 10nA current) values at the drain voltage $V_{ds} = 0.6V$. Fig. 5b shows simulation results of I_{out} of the cascode by fixing the transistor characteristics of N3 to be the solid line of Fig. 5a and changing that of N4 according to the three cases depicted in Fig. 5a. It can be seen that the cascode circuit is suitable to verify the intra-chip transistor mismatch with mV accuracy. The estimated $V_{g.10nA}$ mismatch is about 8mV. The slight increase of I_{out} with increasing V_{out} in Fig. 3 for L_{gate}=0.6μm is due to the V_{th} dependence on V_{ds} caused by the short-channel effect.

III. Separation of Inter- and Intra-Chip Fluctuations

A special advantage of the cascode current source demonstrated here is that the inter- and the intra-chip fluctuations can be measured at the same time:

- The intra-chip fluctuations are given by the current fluctuations at the output(I_{out}), because they depend on the mismatch of transistors N3 and N4.
- The voltage response V_{in} to the forced input current of I_{in}=10nA gives the inter-chip fluctuations, because the voltage response depends on the absolute fluctuation in the characteristics of transistors N1 and N3.

Both measured fluctuations are depicted together in Figs. 2 and 3. It can be recognized that the inter- and intra-chip fluctuations are substantially larger for L_{gate}=0.6μm. Here we try to evaluate the magnitude of both types of fluctuations quantitatively. Figs. 6 and 7 show measured I-V characteristics of single transistors on the same 9 chips for L_{gate}=2.1μm and L_{gate}=0.6μm, respectively. These measured inter-chip $V_{g.10nA}$ fluctuations of single transistors together with the V_{in} fluctuations of the cascode current source are used to extract the magnitude of the intra-chip fluctuation at $V_{g.10nA}$. Fig. 8 shows measured $V_{in}/2$ vs. $V_{g.10nA}$ for each chip. The reason for $V_{in}/2$ is based on the approximation that N1 and N3 are identical, and are equivalently responsible for the inter-chip fluctuations. In this case, a linear correlation with the slope 1 is expected. The scattering of measured points in horizontal direction reveals the inter-chip fluctuations. The scattering of the measured points around a line with slope 1 reveals the intra-chip fluctuations between N1 and N3. As a result we can evaluate the intra- and inter-chip fluctuations for L_{gate}=2.1μm to be 11.6mV and 25.5mV, respectively. The measured I_{out} fluctuations shown in Fig. 2 and 3 reveal the relative fluctuations between N3 and N4. On the contrary, the extracted fluctuation in Fig. 8 is between N1 and N3. Since the two transistor pairs N1/N3 and N3/N4 have similar geometrical spacings, measured magnitude of intra-chip fluctuations is also similar. The advantage is that the intra inter separation method proposed here is a simple and direct approach. Fig. 9 shows the separation of intra- and inter-chip fluctuations for the L_{gate}=0.6μm case.

The obtained fluctuation data is summarized in Table I. Here we emphasize an interesting feature of this fluctuation data. With decreasing L_{gate} the intra-chip fluctuations increase much faster than inter-chip fluctuations. If this trend can be extrapolated to smaller L_{gate}, it is a severe concern especially for the design reliability of analog circuits.

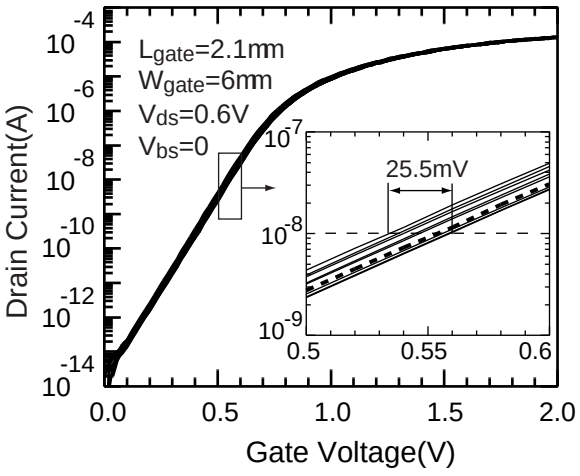

Fig. 6. Measured $I-V$ characteristics of single n-MOSFETs with L_{gate}=2.1μm on the 9 chips at $V_{ds} = 0.6V$ and bulk voltage V_{bs} = 0. The thick dashed line was taken as the nominal case.

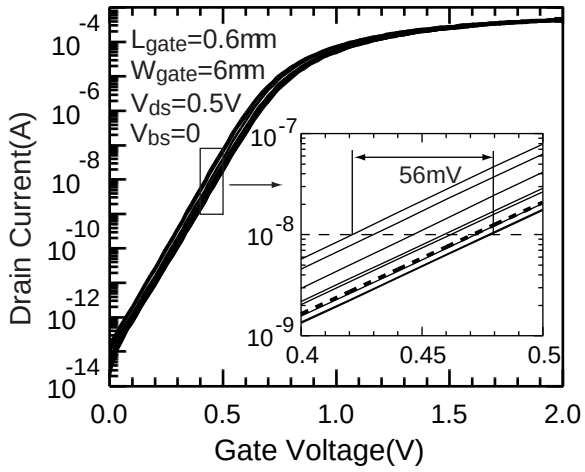

Fig. 7. The same plot as Fig. 6 but for L_{gate}=0.6μm at $V_{ds} = 0.5V$ and $V_{bs} = 0$.

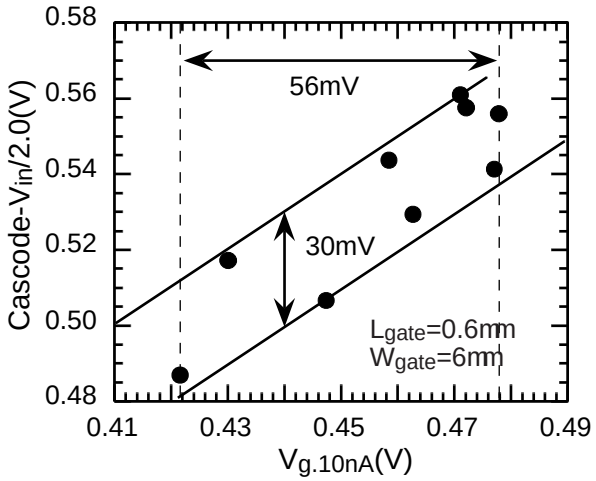

Fig. 9. The same correlation as Fig. 8 but for L_{gate}=0.6μm. Inter-chip and intra-chip fluctuations are extracted to be 56mV and 30mV, respectively.

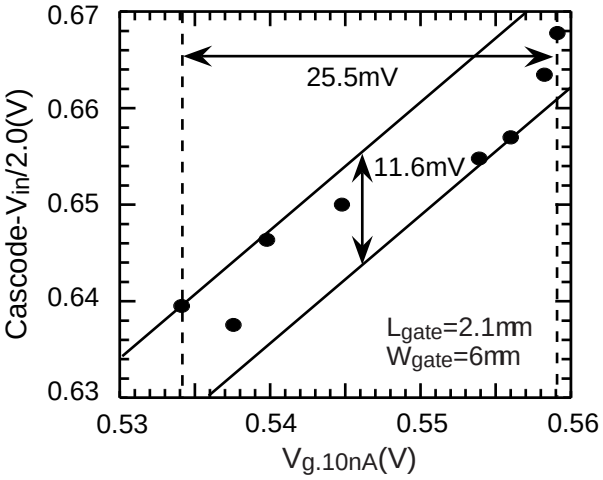

Fig. 8. Measured correlation between $V_{in}/2$(expected gate potential on N1) and $V_{g.10nA}$ of a single n-MOSFET on the same chip. All together data of 9 chips are depicted. Inter-chip and intra-chip fluctuations are extracted to be 25.5mV and 11.6mV, respectively.

IV. Modeling of the Correlation between Technology and Circuit-Performance Fluctuations

To verify the technological origin of the large intra-chip fluctuation of $V_{g.10nA}$ in comparison with the inter-chip fluctuation, simulation experiment is performed. To demonstrate the simulation reliability, I-V characteristics obtained with HiSIM [7,8] are compared with measured data in Figs. 10 and 11 for the nominal I-V characteristics of Figs. 6 and 7. The model parameter values for the fluctuation boundaries of the I-V characteristics are also extracted as demonstrated in Figs. 12 and 13. For the extraction only three model parameters, the substrate impurity concentration N_{sub}, the gate-oxide thickness T_{ox} and the deviation of the gate length from the design (ΔL_{gate}) are varied. ΔL_{gate} includes the fluctuation of L_{gate} and the horizontal out-diffusion length of the S/D contact beneath the gate. Since our investigation is restricted to the subthreshold characteristics, the fluctuation of the contact resistance was neglected. Nevertheless, the parameter extraction justifies this neglection even in the strong inversion region.

The deviation of extracted parameter sets from the nominal process target is listed in Table II. The reliability of the extracted model-parameter fluctuations is proved by the agreement over a wide range of the V_{bs} variations. The T_{ox} fluctuation seems negligibly small and allways above the process target for the technology studied here. The extracted parameter sets reveal that the L_{gate} and the N_{sub} fluctuations are the major concern for the inter-chip fluctuation. Since the 9 chips are randomly selected from a lot, there are no corelations among fluctuations. Fig. 14 shows simulated sensitivities of the three model parameters at $V_{g.10nA}$. The sensitivity of ΔL_{gate} for L_{gate}=0.6μm is strongly enhanced as can be expected. That of N_{sub} is only a bit larger for L_{gate}=0.6μm than that for L_{gate}=2.1μm. However, that of T_{ox} shows opposite dependence due to the short-channel nature of the characteristics for L_{gate}=0.6μm. With these sensitivities the cause of the intra-chip $V_{g.10nA}$ fluctuation listed in Table I is estimated as shown in Table III. For the estimation the T_{ox} fluctuation is ignored. The inter-chip fluctuation in Table III is taken from the maximum fluctuations listed in Table II.

Since we have only 9 chip measurements and statistically not sufficient, the boundaries of measured I-V char-

acteristics are not symmetrical. Here we assumed that the nominal values should be in the middle of the fluctuations, if we have enough statistics. The reason for the relatively large intra-chip fluctuations of ΔL_{gate} in comparison with the inter-chip fluctuations is probably due to the layout of the design, which didn't include dummy gates for increased uniformity of the active gate etching. Usually 3σ values of Gaussian distributions determine the inter-chip fluctuation boundaries. Our extracted values in Table III are a bit smaller than the values given in literature [9]. The reason may be an improved technology in comparison to the earlier period.

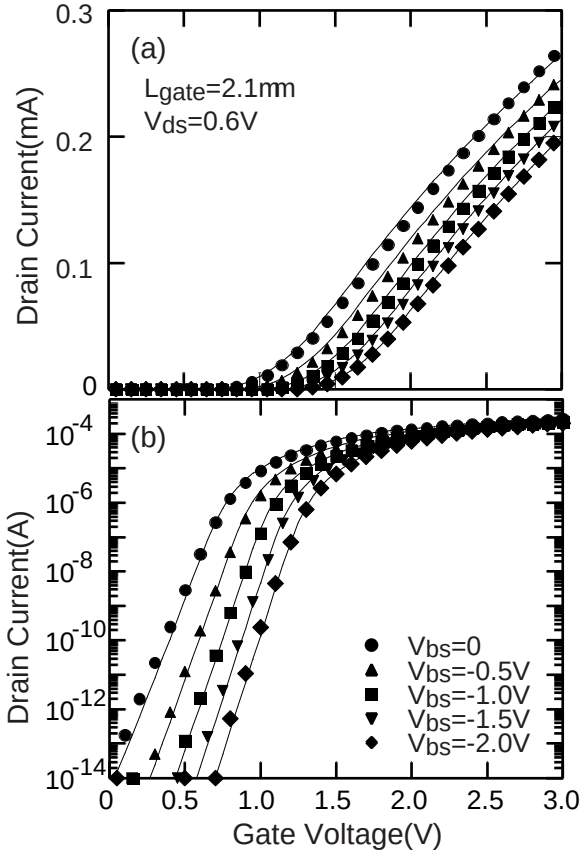

Fig. 10. Comparison of measured $I-V$ characteristics with simulated results of the nominal case in Fig. 6 and L_{gate}=2.1μm. Symbols are measurements and solid lines are simulation results of (a) linear plot, and (b) logalithmic plot.

TABLE I
EXTRACTED INTRA- AND INTER-CHIP FLUCTUATIONS OF $V_{g.10nA}$ FROM MEASURED CASCODE CHARACTERISTICS.

L_{gate}	intra	inter
2.1μm	11.6mV	25.5mV
0.6μm	30mV	56mV

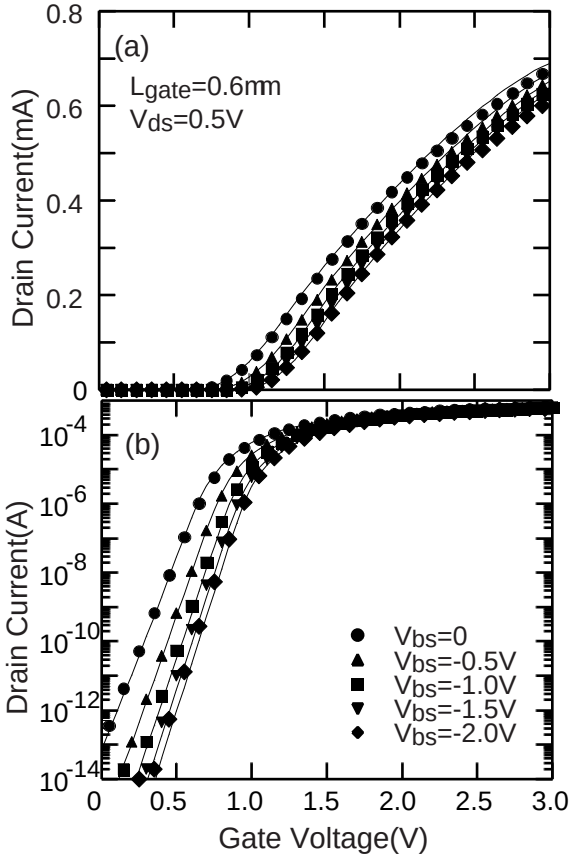

Fig. 11. The same comparison as Fig. 10 but for L_{gate}=0.6μm.

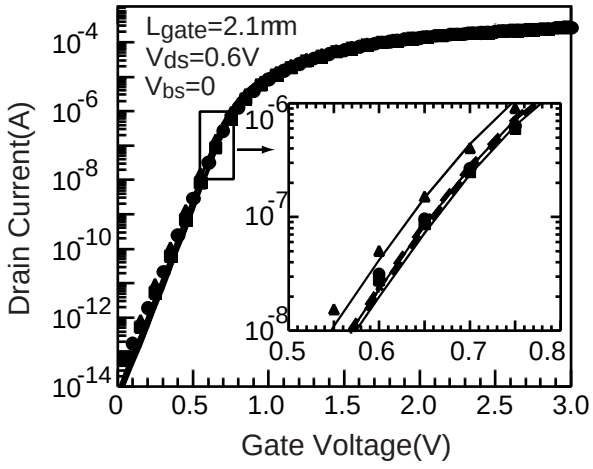

Fig. 12. Comparison of mearured $I-V$ characteristics (symbols) of the nominal case and measurement boundaries with simulated results (lines) for L_{gate}=2.1μm.

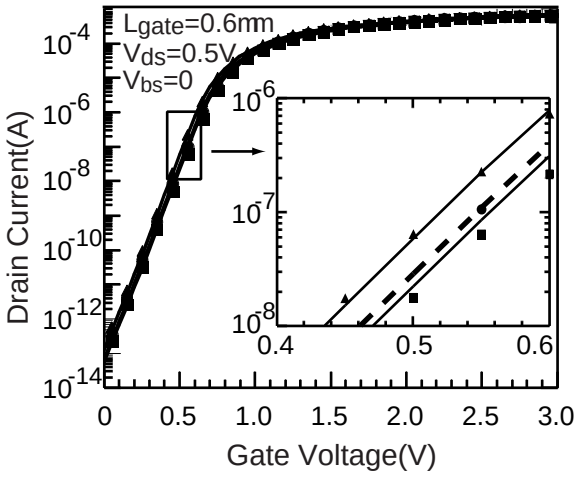

Fig. 13. The same comparison as Fig. 12 but for L_{gate}=0.6μm.

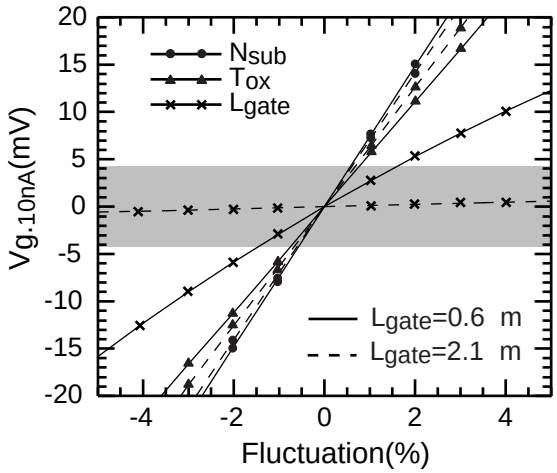

Fig. 14. Sensitivity analysis of three model parameters. Change of the parameter values in % results in a change of the $V_{g.10nA}$ value in mV.

V. Discussion and Conclusion

Though we performed our investigation only with 9 chips here, a rather thorough insight into the correlation between circuit-performance and technology fluctuations could be obtained. This is attributed to the method of using a test circuit which operates in the technologically sensitive subthreshold region and a drift-diffusion MOSFET model for establishing this correlation. Of course our method can be extended to a large amount of measurement data for better statistics as well as to other test circuits.

In conclusion we have proposed and successfully verified a correlation method of circuit performance and technology fluctuations. This method is expected to be helpful for improving design reliability with coming MOSFET generations.

TABLE II

Extracted inter-chip deviations of model-parameter values from nominal values as demonstrated in Fig. 12 and 13. "high" means the boundary case with larger $V_{g.10nA}$ and "low" means that with smaller $V_{g.10nA}$.

	high	low
ΔN_{sub}	-1.2%	-7%
ΔT_{ox}	$+1.4\%$	$+0.7\%$
$\Delta L_{gate}/0.6\mu m$	$+6.7\%$	-3.3%

TABLE III

Resulting model-parameter fluctuations from nominal values causing intra- and inter-chip fluctuations of $V_{g.10nA}$.

	ΔN_{sub}	ΔT_{ox}	ΔL_{gate}
intra	$\pm 0.6\%$	~ 0	$\pm 3.8\%$
inter	$\pm 7\%$	$\pm 1.4\%$	$\pm 6.7\%$

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