High-Speed FIR Digital Filter with CSD Coefficients Implemented on FPGA

Mitsuru Yamada
Akinori Nishihara
Graduate School of Science and Engineering, Tokyo Institute of Technology
2-12-1, Ookayama, Meguro-ku, Tokyo, 152-8552, Japan
Tel: 03-5734-2560, e-mail: myamada@ss.titech.ac.jp

Abstract- A very fast and low-complexity FIR digital filter on FPGA is presented. Multipliers in the filter whose coefficients are expressed as canonic signed digit (CSD) code are realized with wired-shifters, adders and subtracters. The critical path is minimized by insertion of pipeline registers and is equal to the propagation delay of an adder. The number of pipeline registers is limited by using an equivalent transformation on a signal flow graph. The price paid for the 100% speedup is 5% increase in the area. The maximum sampling frequency is 78.6MHz.

1. INTRODUCTION

In the implementation of high speed FIR digital filters, computational speed and the die area of the multiplier are the main key issues. Multipliers with CSD coefficients can be realized using wired shifters, adders and subtracters without using conventional multipliers[1]. We show an FPGA implementation example of FIR digital filters having CSD coefficients, where pipelining and other techniques are used to minimize the critical path and to reduce the die area. In this method, the critical path can be made the minimum as the delay of a single adder. Therefore, the critical path is properly shorter than [1]'s.

2. DESIGN PROCEDURE

Design of these filters is formulated as the integer programming with the FIR filter’s coefficient as variables [2]. The tolerant range of desired frequency response of the filter is specified as constraints of the integer programming. Table 1 shows the specifications and the resultant filter coefficients of the design example. Figure 1 shows the frequency response and Fig.2 shows the block diagram of the designed filter.

<table>
<thead>
<tr>
<th># of taps : 15</th>
<th>$h_0, h_{14} = -1$</th>
<th>$h_4, h_{10} = -19$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coefficient : 8 bit</td>
<td>$h_1, h_{13} = 0$</td>
<td>$h_5, h_9 = 0$</td>
</tr>
<tr>
<td>Nonzero digit : 3</td>
<td>$h_2, h_{12} = 6$</td>
<td>$h_6, h_8 = 78$</td>
</tr>
<tr>
<td>DC gain : $2^8$</td>
<td>$h_3, h_{11} = 0$</td>
<td>$h_7 = 128$</td>
</tr>
</tbody>
</table>

Figure 1: Design example of a half-band filter

Figure 2: Block diagram of the designed FIR filter

3. FEATURE OF FPGA

FPGAs consist of large logic blocks that are configured. The logic blocks consist of a D-type flip-flop (DFF) and a configurable look-up table (LUT) which has several inputs. Figure 3(a) shows the case where the only an adder is implemented in a logic block, and Fig.3(b) shows the case where an adder and a delay element are implemented. In the latter case, a delay element is implemented by enabling the DFF which is included in the adder’s logic block. Thus putting a delay element just after an adder does not increase the area at all.

The above observation shows that delay elements can be inserted between consecutive adders or subtracters as
pipeline registers to minimize the critical path of the filter without increasing the area.

\[ \begin{align*}
\text{Fig. 3: Implementation of an adder and an adjacent delay element in FPGAs} & \\
\end{align*} \]

4. MINIMIZATION OF CRITICAL PATH

The input signal word length is specified as 12-bit in this design and the maximum internal word length is 20-bit.

First, in order to reduce the critical path, delay elements are inserted between adders which act as a part of multiplication. Suppose the propagation delay of an adder is \( T_a \), and the number of nonzero digits of the filter coefficients is \( N_z \). In the conventional signal flow shown in Fig.2, the length of the critical path is \( N_z T_a \). After the pipeline registers are inserted, it becomes minimum of \( T_a \), the propagation delay of a single adder. In this case, the length of the critical path decreases to 33 % as shown in Table 2.

\[ \begin{align*}
\text{Table 2: Implementation result for the FPGA} & \\
\hline
\text{Fig. 2} & \text{Fig. 4} \\
\hline
\text{Signal word length} & 12 \text{ bit} & 12 \text{ bit} \\
\# of adders & 14 & 14 (100 \%) \\
\# of delay elements & 14 & 21 (150 \%) \\
\text{Critical path length (Adder)} & 3 & 3 (33 \%) \\
\text{Group-delay} & 7 & 9 (129 \%) \\
\text{Area (Logic block)} & 204 & 215 (105 \%) \\
\text{Actual critical path length} & 25.3 \text{ ns} & 12.7 \text{ ns (50 \%)} \\
\text{Sampling frequency} & 39.5 \text{ MHz} & 78.6 \text{ MHz} \\
\hline
\end{align*} \]

Minimization of the critical path increases the area to 105 %, where the area is measured by the number of logic blocks used. Although the critical path length is estimated to decrease to 33 %, the actual critical path decreases to 50 %. Thus the maximum sampling frequency is obtained as 78.6 MHz.

This FPGA device is installed onto an evaluation board with an A-D converter and a D-A converter. The observed response is the same as Fig.1 by using an analog gain-phase analyzer.

From the above, in implementation on FPGAs, the length of critical path of the FIR filter with CSD coefficients can be reduced without much increase in the area. Improvement of operating speed for FIR filters by using the proposed method is confirmed to be effective for FPGAs.

6. CONCLUSIONS

A special feature in internal structure of FPGAs is presented. With that in mind FIR digital filter structures are modified so that the length of critical path becomes minimum of a single adder. It is proved that despite delay elements are inserted into the designed FIR filter, the area increase is only a little. Therefore, high speed, compact and linear-phase FIR digital filters are obtained.

REFERENCES
