ASP-DAC
Asia and South Pacific Design Automation Conference 2001
January 30 - February 2, 2001
Pacifico Yokohama, Yokohama, Japan

Click on the text below to go to:

ASP-DAC’2001:

Cover Page
Front Matter
Table of Contents
Session Index
Author Index
ASP-DAC 2001
Asia and South Pacific Design Automation Conference 2001
with
Electronic Design and Solution Fair 2001
January 30 – February 2, 2001
Pacifico Yokohama
Yokohama, Japan
ASP-DAC 2001 Organizing Committee

General Chair
Satoshi Goto
NEC Corporation
4-1-1 Miyazaki, Miyamae-ku,
Kawasaki 216-8555 Japan
Phone: +81-44-856-2006
FAX: +81-44-856-2021
sgoto@rdg.cl.nec.co.jp

TPC Co-Chairs
Hiroto Yasuura
Kyushu Univ.

Secretaries
Masaaki Yamada
Toshiba Corporation
mm.yamada@toshiba.co.jp

Ravi Pai
Silicon Automation Systems Ltd.

Takeshi Yoshimura
NEC Corporation
yoshi@ccm.cl.nec.co.jp

TPC Vice Chair
Masaharu Imai
Osaka Univ.

Past Gen. Chair
Kenji Yoshida
STARC

TPC Secretaries
Hiroshi Date
Institute of Systems &
Information Technologies
KYUSHU

Steering Committee Chair
Tatsuo Ohtsuki
Waseda Univ.

Tohru Ishihara
The Univ. of Tokyo

Assistant Secretary
Kazutoshi Wakabayashi
NEC Corp.

Design Contest Co-Chairs
Hidetoshi Onodera
Kyoto Univ.
ASP-DAC Rep. at DAC
Hidetoshi Onodera
Kyoto Univ.

ASP-DAC Rep. at DATE
Tokinori Kozawa
STARC

IEICE / TGICD Rep.
Norihisa Kitagawa
Texas Instruments Japan

IEICE / TGCAS Rep.
Hisakazu Kikuchi
Niigata Univ.

IEICE / TGVLD Chair
Hidetoshi Onodera
Kyoto Univ.

IPSJ / SIGDA Chair
Hirofumi Hamamura
Fujitsu Ltd.

JIEP Rep.
Masao Yanagisawa
Waseda Univ.

JEITA Rep.
Yosifumi Okamoto
Matsushita Electric Industrial Co., Ltd.
ASP-DAC 2001 Steering Committee

Chair
Tatsuo Ohtsuki
Dept. of Electronics, Information & Communication Engrg.
Waseda Univ.
3-4-1 Okubo, Shinjuku,
Tokyo 169-8555 Japan
Tel: +81-3-5286-3387
Fax: +81-3-3203-9184
to@ohtsuki.comm.waseda.ac.jp

Vice Chair
Fumiyasu Hirose
Cadence Design Systems, Japan
hirose@cadence.com

IEEE CAS Representative
Ellen J. Yoffa
IBM Corporation

Secretary
Tsuneo Nakata
Fujitsu Laboratories Ltd.
nakata@flab.fujitsu.co.jp

DAC Representative
Jan M. Rabaey
University of California at Berkeley

ASP-DAC 2000 General Chair
Kenji Yoshida
STARC

DATE Representative
Peter Marwedel
University of Dortmund

ASP-DAC 2001 General Chair
Satoshi Goto
NEC Corporation

JEITA Representative
Yoshifumi Okamoto
Matsushita Electric Industrial Co., Ltd.

STARC Representative
Tokinori Kozawa
STARC

ACM SIGDA Representative
Nikil Dutt
University of California at Irvine

eD&S Fair Chair
Yoshimune Hagiwara
Hitachi Limited
IEICE TGCAS Chair
Hisakazu Kikuchi
Niigata University

Xian-Long Hong
Tsinghua University, Beijing

IEICE TGVLD Chair
Hidetoshi Onodera
Kyoto University

Chong-Min Kyung
Korea Advanced Institute of Science and Technology

IEICE TGICD Chair
Norihisa Kitagawa
Texas Instruments, Japan

Hon-Wai Leong
National University of Singapore

IPSJ SIGSLDM Chair
Hirofumi Hamamura
Fujitsu Limited

Youn-Long Steve Lin
Tsing Hua University, Hsin-Chu

JIEP Representative
Masao Yanagisawa
Waseda University

Sunil D. Sherlekar
Silicon Automation Systems (INDIA) PVT. LTD.

International Members
Richard M M Chen
City University of Hong Kong

David Skellern
Macquarie University

Graham R. Hellestrand
University of New South Wales

Alexander Stempkovsky
Russin Academy of Science
ASP-DAC 2001 General Chair’s Message

Welcome to ASP-DAC 2001

On behalf of the Organizing Committee, I would like to welcome you to the Asia and South Pacific Design Automation Conference 2001 (ASP-DAC 2001). This year’s ASP-DAC will be held again in the Pacifico Yokohama, Japan, jointly with Electric Design and Solution Fair 2001. The goal of the ASP-DAC is to provide an international forum for researchers and engineers in academia and industry, in the area of electronic system/VLSI design, and DA/CAD. ASP-DAC is a sister conference of DAC in the USA and DATE in Europe.

We have three excellent keynote speakers this year, who will talk about future directions of Electronics Industries and VLSI design technologies. Dr. Hajime Sasaki, Chairman of NEC Corporation, will give a talk on the role of Semiconductor Industry in the 21st Century. Dr. Ming-Jeh Chien, Chairman of First International Computer, Taiwan, will talk about Market and Technology in PC Products. Dr. Raul Camposano, Chief Technical Officer of Synopsys, USA, will talk on EDA Challenge to SOC solutions. I believe that these three distinguished talk will inspire the attendants to understand and predict the next generation VLSI design technologies.

This year, the Technical Program Committee, under the leadership of Prof. Hiroto Yasuura, Dr. Ravi Pai and Prof. Masaharu Imai reviewed 147 papers to select this year's outstanding Program. 90 papers are selected for their technical excellence, with an emphasis to bring new ideas, new subjects, improved methods and outstanding technical presentations to the Conference.

Papers selected have been organized into four trucks which cover the wide variety of hot topics from system design level to physical design. They also include special sessions such as panels, embedded tutorials. Among them, a special panel is scheduled just after the opening session on Wednesday and another truck consisting of special sessions is planned on Thursday.

A unique feature of ASP-DAC is the University LSI Design Contest, which focuses a real chip design in academia. 19 designs have been selected for poster presentation, from which 3 award winners will be announced at the conference.

On Tuesday, five full day tutorials are scheduled to give complete introductions of state-of-the-art design/CAD topics; (1)SpecC: Specification language and design methodology, (2)IP authoring and SOC integration, verification, and testing, (3)Software development methods for embedded systems, (4)Integrating logic synthesis and timing closure layout for DSM, (5)Design issues regarding wire-line/wireless network chip implementation.

Recent IT revolution is now facing tremendous challenges caused by accelerated scaling down and ever increasing complexity of System-on-Chip. I believe the ASP-DAC 2001 will be a precious opportunity for you to find valuable information by exchanging ideas with CAD researchers, CAD developers, and VLSI designers.

I hope you will have a valuable and enjoyable experience at Yokohama, Japan.

Satoshi Goto
General Chair, ASP-DAC 2001
ASP-DAC 2001 Technical Program Committee

Co-Chairs

Hiroto Yasuura
Kyushu Univ., Japan
yasuura@cc.csee.kyushu-u.ac.jp

Ravi Pai
Silicon Automation Systems, India
pai@sasi.com

Vice Chair

Masaharu Imai
Osaka Univ., Japan
imai@ics.es.osaka-u.ac.jp

Secretaries

Hiroshi Date
Inst. of Systems & Information Technologies KYUSHU, Japan
date@k-isit.or.jp

Tohru Ishihara
Univ. of Tokyo, Japan
ishihara@silicon.u-tokyo.ac.jp

Subcommittee Members :
(* indicates the subcommittee chair)

[1] System Design Methodology

*Yoshinori Takeuchi
Osaka Univ., Japan

Rajesh Gupta
UC Irvine, U.S.A.

Tadatoshi Ishii
Toshiba, Japan

Nagisa Ishiura
Osaka Univ., Japan

Tsuyoshi Isshiki
Tokyo Institute of Technology, Japan

Ahmed Amine Jerraya
TIMA, France

Koichi Sato
NEC, Japan

Nozomu Togawa
Waseda Univ., Japan

Hiroyuki Tomiyama
UC Irvine, U.S.A.

Serge Vernalde
IMEC, Belgium

Masayuki Yamaguchi
SHARP, Japan

[2] Synthesis and Verification in Logic Design

*Masahiro Fujita
Univ. of Tokyo, Japan

Shih-Chieh Chang
National Chung-Cheng Univ., Taiwan

Supratik Chakraborty
IIT Bombay, India

Ed Clarke
CMU, U.S.A.

Hans Eveking
Technical Univ. of Darmstadt, Germany

Jing-Yang Jou
National Chiao Tung Univ., Taiwan

Rajeev Murgai
Fujitsu Laboratories of America, U.S.A.

S. Ramesh
IIT Bombay, India

Hiroshi Sawada
NTT, Japan

Yutaka Tamiya
Fujitsu Lab., Japan

Tiziano Villa
Parades, Italy

Ching-Wei
National Chung-Cheng Univ., Taiwan

Tomohiro Yoneya
Tokyo Institute of Technology, Japan


*Masahiro Fukui
Matsushita, Japan

Yao-Wen Chang
National Chiao Tung Univ., Taiwan

Ikuo Harada
ATR, Japan

Xianlong Hong
Tsinghua Univ., China

Masanori Imai
STARC, Japan

Tomonori Izumi
Kyoto Univ., Japan

Tetsushi Koide
Univ. of Tokyo, Japan

Takumi Okamoto
NEC, Japan
Shunji Saika  
Matsushita, Japan

Hyunchul Shin  
Hanyang Univ., Korea

Yoichi Shiraiishi  
Gunma Univ., Japan

C. K. Wong  
The Chinese Univ. of Hong Kong, China


*Seiji Kajihara  
Kyushu Inst. of Tech., Japan

Kwang-Ting (Tim) Cheng  
UC Santa Barbara, U.S.A.

Hiroshi Date  
ISIT, Japan

Kazumi Hatayama  
Hitachi, Japan

Tomoo Inoue  
Hiroshima City Univ., Japan

Yukiya Miura  
Tokyo Metropolitan Univ., Japan

Chauchin Su  
National Central Univ. Taiwan

Cheng-Wen Wu  
National Tsing Hua Univ. Taiwan

Masaaki Yoshida  
NEC, Japan


*Kimihiro Ogawa  
Sony LSI, Japan

Akira Hyogo  
Science Univ. of Tokyo, Japan

Yasuaki Inoue  
Univ. of East Asia, Japan

Kenneth S. Kundert  
Cadence, U.S.A.

Toshiyuki Saito  
NEC, Japan

Akio Ushida  
Tokushima Univ., Japan

Chorng-kuang Wang  
National Taiwan Univ., Taiwan

Jacob White  
MIT, U.S.A.

Goichi Yokomizo  
Hitachi, Japan


*Mitiko Miura-Mattausch  
Hiroshima Univ., Japan

Uwe Feldmann  
Infineon Technologies, Germany

Kiyoshi Ishikawa  
Mitsubishi, Japan

Boon-Khim Liew  
TSMC, Taiwan

Hiroshi Masuda  
STARC, Japan

Hiroshi Matsumoto  
NEC, Japan

Mikako Miyama  
Hitachi, Japan

Naoyuki Shigyo  
Toshiba, Japan

T. Toyabe  
Toyo Univ., Japan


*Hiroaki Takada  
Toyohashi Univ. of Technology, Japan

Naehyuck Chang  
Seoul National Univ., Korea

Pai H. Chou  
UC Irvine, U.S.A.

Rolf Ernst  
TU Braunschweig, Germany

Ing-Jer Huang  
National Sun-Yat-Sen Univ., Taiwan

Peter Marwedel  
Univ. of Dortmund, Germany

Hiroshi Monden  
NEC, Japan

Tatsuo Nakajima  
Waseda Univ., Japan

Shigeki Nankaku  
Mitsubishi, Japan

Kiichiro TAMARU  
Toshiba, Japan
[8] Reconfigurable Systems

*Hiroto Yasuura  
Kyushu Univ., Japan

Hideharu Amano  
Keio Univ., Japan

Kiyongh Choi  
Seoul National Univ. Korea

Reiner Hartenstein  
Kaiserslautern Univ., Germany

Toshiaki Miyazaki  
NTT, Japan

Sri Parameswaran  
The University Of Queensland, Australia

Barry Shackleford  
HP Lab, U.S.A.

Allen C.-H. Wu  
Tsing Hua University, Taiwan

[9] Design Experiments

*Masakazu Yamashina  
NEC, Japan

Shekhar Borkar  
Intel, U.S.A.

Tadahiro Kuroda  
Keio Univ., Japan

Masataka Matsui  
Toshiba, Japan

Hiroyuki Mizuno  
Hitachi, Japan

Satoshi Matsushita  
NEC, Japan

[10] (Special Session) Asynchronous System Design

Dong-Ik Lee  
Kwangju Institute of Science and Technology, Korea

Tomohiros Yoneda  
Tokyo Institute of Technology, Japan
List of Reviewers

T. Asaka
F. D. Bernardinis
K. O. Boateng
Y. Cai
Y. Desaki
S. Dong
J. Eckmueler
M. Edahiro
J. Fujii
K. Fujiyoshi
W. Gosti
K. Hachiya
M. Hashimoto
M. Hashizume
M. Heissmeier
J. Henkel
Y. Higami
H. Higuchi
C. Hillermeier
S. Hoereth
T. Hoffmann
M. Itoh
K. Iwasaki
H. Iwashita
W. Jacobs
J. Jeon
T. Kakuda
T. Kam
S. Kamohara
D. Kim
K. Kobayashi
S. Kobayashi
Y. Kubo
W. Kunz
A. Kurokawa
M. Lajolo
L. Lavagno
P. M. Lee
S.-I. Liu
B. Ludwig
L. Mangeruca
Y. Matsunaga
A. Moniwa
M. Moukara
U. Nageldinger
Y. Nakamura
T. Nakata
S. Nakatake
Y. Nishida
K. Okada
A. D. Oliveira
T. Ono
A. Ragunathan
K. Sakanushi
M. Sanada
H. Sato
T. Sato
A. Seidl
V. Singhal
S. Sinha
F. Somenzi
N. Takagi
A. Takahashi
Y. Takashima
M. Tanno
K. Tsukada
L. Weiss
J.-H. Won
W. Wu
J.-T. Wu
H. Yamazaki
T. Yanagihara
H. Yotsuyamagi
Technical Program Co-Chairs’ Message

On behalf of the Technical Program Committee of ASP-DAC 2001, we would like to welcome all of you to ASP-DAC 2001, the first conference on EDA and design technologies in the new century.

The Technical Program Committee of ASP-DAC 2001 is organized by 88 EDA and LSI design professionals with 9 subcommittees. Each subcommittee selected high quality papers on System Design Methodology, Synthesis and Verification in Logic Design, Optimization and Verification in Physical Design, Test Technology and Design for Testability, Analog Circuit Design, Design for Manufacturability, Embedded Systems and Software, Reconfigurable Systems, and Design Experiments, respectively. Prof. Dongik Lee also independently organized a committee for special sessions on “Asynchronous System Design”. 161 papers were submitted to the regular and special sessions from 20 countries/regions. 83 papers are accepted as regular papers and 14 papers for short presentation. In the accepted papers, 80 papers are from academia. Best paper awards are presented to the highest quality papers among all accepted papers. 2 papers are awarded by the Best Paper Selection Committee in the Technical Program Committee.

These technical papers are complemented by an exciting mix of a panel discussion and invited talks on hot topics as well as educational embedded tutorials. Prof. Hidetoshi Onodera moderates a panel discussion entitled “Beyond the Red Brick Wall: Challenges and Solutions in 50nm Physical Design”. Four distinguish researchers are invited as invited speakers and their talks will address the directions of design methodologies for ultra deep submicron era (A6-a and B1-3), low power circuit design (C4-1) and system synthesis technology (C2-1). Eight tutorial talks by top scientists are also embedded in the technical sessions. The subjects of the embedded tutorials cover recent important progresses in design for manufacturability (B2-3), mixed signal simulation (B4-4), test technology (D4-1), low power design and compiler techniques for embedded systems (D3-1 and D5-1), and reconfigurable computation (C7-3). Another 2 tutorial talks on asynchronous system design are embedded in the special sessions (E3-1 and E4-1).

As co-chairs of Technical Program Committee, we want to thank all of members of the committee, people who reviewed papers, moderators of sessions, and all of authors and speakers who submitted papers and will give talks in the conference. We also appreciate the publication chair, Prof. Kiyoharu Hamaguchi and TPC secretaries, Dr. Hiroshi Date and Dr. Tohru Ishihara for their dedications to prepare the technical program and the proceedings. Thanks are also due to Mr. Makoto Sugihara and Mr. Sozo Inoue, who developed and maintained an electric submission and review system, which is firstly introduced to this conference. Their efforts made the conference more popular and more international.

We hope that you will find new directions of EDA and design technologies in the program and the proceedings of ASP-DAC 2001.

Hiroto Yasuura   Ravi Pai
Co-Chairs, ASP-DAC 2001 Program Committee
ASP-DAC 2001 Best Papers

B1.1 “Correlation Method of Circuit-Performance and Technology Fluctuations for Improved Design Reliability”,

C6.3 “Design Rewiring Based on Diagnosis Techniques”,
A. Veneris (Univ. of Toronto, Canada), M. S. Abadir (Motorola Inc, USA), I. Ting (Alcatel Corp, Canada)
University LSI Design Contest Committee

Co-Chairs
Hidetoshi Onodera
Kyoto Univ., Japan
onodera@kuee.kyoto-u.ac.jp

S. K. Nandy
Indian Institute of Science, India
nandy@serc.iisc.ernet.in

Vice Chair
Tadahiro Kuroda
Keio University, Japan
kuroda@elec.keio.ac.jp

Members
Hideharu Amano
Keio Univ., Japan

Takafumi Aoki
Tohoku Univ., Japan

Tadayoshi Enomoto
Chuo Univ., Japan

Akira Hyogo
Science Univ. of Tokyo, Japan

Makoto Ikeda
Univ. of Tokyo, Japan

Shoji Kawahito
Shizuoka Univ., Japan

Koji Kotani
Tohoku Univ., Japan

Hajime Kubosawa
Fujitsu, Japan

Masataka Matsui
Toshiba, Japan

Yasuyuki Matsuya
NTT, Japan

Hiroyuki Mizuno
Hitachi, Japan

Masato Motomura
NEC, Japan

Kazuaki Murakami
Kyushu Univ., Japan

Makoto Nagata
Hiroshima Univ., Japan

Borivoje Nikolic
UC Berkeley, U.S.A.

Vojin G. Oklobdzija
UC Davis, U.S.A.

Takao Onoie
Kyoto Univ., Japan

In-Cheol Park
KAIST, Korea

Kazuo Taki
Kobe Univ., Japan

Chi-Ying Tsui
Hong Kong Univ. of Science and Technology, China

Toshiro Tsukada
Hitachi, Japan

Ingrid Verbauwhede
UCLA, U.S.A.

Tomohisa Wada
Univ. of Ryukyus, Japan

Kazuyoshi Waki
Rohm, Japan

Hoi-Jun Yoo
KAIST, Korea
University LSI Design Contest Co-Chairs’ Message

The University LSI Design Contest was conceived as a unique program of ASP-DAC Conference. The purpose of the Contest is to encourage education and research in LSI design, and its realization on chips at universities, and other educational organizations by providing the opportunities to present and discuss innovative and state-of-the-art designs at the conference.

Application areas and types of circuits include (1) Analog and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, and (4) Custom Application Specific Circuits. Methods or technology used for implementation include (a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices, including FPGA/PLDs. Actual implementation on real devices is mandatory.

This year, nineteen selected designs from four countries/areas will be disclosed in Session A1 with a short presentations followed by live discussions in front of posters. Two out of the nineteen designs are in analog and mixed signal circuits, five designs span applications in digital signal processing, two microprocessor designs, and ten custom application specific circuits. Demonstrations on the achievements will also be made for some of the designs. Opportunities for demonstrations at eD&S Fair 2001 will be provided for the above designs.

Submitted designs were reviewed by the members of the University Design Contest Committee based on the following criteria: Reliability of design and implementation, Quality of implementation, Performance of the design, Novelty, and Additional Special features. In the selection process, emphasis was placed more on reliability, quality, and performance. As a result, the nineteen designs were selected. Also, we have instituted one outstanding design award and two special feature awards.

It is with great pleasure that we acknowledge the contributions to the Design Contest, and it is our earnest belief that it will promote and enhance research and education in LSI design in academic organizations. It is also our hope that many people not only in academia but in industry will attend the contest and enjoy the stimulating discussions.

Hidetoshi Onodera and S.K.Nandy
Co-Chairs, University LSI Design Contest Committee

Tadahiro Kuroda
Vice Chair, University LSI Design Contest Committee
ASP-DAC 2001 University LSI Design Contest Awards

Outstanding Design Award

Single Chip 3D Rendering Engine Integrating Embedded DRAM Frame Buffer and Hierarchical Octet Tree (HOT) Array Processor with Bandwidth Amplification
Yong-Ha Park, *Seon-Ho Han, and Hoi-Jun Yoo
(Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, *Electronics and Telecommunications Research Institute)

Outstanding Design Award presented for the implementation of a high performance rendering engine integrating array processors in a hierarchical octet tree structure with embedded DRAM buffers for low power and high bandwidth operations.

Special Feature Award

A Smart Position Sensor for 3-D Measurement
Tomohiro Nezuka, Masashi Hoshino, Makoto Ikeda, and Kunihiro Asada
(Department of Electronics Engineering, VLSI Design and Education Center, The University of Tokyo)

Special Feature Award presented for a smart position sensor for 3-D measurement integrating a pixel array with variable block address decoder that enables quad-tree scan for efficient position sensing.

Special Feature Award

A Parallel Vector Quantization Processor Featuring An Effective Search Algorithm for Real-time Motion Picture Compression
Toshiyuki Nozawa, Makoto Imai, Masanori Fujibayashi, and Tadahiro Ohmi
(Department of Electronic Engineering, Tohoku University, New Industry Creation Hatchery Center, Tohoku University)

Special Feature Award presented for a parallel vector quantization processor incorporating a two-step search algorithm for real-time encoding of moving pictures.
Keynote Address I

“Role of the Semiconductor Industry in the 21st Century
= Human Talent is the heart of the Information Society =”

Hajime Sasaki

Chairman, NEC Corporation, Japan

The impact of the rapidly expanding IT Revolution can be compared to the invention in the 15th century of the Gutenberg printing press. It has often been said that the information age is around the corner, but it is clearly occurring now.

There are three major revolutionary changes that have led to the information society. First is the breakthrough development of semiconductor technology, which began with the invention of the transistor, the base of today’s most complicated semiconductors. Second is the development of the Internet, which has made it possible to distribute information on a worldwide scale. Last is the Mobile revolution, which has truly placed the power of the information revolution in the individual’s pocket. Through Mobile tools and Internet infrastructure, the power of knowledge will be the driving force of social change. This is the heart of the Information Society.

Over the past 50 years, the industrial seed supporting the Information Society has been the semiconductor. The application of this technology has progressed greatly from its birth in the monstrous ENIAC that calculated artillery distance to the present day PC computer that sits on your desktop. Moreover, the role of the semiconductor will continue its importance as the Internet and Mobile trend looks to continue its rapid growth.

However, there are certain challenges in front of the semiconductor industry’s growth path. One is found in the changing competitive landscape as evidenced by the blooming System on a Chip market. From now, IP strategy will be the factor determining success or failure. Scales of economy will not create winning products. It will be the most advanced technology that wins a customer’s order. Furthermore, market forces will efficiently match the right companies with the right IP at the right time.

As we approach the sub 0.1-micrometer design rule era, the main challenge faced is not in the hardware; on the contrary, it is faced in the ability to design chips that maximize the capability of the hardware. Up until now, the main focus of the semiconductor industry was to concentrate on the improvement of manufacturing equipment and the hardware itself. From now, the ability to enhance design efficiency will become just as important.

As the foundation of design is human knowledge, it is important to remember that education is critical to the enhancement and development of design technology. Investing in design equipment will not be the only way to bring about dramatic increases in productivity, as is the case in the hardware side of the business. Investment in developing qualified design engineers will be just as important. However, human knowledge cannot be developed in a day. It requires the combined efforts of industry, government and academia thinking from a strategic perspective to incubate the human talent necessary to ensure continued improvements in the semiconductor industry.
Keynote Address II

“Market and technology in PC products”

Ming-Jeh Chien

Chairman, First International Computer, Taiwan

The future will see continued PC growth supported by the internet applications.

On one hand, the increasingly - complicated applications and huge database demand high performance CPU. Software vendors now have the H/W to develop more processing intensive S/W in area such as MPEG-4, Audio/Video, Voice recognitions, virtual reality and internet gaming. This will certainly need leading technology to meet high speed/low power requirement.

On the other hand, explosive needs to access information through internet demand user - friendly devices such as internet appliances, PDA etc. Internet appliances are user - application oriented products. The success depends more on the marketing strategy than the leading technology. The good example is the cellular phone hand set. In fact, the boundary between phone and PDA is blurry, since PDA is including wireless communication capability.
System-on-Chip (SOC) design presents formidable challenges, with profound ramifications for the design tools needed. These challenges can be classified into three categories: technology, complexity, and system design.

First, advancing technology involves new materials, smaller feature sizes, and faster clock speeds. In this environment, what were previously parasitics become first-order effects. The first to impact design is the RC-delay (resistance-capacitance) of the wires or interconnect, which has resulted in the problem of timing closure. To obtain timing closure, it is necessary to unify synthesis, placement, and, eventually, routing into one electronic design automation (EDA) solution that can optimize logic and interconnect simultaneously. The next problem is the degradation of signal integrity, which can be caused by capacitive and inductive cross coupling, by IR voltage drop (current-resistance), and by substrate noise injection. The EDA tool solution in this case consists of fast and accurate analysis that can drive avoidance and correction of signal integrity problems primarily in routing, as well as in synthesis and placement. EDA tools must also increasingly address other unwanted side effects, such as electro migration, wire self-heat, hot electron device degradation, process antenna effect, and thermal stress.

The second challenge is complexity. Today, large SoCs consist of tens of millions of transistors, resulting in hundreds of millions of rectangles, with an increase of at least another order of magnitude over the next few years. The only way to address such large designs is through hierarchy (a chip composed of blocks) and the use of pre-designed blocks called “intellectual property” (IP). No SoC today is designed without using at least two levels of hierarchy, as well as IP in the form of memory, processors, etc. As a result, hierarchy support in EDA tools is essential. The trend towards hierarchical chip-level tools, such as extraction, synthesis, timing analysis, etc., is accelerating, adding to the complexity of the EDA tools themselves. Furthermore, a uniform treatment of hierarchy among related tools (or all tools) becomes a necessity.

The third challenge is in system design. As semiconductors become larger parts of electronic systems, all the way to a complete system on a chip, system design increasingly encompasses chip design and vice versa. This phenomenon increases the need for system-level EDA tools that integrate well with the traditional logical and physical tools used for chip design. System design is more domain specific, or vertical, than the more generic, or horizontal, logical and physical design. This difference results in various system-level abstractions, such as DSP, reactive control, protocols, etc., which must be addressed by EDA tools. Reaching for a higher level of abstraction poses even more challenges to the development of such tools.

This presentation poses EDA solutions to these challenges, gives concrete examples, and argues that complete solutions, rather than point tools, will increasingly and justifiably dominate the EDA field.
ASP-DAC 2001 Executive Panel Discussion

Secrets to Success in a Start-Up EDA Business

Organizer:  T. Kozawa - STARC, Japan
Moderator:  J. Goodsel - Simplex Solutions and CoWare
Panelists:  S. S. Wang - NAssda Corp.
           B. Rosenthal - Tensilica
           D. Fairbairn - Simutech Corp.
           M. Tsai - Axis
           H. Hasegawa - HD Lab.
Table of Contents

Organizing Committee ............................................................ iii
Steering Committee ............................................................... vi
General Chair’s Message ......................................................... x
Technical Program Committee ................................................. xi
List of Reviewers ................................................................. xiv
Technical Program Co-Chair’s Message ...................................... xv
Best Paper Awards ............................................................... xvi
University LSI Design Contest Committee ................................. xvii
University LSI Design Contest Co-Chair’s Message ....................... xviii
University LSI Design Contest Awards ...................................... xix
Keynote Addresses ............................................................... xx
Executive Panel Discussion ..................................................... xxiii

Session A1
(Special Session) University LSI Design Contest

Co-chairs: Hidetoshi Onodera, S. K. Nandy, Tadahiro Kuroda

A1.1 A Vector-Pipeline DSP for Low-Rate Videophones
Kazutoshi Kobayashi, Makoto Eguchi, Takuya Iwahashi, Takehide Shibayama,
Xiang Li, Kousuke Takai, Hidetoshi Onodera .................................. 1

A1.2 A High-Speed PLA Using Array Logic Circuits with Latch Sense Amplifiers
and a Charge Sharing Scheme
Hiroaki Yamaoka, Makoto Ikeda, Kunihiro Asada ............................. 3

A1.3 Multi-Hit Time-to-Digital Converter VLSI for High-Energy Physics Experiments
Yasuo Arai ................................................................. 5

xxiv
A1.4 High-Speed FIR Digital Filter with CSD Coefficients Implemented on FPGA
Mitsuru Yamada, Akinori Nishihara .............................................................. 7

A1.5 Single Chip 3D Rendering Engine Integrating Embedded DRAM Frame Buffer and Hierarchical Octet Tree (HOT) Array Processor with Bandwidth Amplification
Yong-Ha Park, Seon-Ho Han, Hoi-Jun Yoo ......................................................... 9

A1.6 A Dynamically Reconfigurable Hardware-Based Cipher Chip
Yukio Mitsuyama, Zaldy Andales, Takao Onoye, Isao Shirakawa ....................... 11

A1.7 Test Circuits for Substrate Noise Evaluation in CMOS Digital ICs
Makoto Nagata, Taka-fumi Ohmoto, Jin Nagai, Takashi Morie, Atsushi Iwata . . . . . 13

A1.8 Realtime Wavelet Video Coder Based on Reduced Memory Accessing
Roberto Y. Omaki, Yu Dong, Morgan H. Miki, Makoto Furuie, Daisuke Taki, Masaya Tarui, Gen Fujita, Takao Onoye, Isao Shirakawa .............................. 15

A1.9 A Prototype Chip of Multicontext FPGA with DRAM for Virtual Hardware
Daisuke Kawakami, Yuichiro Shibata, Hideharu Amano .................................... 17

A1.10 A Single-Inductor Dual-Output Integrated DC/DC Boost Converter for Variable Voltage Scheduling
Dongsheng Ma, Wing-Hung Ki, Chi-Ying Tsui, Philip K. T. Mok ....................... 19

A1.11 A Smart Position Sensor for 3-D Measurement
Tomohiro Nezuka, Masashi Hoshino, Makoto Ikeda, Kunihiro Asada .................. 21

A1.12 Parameterized MAC Unit Implementation
Ming-Chih Chen, Ing-Jer Huang, Chung-Ho Chen ............................................. 23

A1.13 A Parallel Vector Quantization Processor Featuring an Efficient Search Algorithm for Real-time Motion Picture Compression
Toshiyuki Nozawa, Makoto Imai, Masanori Fujibayashi, Tadahiro Ohmi .......... 25

A1.14 An 8-b nRERL Microprocessor for Ultra-Low-Energy Applications
Seokkee Kim, Jun-Ho Kwon, Soo-Ik Chae ....................................................... 27

A1.15 Design and Implementation of JPEG Encoder IP Core
Chung-Jr Lian, Liang-Gee Chen, Hao-Chieh Chang, Yung-Chi Chang ............ 29

A1.16 A Real-time 64-Monosyllable Recognition LSI with Learning Mechanism
Kazuhiro Nakamura, Qiang Zhu, Shinji Maruoka, Takashi Horiyama, Shinji Kimura, Katsumasa Watanabe ......................................................... 31

A1.17 Reusable Embedded In-Circuit Emulator
Ing-Jer Huang, Hsin-Ming Chen, Chung-Fu Kao ............................................. 33
A1.18 Flexible Processor Based on Full-Adder / D-Flip-Flop Merged Module
Satoshi Sakaidani, Naoto Miyamoto, Tadahiro Ohmi

A1.19 Development of PPRAM-Link Interface (PLIF) IP Core for High-Speed Inter-SoC Communication
Takanori Okuma, Koji Hashimoto, Kazuaki Murakami

Session B1
Device/Circuit Co-designing for Advanced Technologies
Co-chairs: Sani R. Nassif, Mikako Miyama

B1.1 Correlation Method of Circuit-Performance and Technology Fluctuations for Improved Design Reliability

B1.2 Realization of Semiconductor Device Synthesis with the Parallel Genetic Algorithm
Zhao Li, Xiaofeng Xie, Wenjun Zhang, Zhilian Yang

B1.3 (Invited Talk) Precise Extraction of Ultra Deep Submicron Interconnect Parasitics with Parameterizable 3D-Modeling
Martin R. Frerichs

Session C1
System Level Specification and Simulation
Co-chairs: Serge Vernalde, Tadatoshi Ishii

C1.1 Compiling SpecC for Simulation
Jianwen Zhu, Daniel D. Gajski

C1.2 Scalable and Flexible Cosimulation of SoC Designs with Heterogeneous Multi-Processor Target Architectures
Patrice Gerin, Sungjoo Yoo, Gabriela Nicolescu, Ahmed A. Jerraya

C1.3 A Higher Level System Communication Model for Object-Oriented Specification and Design of Embedded Systems
Kjetil Svarstad, Nezih Ben-Fredj, Gabriela Nicolescu, Ahmed A. Jerraya

C1.4 Dataflow Specification for System Level Synthesis of 3D Graphics Applications
Chanik Park, Sungchan Kim, Soonhoi Ha
Session D1  
Issues in BDD and Sequential Verification  

Co-chairs: Yirng-An Chen, Shinichi Minato  

D1.1 The Multiple Variable Order Problem for Binary Decision Diagrams: Theory and Practical Application  
Christoph Scholl, Bernd Becker, Andreas Brogle .......................... 85  

D1.2 Application of Linearly Transformed BDDs in Sequential Verification  
Wolfgang Günther, Andreas Hett, Bernd Becker ............................. 91  

D1.3 A New Partitioning Scheme for Improvement of Image Computation  
Christoph Meinel, Christian Stangier ........................................ 97  

D1.4 An Efficient Design-for-Verification Technique for HDLs  
Chien-Nan Jimmy Liu, I-Ling Chen, Jing-Yang Jou ......................... 103  

Session A2  
Interconnect Design Optimization (I)  

Co-chairs: D. F. Wong, Takumi Okamoto  

A2.1 Reducing Bus Delay in Submicron Technology Using Coding  
Paul P. Sotiriadis, Anantha Chandrakasan ..................................... 109  

A2.2 Optimal Spacing and Capacitance Padding for General Clock Structures  
Yu-Min Lee, Hing Yin Lai, Charlie Chung-Ping Chen ........................ 115  

A2.3 Provably Good Global Buffering by Multi-Terminal Multicommodity Flow Approximation  
Feodor F. Dragan, Andrew B. Kahng, Ion Măndoiu, Sudhakar Muddu, Alexander Zelikovsky ......................................................... 120  

A2.4 Construction of Minimal Delay Steiner Tree Using Two-pole Delay Model  
LiYi Lin, YiYu Liu, TingTing Hwang ........................................... 126  

Session B2  
Design for Manufacturability  

Co-chairs: Martin R. Frerichs, Mitiko Miura-Mattausch  

B2.1 New Graph Bipartizations for Double-Exposure, Bright Field Alternating Phase-Shift Mask Layout  
Andrew B. Kahng, Shailesh Vaya, Alexander Zelikovsky .................... 133
B2.2 Hierarchical Dummy Fill for Process Uniformity
Yu Chen, Andrew B. Kahng, Gabriel Robins, Alexander Zelikovsky ............. 139

B2.3 (Embedded Tutorial) Modeling and Forecasting of Manufacturing Variations
Sani R. Nassif ................................................................. 145

Session C2
System Level Design

Co-chairs: Rajesh Guputa, Yoshinori Takeuchi

Takashi Kambe, Akihisa Yamada, Koichi Nishida, Kazuhsa Okada, Mitsuhisa Ohnishi, Andrew Kay, Paul Boca, Vince Zammit, Toshio Nomura ................. 151

C2.2 Area/Delay Estimation for Digital Signal Processor Cores
Yuichiro Miyaoka, Yoshiharu Kataoka, Nozomu Togawa, Masao Yanagisawa, Tatsuo Ohtsuki ........................................................ 156

C2.3 An RTL Design-Space Exploration Method for High-Level Applications
Peng-Cheng Kao, Chih-Kuang Hsieh, Allen C.-H. Wu ................................ 162

Session D2
Important Problems in Equivalence Checking

Co-chairs: Hans Eveking, Yusuke Matsunaga

D2.1 Equivalence Checking of Integer Multipliers
Jiunn-Chern Chen, Yirng-An Chen ........................................... 169

D2.2 Addressing Verification Bottlenecks of Fully Synthesized Processor Cores Using Equivalence Checkers
Subash Chandar G, Vaideeswaran S ......................................... 175

D2.3 An Efficient Solution to the Storage Correspondence Problem for Large Sequential Circuits
Wanlin Cao, Duncan M. H. Walker, Rajarshi Mukherjee ...................... 181

Session A3
Interconnect Design Optimization (II)

Co-chairs: Charlie C.-P Chen, Ikuo Harada

A3.1 A 3-Step Approach for Performance-Driven Whole-Chip Routing
Yih-Chih Chou, Youn-Long Lin .............................................. 187

xxviii
A3.2 Efficient Minimum Spanning Tree Construction without Delaunay Triangulation
_Hai Zhou, Narendra Shenoy, William Nicholls_ ................................. 192

A3.3 Memory-Efficient Interconnect Optimization
_Minghorng Lai, D. F. Wong_ ....................................................... 198

Session B3
Parasitic Extraction and Reduced Order Model

_Co-chairs: Richard Shi, Peter M. Lee_

B3.1 Balanced Truncation with Spectral Shaping for RLC Interconnects
_Payam Heydari, Massoud Pedram_ ........................................... 203

B3.2 An Optimum Fitting Algorithm for Generation of Reduced-Order Models

B3.3 A Virtual 3-D Multipole Accelerated Extractor for VLSI Parasitic Interconnect Capacitance
_Zhaozhi Yang, Zeyi Wang, Shuzhou Fang_ .............................. 214

Session C3
Functional Decomposition and PLA-based Logic Synthesis

_Co-chairs: Rajeev Murgai, Tsutomu Sasao_

C3.1 On the Minimization of SOPs for Bi-Decomposable Functions
_Tsutomu Sasao, Jon T. Butler_ ................................................. 219

C3.2 Finding an Optimal Functional Decomposition for LUT-based FPGA Synthesis
_Jian Qiao, Makoto Ikeda, Kunihiro Asada_ ........................................ 225

C3.3s Practical Logic Synthesis for CPLDs and FPGAs with PLA-Style Logic Blocks
_Kenneth Yan_ .......................................................................... 231

C3.4s A New Technology Mapping for CPLD under Time Constraint
_Jae-Jin Kim, Hi-Seok Kim, Chi-Ho Lin_ ........................................ 235
# Session D3

**Low Power Techniques for Embedded Software**

*Co-chairs: Naehyuck Chang, Hiroaki Takada*

<table>
<thead>
<tr>
<th>D3.1</th>
<th>(Embedded Tutorial) Power Optimization and Management in Embedded Systems</th>
<th>Massoud Pedram</th>
<th>239</th>
</tr>
</thead>
<tbody>
<tr>
<td>D3.2</td>
<td>Low Power Techniques for Address Encoding and Memory Allocation</td>
<td>Wei-Chung Cheng, Massoud Pedram</td>
<td>245</td>
</tr>
<tr>
<td>D3.3s</td>
<td>Investigating the Effect of Voltage-Switching on Low-Energy Task Scheduling in Hard Real-Time Systems</td>
<td>Vishnu Swaminathan, Krishnendu Chakrabarty</td>
<td>251</td>
</tr>
</tbody>
</table>

# Session E3

**(Special Session) Asynchronous System Design: Architecture and Low-Power Design**

*Co-chairs: Dong-Ik Lee, Tomohiro Yoneda*

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>E3.2</td>
<td>Imprecise Data Computation for High Performance Asynchronous Processors</td>
<td>Jeong-Gun Lee, Eui-seok Kim, Dong-Ik Lee</td>
<td>261</td>
</tr>
</tbody>
</table>

# Session A4

**(Panel) Beyond the Red Brick Wall: Challenges and Solutions in 50nm Physical Design**

*Moderator: Hidetoshi Onodera*

*Panelists: Andrew B. Kahng, Wayne W. M. Dai, Sani R. Nassif, Juho Kim, Akira Tanabe, Toshihiro Hattori*

# Session B4

**Analog Design Methodology**

*Co-chairs: Edmund K. Cheng, Hideki Asai*

| B4.1 | A Pipelined ADC Macro Design for Multiple Applications | Kuniyuki Tani, Norihiro Nikai, Atsushi Wada, Tetsuro Sawai | 269 |
B4.2 A Dynamically Phase Adjusting PLL with a Variable Delay
Takeo Yasuda, Hiroaki Fujita, Hidetoshi Onodera .............................. 275

B4.3 Device-Level Placement for Analog Layout: An Opportunity for Non-Slicing Topological Representations
Florin Balasa ................................................................. 281

B4.4 (Embedded Tutorial) A Mixed-Signal Simulator for VHDL-AMS
Xiao Liyi, Li Bin, Ye Yizheng, Huang Guoyong, Guo Jinjun, Zhang Peng .... 287

---

Session C4
Low Power Design Methodology

Co-chairs: Masakazu Yamashina, Hiroyuki Mizuno

C4.1 (Invited Talk) Low Power Design Challenges for the Decade
Shekhar Borkar ................................................................. 293

C4.2 An On-Chip 96.5% Current Efficiency CMOS Linear Regulator
Kazuhisa Sunaga, Tetsuo Endoh, Hiroshi Sakuraba, Fujio Masuoka ........ 297

C4.3s Reducing Cache Energy Through Dual Voltage Supply
Vasily G. Moshnyaga ....................................................... 302

C4.4s Trace-driven System-level Power Evaluation of System-on-a-chip Peripheral Cores
Tony D. Givargis, Frank Vahid, Jörg Henkel .................................. 306

---

Session D4
Advanced BIST : Methodology and Applications

Co-chairs: Krishnendu Chakrabarty, Kazumi Hatayama

D4.1 (Embedded Tutorial) Towards the Logical Defect Diagnosis for Partial-Scan Designs
Shi-Yu Huang ................................................................. 313

D4.2 GF(2^p) Cellular Automata as a Built In Self Test Structure
Biplab K. Sikdar, Debesh K. Das, Vamsi Boppana, Cliff Yang, Sobhan Mukherjee, P. Pal Chaudhuri ...................................................... 319

D4.3 Processor-Programmable Memory BIST for Bus-Connected Embedded Memories
Ching-Hong Tsai, Cheng-Wen Wu ........................................... 325

D4.4s A DFT Method for RTL Circuits to Achieve Complete Fault Efficiency Based on Fixed-control Testability
Satoshi Ohtake, Shintaro Nagai, Hiroki Wada, Hideo Fujiwara .............. 331
Session E4
(Special Session) Asynchronous System Design: Verification

Co-chairs: Joep Kessels, Takashi Nanya

E4.1 (Embedded Tutorial) Timed Circuits: A New Paradigm for High-Speed Design

E4.2 Conformance and Mirroring for Timed Asynchronous Circuits
Bin Zhou, Tomohiro Yoneda, Bernd-Holger Schlingloff

E4.3 Formal Verification of Pulse-Mode Circuits
Xiaohua Kong, Radu Negulescu

Session A5
DSM Design and Analysis

Co-chairs: Andrew B. Kahng, Toshiro Akino

A5.1 A Statistical Static Timing Analysis Considering Correlations Between Delays
Shuji Tsukiyama, Masakazu Tanaka, Masahiro Fukui

A5.2 Post-Layout Transistor Sizing for Power Reduction in Cell-Based Design
Masanori Hashimoto, Hidetoshi Onodera

A5.3 An Efficient Quasi-Multiple Medium Algorithm for the Capacitance Extraction of Actual 3-D VLSI Interconnects
Wenjian Yu, Zeyi Wang

Session B5
Signal Integrity and Analysis

Co-chairs: David Overhauser, Kimihiro Ogawa

B5.1 Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization
Jason Cong, David Zhigang Pan, Prasanna V. Srinivas

B5.2 KSim: A Stable and Efficient RKC Simulator for Capturing On-Chip Inductance Effect
Hao Ji, Anirudh Devgan, Wayne Dai

B5.3 An Efficient Analytical Model of Coupled On-chip RLC Interconnects
Liang Yin, Lei He
Session C5
Design Experiments for Mobile Applications

Co-chairs: Shekhar Borkar, Satoshi Matsushita

C5.1 RSA Cryptosystem Design Based on the Chinese Remainder Theorem
Chung-Hsien Wu, Jin-Hua Hong, Cheng-Wen Wu ........................................... 391

C5.2 Speech Recognition Chip for Monosyllables
Kazuhiro Nakamura, Qiang Zhu, Shinji Maruoka, Takashi Horiyama, Shinji Kimura, Katsumasa Watanabe ................................................................. 396

C5.3 Low Power Implementation of a Turbo-Decoder on Programmable Architectures
Frank Gilbert, Alexander Worm, Norbert Wehn .............................................. 400

C5.4 Area-Efficient and Reusable VLSI Architecture of Decision Feedback Equalizer for QAM Modem
Hyeongseok Yu, Byung Wook Kim, Yeon Gon Cho, Jun Dong Cho, Jea Woo Kim, Jae Kon Lee, Hyun Chul Park, Ki Won Lee ................................................. 404

Session D5
Compilation Techniques for Embedded Software

Co-chairs: Pai H. Chou, Shigeki Nankaku

D5.1 (Embedded Tutorial) New Directions in Compiler Technology for Embedded Systems
Nikil Dutt, Alex Nicolau, Hiroyuki Tomiyama, Ashok Halambi ......................... 409

D5.2 Optimized Address Assignment for DSPs with SIMD Memory Accesses
Markus Lorenz, David Kottmann, Steven Bashford, Rainer Leupers, Peter Marwedel ................................................................. 415

D5.3 A Formal Approach to Component Based Development of Synchronous Programs
Partha S. Roop, A. Sowmya, S. Ramesh .......................................................... 421

Session E5
(Special Session) Asynchronous System Design: Synthesis

Co-chairs: Chris J. Myers, Yoichiro Sato

E5.1 Synthesis of Four-Phase Asynchronous Control Circuits from Pipeline Dependency Graphs
Hiroto Kagotani, Takuji Okamoto, Takashi Nanya ......................................... 425
E5.2 **High-Level Design for Asynchronous Logic**  
*Ross Smith, Michiel Ligthart* ............................................ 431

E5.3 **Eliminating Isochronic-Fork Constraints in Quasi-Delay-Insensitive Circuits**  
*Nattha Sretasereekul, Takashi Nanya* ............................................ 437

**Session A6**  
**Design Technology Productivity in the DSM Era**

*Co-chairs: Xianlong Hong, M. Edahiro*

A6.1 **(Invited Talk) Design Technology Productivity in the DSM Era**  
*Andrew B. Kahng* .................................................. 443

**Session B6**  
**System Level Power Optimization**

*Co-chairs: Massoud Pedram, Toshinori Sato*

B6.1 **LEneS: Task Scheduling for Low-Energy Systems Using Variable Supply Voltage Processors**  
*Flavius Gruian, Krzysztof Kuchcinski* ............................................ 449

B6.2 **A System Level Memory Power Optimization Technique Using Multiple Supply and Threshold Voltages**  
*Tohru Ishihara, Kunihiro Asada* ............................................ 456

B6.3 **Low-Power High-Level Synthesis Using Latches**  
*Wooseung Yang, In-Cheol Park, Chong-Min Kyung* .......................... 462

**Session C6**  
**Multi-level Logic Optimization for Logic Circuits**

*Co-chairs: Shi-Yu Huang, Hiroshi Sawada*

C6.1 **Functional Extension of Structural Logic Optimization Techniques**  
*J. A. Espejo, L. Entrena, E. San Millán, E. Oliás* ...................... 467

C6.2 **Improved Alternative Wiring Scheme Applying Dominator Relationship**  
*Chin-Ngai Sze, Yu-Liang Wu* ............................................ 473

C6.3 **Design Rewiring Based on Diagnosis Techniques**  
*Andreas Veneris, Magdy S. Abadir, Ivor Ting* .................................. 479
## Session D6
### Practical and High Level DFT

**Co-chairs:** Cheng-Wen Wu, Tomoo Inoue

**D6.1** Design for Testability Strategies Using Full/Partial Scan Designs and Test Point Insertions to Reduce Test Application Times  
*Toshinori Hosokawa, Masayoshi Yoshimura, Mitsuyasu Ohta* ........................................ 485

**D6.2** A Computer Aided Engineering System for Memory BIST  
*Chauchin Su, Shih-Ching Hsiao, Hau-Zen Zhu, Chung-Len Lee* ................. 492

**D6.3** Synthesis of Single-Output Space Compactors with Application to Scan-based IP cores  
*Bhargab B. Bhattacharya, Alexej Dmitriev, Michael Gössel, Krishnendu Chakrabarty* ........................................................ 496

## Session A7
### Performance Driven Floorplanning and Placement (I)

**Co-chairs:** Wayne W. M. Dai, Hiroshi Murata

**A7.1** Slicing Floorplan with Clustering Constraints  
*Wing Seung Yuen, Fung Yu Young* ..................................................... 503

**A7.2** VLSI Floorplanning with Boundary Constraints Based on Corner Block List  
*Yuchun Ma, Sheqin Dong, Xianlong Hong, Yici Cai, Chung-Kuan Cheng, Jun Gu* 509

**A7.3** Module Placement with Boundary Constraints Using the Sequence-Pair Representation  
*Jianbang Lai, Ming-Shiun Lin, Ting-Chi Wang, Li-C. Wang* ................... 515

**A7.4** FAST-SP: A Fast Algorithm for Block Placement Based on Sequence Pair  
*Xiaoping Tang, D. F. Wong* .......................................................... 521

## Session B7
### Improving Delay and Power Estimation

**Co-chairs:** Wolfgang Roething, Hidetoshi Onodera

**B7.1** Toward Better Wireload Models in the Presence of Obstacles  
*Chung-Kuan Cheng, Andrew B. Kahng, Bao Liu, Dirk Stroobandt* .............. 527
B7.2 A Fast and Accurate Delay Estimation Method for Buffered Interconnects
Youxin Gao, D. F. Wong ...................................................... 533

B7.3 On-Chip Interconnections: Impact of Adjacent Lines on Timing
D. Deschacht, G. Servel ..................................................... 539

B7.4 Short Circuit Power Estimation of Static CMOS Circuits
Seung-Ho Jung, Jong-Hunn Baek, Seok-Yoon Kim .......................... 545

Session C7
Networked Reconfiguration and Systems
Co-chairs: Allen C.-H. Wu, Toshiaki Miyazaki

C7.1 A Novel Network Node Architecture for High Performance and Function
Flexibility
Takahiro Murooka, Atsushi Takahara, Toshiaki Miyazaki .................... 551

C7.2 Virtual Java/FPGA Interface for Networked Reconfiguration
Yajun Ha, Geert Vanmeerceek, Patrick Schaumont, Serge Vernalde, Marc Engels, Rudy Lauwereins, Hugo De Man .......................... 558

C7.3 (Embedded Tutorial) Coarse Grain Reconfigurable Architecture
Reiner Hartenstein .......................................................... 564

Session D7
Advances in Timing Optimization of Logic Circuits
Chair: Yutaka Tamiya

D7.1 Efficient Global Fanout Optimization Algorithms
Rajeev Murgai ............................................................... 571

D7.2 Timing Driven Gate Duplication in Technology Independent Phase
Ankur Srivastava, Chunhong Chen, Majid Sarrafzadeh ....................... 577

D7.3 On Speeding Up Extended Finite State Machines Using Catalyst Circuitry
Shi-Yu Huang ............................................................... 583

Session A8
Performance Driven Floorplanning and Placement (II)
Co-chairs: Tetsushi Koide, Tomonori Izumi

A8.1 Integrated Power Supply Planning and Floorplanning
I-Min Liu, Hung-Ming Chen, Tan-Li Chou, Adnan Aziz, D. F. Wong .......... 589

xxxvi
A8.2 Post-Layout Timing-Driven Cell Placement Using An Accurate Net Length Model with Movable Steiner Points
Amir H. Ajami, Massoud Pedram ........................................ 595

A8.3s VLSI Block Placement Using Less Flexibility First Principles
Sheqin Dong, Xianlong Hong, Youliang Wu, Yizhou Lin, Jun Gu .. 601

A8.4s A New Congestion-Driven Placement Algorithm Based on Cell Inflation
Wenting Hou, Hong Yu, Xianlong Hong, Yici Cai, Weimin Wu, Jun Gu, William H. Kao . .................... 605

Session B8
Logic Synthesis for Low Power and Design Space Exploration

Co-chairs: Supratik Chakraborty, Makoto Ikeda

B8.1 Cell Selection from Technology Libraries for Minimizing Power
Yumin Zhang, Xiaobo Sharon Hu, Danny Z. Chen ....................... 609

B8.2 Low Power Optimization Technique for BDD Mapped Circuits
Per Lindgren, Mikael Kerttu, Mitch Thornton, Rolf Drechsler ........ 615

B8.3 Accurate Exploration of Timing and Area Trade-offs in Arithmetic Optimization Using Carry-Save-Adders
Youngtae Kim, Taewhan Kim ................................................. 622

Session C8
Optimization Technique for FPGAs

Co-chairs: Reiner Hartenstein, Tetsuo Hironaka

C8.1 RPack: Routability-Driven Packing for Cluster-Based FPGAs
Elaheh Bozorgzadeh, Seda Ogrenci-Memik, Majid Sarrafzadeh . .... 629

C8.2 Power Minimization in LUT-Based FPGA Technology Mapping
Zhi-Hong Wang, En-Cheng Liu, Jianbang Lai, Ting-Chi Wang .......... 635

C8.3s Combinatorial Routing Analysis and Design of Universal Switch Blocks
Hongbing Fan, Jiping Liu, Yu-Liang Wu . ..................................... 641

C8.4s Automated Synthesis of Pipelined Designs on FPGAs for Signal and Image Processing Applications Described in MATLAB
Malay Haldar, Anshuman Nayak, Alok Choudhary, Prith Banerjee . .. 645
Session D8
Processor Synthesis

Co-chairs: Allen C.-H. Wu, Nagisa Ishiura

D8.1 **Effectiveness of the ASIP Design System PEAS-III in Design of Pipelined Processors**  
Akira Kitajima, Makiko Itoh, Jun Sato, Akichika Shiomi, Yoshinori Takeuchi, Masaharu Imai ................................................................. 649

D8.2 **High-Level Specification and Efficient Implementation of Pipelined Circuits**  
Maria-Cristina Marinescu, Martin Rinard ........................................ 655

D8.3 **High-Level Synthesis Under Multi-Cycle Interconnect Delay**  
Jinhwan Jeon, Daehong Kim, Dongwan Shin, Kiyoungh Choi ............. 662
## Author Index

### A

<table>
<thead>
<tr>
<th>Name</th>
<th>Page Numbers</th>
<th>Page Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abadir, Magdy S.</td>
<td>(C6.3) 479</td>
<td>(C6.3) 479</td>
</tr>
<tr>
<td>Ajami, Amir H.</td>
<td>(A8.2) 595</td>
<td>(A8.2) 595</td>
</tr>
<tr>
<td>Amano, Hideharu</td>
<td>(A1.9) 17</td>
<td>(A1.9) 17</td>
</tr>
<tr>
<td>Andales, Zaldy</td>
<td>(A1.6) 11</td>
<td>(A1.6) 11</td>
</tr>
<tr>
<td>Arai, Yasuo</td>
<td>(A1.3) 5</td>
<td>(A1.3) 5</td>
</tr>
<tr>
<td>Asada, Kunihiro</td>
<td>(A1.2) 3</td>
<td>(A1.11) 21</td>
</tr>
<tr>
<td></td>
<td>(C3.2) 225</td>
<td>(B6.2) 456</td>
</tr>
<tr>
<td>Aziz, Adnan</td>
<td>(A8.1) 589</td>
<td>(A8.1) 589</td>
</tr>
</tbody>
</table>

### B

<table>
<thead>
<tr>
<th>Name</th>
<th>Page Numbers</th>
<th>Page Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baek, Jong-Humun</td>
<td>(B7.4) 545</td>
<td>(B7.4) 545</td>
</tr>
<tr>
<td>Balasa, Florin</td>
<td>(B4.3) 281</td>
<td>(B4.3) 281</td>
</tr>
<tr>
<td>Banerjee, Prith</td>
<td>(C8.4s) 645</td>
<td>(C8.4s) 645</td>
</tr>
<tr>
<td>Bashford, Steven</td>
<td>(D5.2) 415</td>
<td>(D5.2) 415</td>
</tr>
<tr>
<td>Becker, Bernd</td>
<td>(D1.1) 85</td>
<td>(D1.2) 91</td>
</tr>
<tr>
<td>Belluomini, Wendy</td>
<td>(E4.1) 335</td>
<td>(E4.1) 335</td>
</tr>
<tr>
<td>Ben-Fredj, Nezih</td>
<td>(C1.3) 69</td>
<td>(C1.3) 69</td>
</tr>
<tr>
<td>Bhattacharya, Bhargab B.</td>
<td>(D6.3) 496</td>
<td>(D6.3) 496</td>
</tr>
<tr>
<td>Bin, Li</td>
<td>(B4.4) 287</td>
<td>(B4.4) 287</td>
</tr>
<tr>
<td>Boca, Paul</td>
<td>(C2.1) 151</td>
<td>(C2.1) 151</td>
</tr>
<tr>
<td>Boppana, Vamsi</td>
<td>(D4.2) 319</td>
<td>(D4.2) 319</td>
</tr>
<tr>
<td>Borkar, Shekhar</td>
<td>(C4.1) 293</td>
<td>(C4.1) 293</td>
</tr>
<tr>
<td>Bozorgzadeh, Elaheh</td>
<td>(C8.1) 629</td>
<td>(C8.1) 629</td>
</tr>
<tr>
<td>Brogle, Andreas</td>
<td>(D1.1) 85</td>
<td>(D1.1) 85</td>
</tr>
<tr>
<td>Butler, Jon T.</td>
<td>(C3.1) 219</td>
<td>(C3.1) 219</td>
</tr>
</tbody>
</table>

### C

<table>
<thead>
<tr>
<th>Name</th>
<th>Page Numbers</th>
<th>Page Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cai, Yici</td>
<td>(A7.2) 509</td>
<td>(A7.2) 509</td>
</tr>
<tr>
<td></td>
<td>(A8.4s) 605</td>
<td>(A8.4s) 605</td>
</tr>
<tr>
<td>Cao, Wanlin</td>
<td>(D2.3) 181</td>
<td>(D2.3) 181</td>
</tr>
<tr>
<td>Chae, Soo-Ik</td>
<td>(A1.14) 27</td>
<td>(A1.14) 27</td>
</tr>
</tbody>
</table>

### D

<table>
<thead>
<tr>
<th>Name</th>
<th>Page Numbers</th>
<th>Page Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chakrabarty, Krishnendu</td>
<td>(D3.3s) 251</td>
<td>(D3.3s) 251</td>
</tr>
<tr>
<td></td>
<td>(D6.3) 496</td>
<td>(D6.3) 496</td>
</tr>
<tr>
<td>Chandrakasan, Anantha</td>
<td>(A2.1) 109</td>
<td>(A2.1) 109</td>
</tr>
<tr>
<td>Chang, Hao-Chieh</td>
<td>(A1.15) 29</td>
<td>(A1.15) 29</td>
</tr>
<tr>
<td>Chang, Yung-Chi</td>
<td>(A1.15) 29</td>
<td>(A1.15) 29</td>
</tr>
<tr>
<td>Chaudhuri, P. Pal</td>
<td>(D4.2) 319</td>
<td>(D4.2) 319</td>
</tr>
<tr>
<td>Chen, Charlie Chung-Ping</td>
<td>(A2.2) 115</td>
<td>(A2.2) 115</td>
</tr>
<tr>
<td>Chen, Chung-Ho</td>
<td>(A1.12) 23</td>
<td>(A1.12) 23</td>
</tr>
<tr>
<td>Chen, Chunhong</td>
<td>(D7.2) 577</td>
<td>(D7.2) 577</td>
</tr>
<tr>
<td>Chen, Danny Z.</td>
<td>(B8.1) 609</td>
<td>(B8.1) 609</td>
</tr>
<tr>
<td>Chen, Hung-Ming</td>
<td>(A8.1) 589</td>
<td>(A8.1) 589</td>
</tr>
<tr>
<td>Chen, I-Ling</td>
<td>(D1.4) 103</td>
<td>(D1.4) 103</td>
</tr>
<tr>
<td>Chen, Jiunn-Chern</td>
<td>(D2.1) 169</td>
<td>(D2.1) 169</td>
</tr>
<tr>
<td>Chen, Liang-Gee</td>
<td>(A1.15) 29</td>
<td>(A1.15) 29</td>
</tr>
<tr>
<td>Chen, Ming-Chih</td>
<td>(A1.12) 23</td>
<td>(A1.12) 23</td>
</tr>
<tr>
<td>Chen, Yirng-An</td>
<td>(D2.1) 169</td>
<td>(D2.1) 169</td>
</tr>
<tr>
<td>Cheng, Yu</td>
<td>(B2.2) 139</td>
<td>(B2.2) 139</td>
</tr>
<tr>
<td>Cheng, Chung-Kuan</td>
<td>(A7.2) 509</td>
<td>(A7.2) 509</td>
</tr>
<tr>
<td></td>
<td>(B7.1) 527</td>
<td>(B7.1) 527</td>
</tr>
<tr>
<td>Cho, Jun Dong</td>
<td>(C5.4s) 404</td>
<td>(C5.4s) 404</td>
</tr>
<tr>
<td>Cho, Yeon Gon</td>
<td>(C5.4s) 404</td>
<td>(C5.4s) 404</td>
</tr>
<tr>
<td>Choi, Kiyoun</td>
<td>(D8.3) 662</td>
<td>(D8.3) 662</td>
</tr>
<tr>
<td>Chou, Tan-Li</td>
<td>(A8.1) 589</td>
<td>(A8.1) 589</td>
</tr>
<tr>
<td>Chou, Yih-Chih</td>
<td>(A3.1) 187</td>
<td>(A3.1) 187</td>
</tr>
<tr>
<td>Choudhary, Alok</td>
<td>(C8.4s) 645</td>
<td>(C8.4s) 645</td>
</tr>
<tr>
<td>Cong, Jason</td>
<td>(B5.1) 373</td>
<td>(B5.1) 373</td>
</tr>
</tbody>
</table>

### D

<table>
<thead>
<tr>
<th>Name</th>
<th>Page Numbers</th>
<th>Page Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dai, Wayne</td>
<td>(B5.2) 379</td>
<td>(B5.2) 379</td>
</tr>
<tr>
<td>Das, Debes K.</td>
<td>(D4.2) 319</td>
<td>(D4.2) 319</td>
</tr>
<tr>
<td>Deschacht, D.</td>
<td>(B7.3) 539</td>
<td>(B7.3) 539</td>
</tr>
<tr>
<td>Devgan, Anirudh</td>
<td>(B5.2) 379</td>
<td>(B5.2) 379</td>
</tr>
<tr>
<td>Dmitriev, Alexej</td>
<td>(D6.3) 496</td>
<td>(D6.3) 496</td>
</tr>
<tr>
<td>Dong, Sheqin</td>
<td>(A7.2) 509</td>
<td>(A7.2) 509</td>
</tr>
<tr>
<td></td>
<td>(A8.3s) 601</td>
<td>(A8.3s) 601</td>
</tr>
<tr>
<td>Dong, Yu</td>
<td>(A1.8) 15</td>
<td>(A1.8) 15</td>
</tr>
<tr>
<td>Name</td>
<td>Page</td>
<td></td>
</tr>
<tr>
<td>-------------------------------</td>
<td>------</td>
<td></td>
</tr>
<tr>
<td>Dragan, Feodor F.</td>
<td>(A2.3) 120</td>
<td></td>
</tr>
<tr>
<td>Drechsler, Rolf</td>
<td>(B8.2) 615</td>
<td></td>
</tr>
<tr>
<td>Dutt, Nikil</td>
<td>(D5.1) 409</td>
<td></td>
</tr>
<tr>
<td>Eguchi, Makoto</td>
<td>(A1.1) 1</td>
<td></td>
</tr>
<tr>
<td>Endoh, Tetsuo</td>
<td>(C4.2) 297</td>
<td></td>
</tr>
<tr>
<td>Engels, Marc</td>
<td>(C7.2) 558</td>
<td></td>
</tr>
<tr>
<td>Entrena, L.</td>
<td>(C6.1) 467</td>
<td></td>
</tr>
<tr>
<td>Espejo, J. A.</td>
<td>(C6.1) 467</td>
<td></td>
</tr>
<tr>
<td>Fan, Hongbing</td>
<td>(C8.3s) 641</td>
<td></td>
</tr>
<tr>
<td>Fang, Shuzhou</td>
<td>(B3.3) 214</td>
<td></td>
</tr>
<tr>
<td>Frerichs, Martin R.</td>
<td>(B1.3) 50</td>
<td></td>
</tr>
<tr>
<td>Fujibayashi, Masanori</td>
<td>(A1.13) 25</td>
<td></td>
</tr>
<tr>
<td>Fujita, Gen</td>
<td>(A1.8) 15</td>
<td></td>
</tr>
<tr>
<td>Fujita, Hiroaki</td>
<td>(B4.2) 275</td>
<td></td>
</tr>
<tr>
<td>Fujiwara, Hideo</td>
<td>(D4.4s) 331</td>
<td></td>
</tr>
<tr>
<td>Fukui, Masahiro</td>
<td>(A5.1) 353</td>
<td></td>
</tr>
<tr>
<td>Furue, Makoto</td>
<td>(A1.8) 15</td>
<td></td>
</tr>
<tr>
<td>G, Subash Chandar</td>
<td>(D2.2) 175</td>
<td></td>
</tr>
<tr>
<td>Gajski, Daniel D.</td>
<td>(C1.1) 57</td>
<td></td>
</tr>
<tr>
<td>Gao, Youxin</td>
<td>(B7.2) 533</td>
<td></td>
</tr>
<tr>
<td>Gerin, Patrice</td>
<td>(C1.2) 63</td>
<td></td>
</tr>
<tr>
<td>Gilbert, Frank</td>
<td>(C5.3s) 400</td>
<td></td>
</tr>
<tr>
<td>Givargis, Tony D.</td>
<td>(C4.4s) 306</td>
<td></td>
</tr>
<tr>
<td>Gössel, Michael</td>
<td>(D6.3) 496</td>
<td></td>
</tr>
<tr>
<td>Gourary, M. M.</td>
<td>(B3.2) 209</td>
<td></td>
</tr>
<tr>
<td>Gruian, Flavius</td>
<td>(B6.1) 449</td>
<td></td>
</tr>
<tr>
<td>Gu, Jun</td>
<td>(A7.2) 509</td>
<td></td>
</tr>
<tr>
<td>(A8.3s) 601</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(A8.4s) 605</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Günther, Wolfgang</td>
<td>(D1.2) 91</td>
<td></td>
</tr>
<tr>
<td>Guoyong, Huang</td>
<td>(B4.4) 287</td>
<td></td>
</tr>
<tr>
<td>Ha, Soonhoi</td>
<td>(C1.4) 78</td>
<td></td>
</tr>
<tr>
<td>Ha, Yajun</td>
<td>(C7.2) 558</td>
<td></td>
</tr>
<tr>
<td>Halambi, Ashok</td>
<td>(D5.1) 409</td>
<td></td>
</tr>
<tr>
<td>Haldar, Malay</td>
<td>(C8.4s) 645</td>
<td></td>
</tr>
<tr>
<td>Han, Seon-Ho</td>
<td>(A1.5) 9</td>
<td></td>
</tr>
<tr>
<td>Harstenstein, Reiner</td>
<td>(C7.3) 564</td>
<td></td>
</tr>
<tr>
<td>Hashimoto, Koji</td>
<td>(A1.19) 37</td>
<td></td>
</tr>
<tr>
<td>Hashimoto, Masanori</td>
<td>(A5.2) 359</td>
<td></td>
</tr>
<tr>
<td>He, Lei</td>
<td>(B5.3) 385</td>
<td></td>
</tr>
<tr>
<td>Henkel, Jörg</td>
<td>(C4.4s) 306</td>
<td></td>
</tr>
<tr>
<td>Hett, Andreas</td>
<td>(D1.2) 91</td>
<td></td>
</tr>
<tr>
<td>Heydari, Payam</td>
<td>(B3.1) 203</td>
<td></td>
</tr>
<tr>
<td>Hong, Jin-Hua</td>
<td>(C5.1) 391</td>
<td></td>
</tr>
<tr>
<td>Hong, Xianlong</td>
<td>(A7.2) 509</td>
<td></td>
</tr>
<tr>
<td>(A8.3s) 601</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(A8.4s) 605</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Horiyama, Takashi</td>
<td>(A1.16) 31</td>
<td></td>
</tr>
<tr>
<td>(C5.2s) 396</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hoshino, Masashi</td>
<td>(A1.11) 21</td>
<td></td>
</tr>
<tr>
<td>Hosokawa, Toshinori</td>
<td>(D6.1) 485</td>
<td></td>
</tr>
<tr>
<td>Hou, Wenting</td>
<td>(A8.4s) 605</td>
<td></td>
</tr>
<tr>
<td>Hsiao, Shih-Ching</td>
<td>(D6.2) 492</td>
<td></td>
</tr>
<tr>
<td>Hsieh, Chih-Kuang</td>
<td>(C2.3) 162</td>
<td></td>
</tr>
<tr>
<td>Hu, Xiaobo Sharon</td>
<td>(B8.1) 609</td>
<td></td>
</tr>
<tr>
<td>Huang, Ing-Jer</td>
<td>(A1.12) 23</td>
<td></td>
</tr>
<tr>
<td>(A1.17) 33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Huang, Shi-Yu</td>
<td>(D4.1) 313</td>
<td></td>
</tr>
<tr>
<td>(D7.3) 583</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hwang, TingTing</td>
<td>(A2.4) 126</td>
<td></td>
</tr>
<tr>
<td>Ikeda, Makoto</td>
<td>(A1.2) 3</td>
<td></td>
</tr>
<tr>
<td>(A1.11) 21</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C3.2) 225</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Imai, Makoto</td>
<td>(A1.13) 25</td>
<td></td>
</tr>
<tr>
<td>Imai, Masaharu</td>
<td>(D8.1) 649</td>
<td></td>
</tr>
<tr>
<td>Ishihara, Toshiro</td>
<td>(B6.2) 456</td>
<td></td>
</tr>
<tr>
<td>Itoh, Makiko</td>
<td>(D8.1) 649</td>
<td></td>
</tr>
<tr>
<td>Iwashashi, Takuya</td>
<td>(A1.1) 1</td>
<td></td>
</tr>
<tr>
<td>Name</td>
<td>Page Numbers</td>
<td>Page Numbers</td>
</tr>
<tr>
<td>-----------------------</td>
<td>--------------</td>
<td>--------------</td>
</tr>
<tr>
<td>Iwata, Atsushi</td>
<td>(A1.7)</td>
<td>13</td>
</tr>
<tr>
<td>Jeon, Jinhwan</td>
<td>(D8.3)</td>
<td>662</td>
</tr>
<tr>
<td>Jerraya, Ahmed A.</td>
<td>(C1.2)</td>
<td>63</td>
</tr>
<tr>
<td></td>
<td>(C1.3)</td>
<td>69</td>
</tr>
<tr>
<td>Ji, Hao</td>
<td>(B5.2)</td>
<td>379</td>
</tr>
<tr>
<td>Jinjun, Guo</td>
<td>(B4.4)</td>
<td>287</td>
</tr>
<tr>
<td>Jou, Jing-Yang</td>
<td>(D1.4)</td>
<td>103</td>
</tr>
<tr>
<td>Jung, Seung-Ho</td>
<td>(B7.4)</td>
<td>545</td>
</tr>
<tr>
<td>Kagotani, Hiroto</td>
<td>(E5.1)</td>
<td>425</td>
</tr>
<tr>
<td>Kahng, Andrew B.</td>
<td>(A2.3)</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td>(B2.1)</td>
<td>133</td>
</tr>
<tr>
<td></td>
<td>(B2.2)</td>
<td>139</td>
</tr>
<tr>
<td></td>
<td>(A6.1)</td>
<td>443</td>
</tr>
<tr>
<td></td>
<td>(B7.1)</td>
<td>527</td>
</tr>
<tr>
<td>Kambe, Takashi</td>
<td>(C2.1)</td>
<td>151</td>
</tr>
<tr>
<td>Kao, Chung-Fu</td>
<td>(A1.17)</td>
<td>33</td>
</tr>
<tr>
<td>Kao, William H.</td>
<td>(A8.4s)</td>
<td>605</td>
</tr>
<tr>
<td>Kataoka, Yoshiharu</td>
<td>(C2.2)</td>
<td>156</td>
</tr>
<tr>
<td>Kawakami, Daisuke</td>
<td>(A1.9)</td>
<td>17</td>
</tr>
<tr>
<td>Kay, Andrew</td>
<td>(C2.1)</td>
<td>151</td>
</tr>
<tr>
<td>Kerttu, Mikael</td>
<td>(B8.2)</td>
<td>615</td>
</tr>
<tr>
<td>Kessels, Joep</td>
<td>(E3.1)</td>
<td>255</td>
</tr>
<tr>
<td>Ki, Wing-Hung</td>
<td>(A1.10)</td>
<td>19</td>
</tr>
<tr>
<td>Killpack, Kip</td>
<td>(E4.1)</td>
<td>335</td>
</tr>
<tr>
<td>Kim, Byung Wook</td>
<td>(C5.4s)</td>
<td>404</td>
</tr>
<tr>
<td>Kim, Daehong</td>
<td>(D8.3)</td>
<td>662</td>
</tr>
<tr>
<td>Kim, Euisook</td>
<td>(E3.2)</td>
<td>261</td>
</tr>
<tr>
<td>Kim, Hi-Seok</td>
<td>(C3.4s)</td>
<td>235</td>
</tr>
<tr>
<td>Kim, Jae-Jin</td>
<td>(C3.4s)</td>
<td>235</td>
</tr>
<tr>
<td>Kim, Jea Woo</td>
<td>(C5.4s)</td>
<td>404</td>
</tr>
<tr>
<td>Kim, Seok-Yoon</td>
<td>(B7.4)</td>
<td>545</td>
</tr>
<tr>
<td>Kim, Seokkee</td>
<td>(A1.14)</td>
<td>27</td>
</tr>
<tr>
<td>Kim, Sungchan</td>
<td>(C1.4)</td>
<td>78</td>
</tr>
<tr>
<td>Kim, Taehwan</td>
<td>(B8.3)</td>
<td>622</td>
</tr>
<tr>
<td>Kim, Youngtae</td>
<td>(B8.3)</td>
<td>622</td>
</tr>
<tr>
<td>Kimura, Shinji</td>
<td>(A1.16)</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>(C5.2s)</td>
<td>396</td>
</tr>
<tr>
<td>Kitajima, Akira</td>
<td>(D8.1)</td>
<td>649</td>
</tr>
<tr>
<td>Kobayashi, Kazutoshi</td>
<td>(A1.1)</td>
<td>1</td>
</tr>
<tr>
<td>Kong, Xiaohua</td>
<td>(E4.3)</td>
<td>347</td>
</tr>
<tr>
<td>Kottmann, David</td>
<td>(D5.2)</td>
<td>415</td>
</tr>
<tr>
<td>Kuchcinski, Krzysztof</td>
<td>(B6.1)</td>
<td>449</td>
</tr>
<tr>
<td>Kumashiro, S.</td>
<td>(B1.1)</td>
<td>39</td>
</tr>
<tr>
<td>Kwon, Jun-Ho</td>
<td>(A1.14)</td>
<td>27</td>
</tr>
<tr>
<td>Kyung, Chong-Min</td>
<td>(B6.3)</td>
<td>462</td>
</tr>
<tr>
<td>Lai, Hing Yin</td>
<td>(A2.2)</td>
<td>115</td>
</tr>
<tr>
<td>Lai, Jianbang</td>
<td>(A7.3)</td>
<td>515</td>
</tr>
<tr>
<td></td>
<td>(C8.2)</td>
<td>635</td>
</tr>
<tr>
<td>Lai, Minghong</td>
<td>(A3.3)</td>
<td>198</td>
</tr>
<tr>
<td>Lauwereins, Rudy</td>
<td>(C7.2)</td>
<td>558</td>
</tr>
<tr>
<td>Lee, Chung-Len</td>
<td>(D6.2)</td>
<td>492</td>
</tr>
<tr>
<td>Lee, Dong-Ik</td>
<td>(E3.2)</td>
<td>261</td>
</tr>
<tr>
<td>Lee, Jae-Kon</td>
<td>(C5.4s)</td>
<td>404</td>
</tr>
<tr>
<td>Lee, Jeong-Gun</td>
<td>(E3.2)</td>
<td>261</td>
</tr>
<tr>
<td>Lee, Ki Won</td>
<td>(C5.4s)</td>
<td>404</td>
</tr>
<tr>
<td>Lee, Yu-Min</td>
<td>(A2.2)</td>
<td>115</td>
</tr>
<tr>
<td>Leupers, Rainer</td>
<td>(D5.2)</td>
<td>415</td>
</tr>
<tr>
<td>Li, Xiang</td>
<td>(A1.1)</td>
<td>1</td>
</tr>
<tr>
<td>Li, Zhao</td>
<td>(B1.2)</td>
<td>45</td>
</tr>
<tr>
<td>Lian, Chung-Jr</td>
<td>(A1.15)</td>
<td>29</td>
</tr>
<tr>
<td>Ligthart, Michiel</td>
<td>(E5.2)</td>
<td>431</td>
</tr>
<tr>
<td>Lin, Chi-Ho</td>
<td>(C3.4s)</td>
<td>235</td>
</tr>
<tr>
<td>Lin, LiYi</td>
<td>(A2.4)</td>
<td>126</td>
</tr>
<tr>
<td>Lin, Ming-Shiu</td>
<td>(A7.3)</td>
<td>515</td>
</tr>
<tr>
<td>Lin, Yizhou</td>
<td>(A8.3s)</td>
<td>601</td>
</tr>
<tr>
<td>Lin, Youn-Long</td>
<td>(A3.1)</td>
<td>187</td>
</tr>
<tr>
<td>Lindgren, Per</td>
<td>(B8.2)</td>
<td>615</td>
</tr>
<tr>
<td>Liu, Bao</td>
<td>(B7.1)</td>
<td>527</td>
</tr>
<tr>
<td>Liu, Chien-Nan Jimmy</td>
<td>(D1.4)</td>
<td>103</td>
</tr>
<tr>
<td>Liu, En-Cheng</td>
<td>(C8.2)</td>
<td>635</td>
</tr>
<tr>
<td>Liu, I-Min</td>
<td>(A8.1)</td>
<td>589</td>
</tr>
<tr>
<td>Liu, Jiping</td>
<td>(C8.3s)</td>
<td>641</td>
</tr>
<tr>
<td>Liu, YiYu</td>
<td>(A2.4)</td>
<td>126</td>
</tr>
<tr>
<td>Lorenz, Markus</td>
<td>(D5.2)</td>
<td>415</td>
</tr>
<tr>
<td>Name</td>
<td>Page Numbers</td>
<td></td>
</tr>
<tr>
<td>-----------------------------</td>
<td>--------------</td>
<td></td>
</tr>
<tr>
<td>Ma, Dongsheng</td>
<td>A1.10: 19</td>
<td></td>
</tr>
<tr>
<td>Ma, Yuchun</td>
<td>A7.2: 509</td>
<td></td>
</tr>
<tr>
<td>Man, Hugo De</td>
<td>C7.2: 558</td>
<td></td>
</tr>
<tr>
<td>Mándoiu, Ion</td>
<td>A2.3: 120</td>
<td></td>
</tr>
<tr>
<td>Marinescu, Maria-Cristina</td>
<td>D8.2: 655</td>
<td></td>
</tr>
<tr>
<td>Maruoka, Shinji</td>
<td>A1.16: 31</td>
<td></td>
</tr>
<tr>
<td>Marwedel, Peter</td>
<td>D5.2: 415</td>
<td></td>
</tr>
<tr>
<td>Masuoka, Fujio</td>
<td>C4.2: 297</td>
<td></td>
</tr>
<tr>
<td>Matsumoto, S.</td>
<td>B1.1: 39</td>
<td></td>
</tr>
<tr>
<td>Mattausch, H. J.</td>
<td>B1.1: 39</td>
<td></td>
</tr>
<tr>
<td>Meinel, Christoph</td>
<td>D1.3: 97</td>
<td></td>
</tr>
<tr>
<td>Mercer, Eric</td>
<td>E4.1: 335</td>
<td></td>
</tr>
<tr>
<td>Miki, Morgan H.</td>
<td>A1.8: 15</td>
<td></td>
</tr>
<tr>
<td>Millán, E. San</td>
<td>C6.1: 467</td>
<td></td>
</tr>
<tr>
<td>Mitsuyama, Yukio</td>
<td>A1.6: 11</td>
<td></td>
</tr>
<tr>
<td>Miura-Mattausch, M.</td>
<td>B1.1: 39</td>
<td></td>
</tr>
<tr>
<td>Miyamoto, Naoto</td>
<td>A1.18: 35</td>
<td></td>
</tr>
<tr>
<td>Miyaoita, Yuichi</td>
<td>C2.2: 156</td>
<td></td>
</tr>
<tr>
<td>Miyawaki, D.</td>
<td>B1.1: 39</td>
<td></td>
</tr>
<tr>
<td>Miyazaki, Toshiaki</td>
<td>C7.1: 551</td>
<td></td>
</tr>
<tr>
<td>Mok, Philip K. T.</td>
<td>A1.10: 19</td>
<td></td>
</tr>
<tr>
<td>Morie, Takashi</td>
<td>A1.7: 13</td>
<td></td>
</tr>
<tr>
<td>Moshnyaga, Vasily G.</td>
<td>C4.3s: 302</td>
<td></td>
</tr>
<tr>
<td>Muddu, Sudhakar</td>
<td>A2.3: 120</td>
<td></td>
</tr>
<tr>
<td>Mukherjee, Rajarshi</td>
<td>D2.3: 181</td>
<td></td>
</tr>
<tr>
<td>Mukherjee, Sobhan</td>
<td>D4.2: 319</td>
<td></td>
</tr>
<tr>
<td>Mulvaney, B. J.</td>
<td>B3.2: 209</td>
<td></td>
</tr>
<tr>
<td>Murakami, Kazuaki</td>
<td>A1.19: 37</td>
<td></td>
</tr>
<tr>
<td>Murgai, Rajeev</td>
<td>D7.1: 571</td>
<td></td>
</tr>
<tr>
<td>Munooka, Takahiro</td>
<td>C7.1: 551</td>
<td></td>
</tr>
<tr>
<td>Myers, Chris J.</td>
<td>E4.1: 335</td>
<td></td>
</tr>
<tr>
<td>Nanya, Takashi</td>
<td>E5.1: 425</td>
<td></td>
</tr>
<tr>
<td>Nassif, Suni R.</td>
<td>B2.3: 145</td>
<td></td>
</tr>
<tr>
<td>Nayak, Anshuman</td>
<td>C8.4s: 645</td>
<td></td>
</tr>
<tr>
<td>Negulescu, Radu</td>
<td>E4.3: 347</td>
<td></td>
</tr>
<tr>
<td>Nezuka, Tomohiro</td>
<td>A1.11: 21</td>
<td></td>
</tr>
<tr>
<td>Nicholls, William</td>
<td>A3.2: 192</td>
<td></td>
</tr>
<tr>
<td>Nicolau, Alex</td>
<td>D5.1: 409</td>
<td></td>
</tr>
<tr>
<td>Nicolescu, Gabriela</td>
<td>C1.2: 63</td>
<td></td>
</tr>
<tr>
<td>Nikai, Norihiro</td>
<td>B4.1: 269</td>
<td></td>
</tr>
<tr>
<td>Nishida, Koiichi</td>
<td>C2.1: 151</td>
<td></td>
</tr>
<tr>
<td>Nishihara, Akinori</td>
<td>A1.4: 7</td>
<td></td>
</tr>
<tr>
<td>Nomura, Toshio</td>
<td>C2.1: 151</td>
<td></td>
</tr>
<tr>
<td>Nozawa, Toshiyuki</td>
<td>A1.13: 25</td>
<td></td>
</tr>
<tr>
<td>Ogreneci-Menik, Seda</td>
<td>C8.1: 629</td>
<td></td>
</tr>
<tr>
<td>Ohmi, Tadahiro</td>
<td>A1.13: 25</td>
<td></td>
</tr>
<tr>
<td>Ohmoto, Takafumi</td>
<td>A1.7: 13</td>
<td></td>
</tr>
<tr>
<td>Ohnishi, Mitsuhisa</td>
<td>C2.1: 151</td>
<td></td>
</tr>
<tr>
<td>Ohta, Mitsuyasu</td>
<td>D6.1: 485</td>
<td></td>
</tr>
<tr>
<td>Ohtake, Satoshi</td>
<td>D4.4s: 331</td>
<td></td>
</tr>
<tr>
<td>Ohtsuki, Tatsuo</td>
<td>C2.2: 156</td>
<td></td>
</tr>
<tr>
<td>Okada, Kazuhisa</td>
<td>C2.1: 151</td>
<td></td>
</tr>
<tr>
<td>Okamoto, Takuji</td>
<td>E5.1: 425</td>
<td></td>
</tr>
<tr>
<td>Okuma, Takanori</td>
<td>A1.19: 37</td>
<td></td>
</tr>
<tr>
<td>Oliás, E.</td>
<td>C6.1: 467</td>
<td></td>
</tr>
<tr>
<td>Omaki, Roberto Y.</td>
<td>A1.8: 15</td>
<td></td>
</tr>
<tr>
<td>Onodera, Hidetoshi</td>
<td>A1.1: 1</td>
<td></td>
</tr>
<tr>
<td>Onoye, Takao</td>
<td>A1.6: 11</td>
<td></td>
</tr>
<tr>
<td>Ooshiro, S.</td>
<td>B1.1: 39</td>
<td></td>
</tr>
<tr>
<td>Pan, David Zhigang</td>
<td>B5.1: 373</td>
<td></td>
</tr>
<tr>
<td>Park, Chanik</td>
<td>C1.4: 78</td>
<td></td>
</tr>
</tbody>
</table>

N

<table>
<thead>
<tr>
<th>Name</th>
<th>Page Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nagai, Jin</td>
<td>A1.7: 13</td>
</tr>
<tr>
<td>Nagai, Shintaro</td>
<td>D4.4s: 331</td>
</tr>
<tr>
<td>Nagata, Makoto</td>
<td>A1.7: 13</td>
</tr>
<tr>
<td>Nakamura, Kazuhiro</td>
<td>A1.16: 31</td>
</tr>
<tr>
<td>Nakayama, N.</td>
<td>B1.1: 39</td>
</tr>
<tr>
<td>Nakaya, N.</td>
<td>B1.1: 39</td>
</tr>
</tbody>
</table>

P

<table>
<thead>
<tr>
<th>Name</th>
<th>Page Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pan, David Zhigang</td>
<td>B5.1: 373</td>
</tr>
<tr>
<td>Park, Chanik</td>
<td>C1.4: 78</td>
</tr>
<tr>
<td>Name</td>
<td>(Anonymity)</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>Park, Hyun Chul</td>
<td>C5.4s</td>
</tr>
<tr>
<td>Park, In-Cheol</td>
<td>B6.3</td>
</tr>
<tr>
<td>Park, Yong-Ha</td>
<td>A1.5</td>
</tr>
<tr>
<td>Pedram, Massoud</td>
<td>B3.1</td>
</tr>
<tr>
<td>(D3.1)</td>
<td>239</td>
</tr>
<tr>
<td>(D3.2)</td>
<td>245</td>
</tr>
<tr>
<td>(A8.2)</td>
<td>595</td>
</tr>
<tr>
<td>Peeters, Ad</td>
<td>E3.1</td>
</tr>
<tr>
<td>Peng, Zhang</td>
<td>B4.4</td>
</tr>
<tr>
<td>Peskin, Eric</td>
<td>E4.1</td>
</tr>
<tr>
<td>Qiao, Jian</td>
<td>C3.2</td>
</tr>
<tr>
<td>Ramesh, S.</td>
<td>D5.3s</td>
</tr>
<tr>
<td>Rinard, Martin</td>
<td>D8.2</td>
</tr>
<tr>
<td>Robins, Gabriel</td>
<td>B2.2</td>
</tr>
<tr>
<td>Roop, Partha S.</td>
<td>D5.3s</td>
</tr>
<tr>
<td>Rusakov, S. G.</td>
<td>B3.2</td>
</tr>
<tr>
<td>S, Vaideeswaran</td>
<td>D2.2</td>
</tr>
<tr>
<td>Sakaidani, Satoshi</td>
<td>A1.18</td>
</tr>
<tr>
<td>Sakuraba, Hiroshi</td>
<td>C4.2</td>
</tr>
<tr>
<td>Sarrafzadeh, Majid</td>
<td>D7.2</td>
</tr>
<tr>
<td>(C8.1)</td>
<td>629</td>
</tr>
<tr>
<td>Sasao, Tsutomu</td>
<td>C3.1</td>
</tr>
<tr>
<td>Sato, Jun</td>
<td>D8.1</td>
</tr>
<tr>
<td>Sawai, Tetsuro</td>
<td>B4.1</td>
</tr>
<tr>
<td>Schaumont, Patrick</td>
<td>C7.2</td>
</tr>
<tr>
<td>Schlingloff, Bernd-Holger</td>
<td>E4.2</td>
</tr>
<tr>
<td>Scholl, Christoph</td>
<td>D1.1</td>
</tr>
<tr>
<td>Serval, G.</td>
<td>B7.3</td>
</tr>
<tr>
<td>Shenoy, Narendra</td>
<td>A3.2</td>
</tr>
<tr>
<td>Shibata, Yuichro</td>
<td>A1.9</td>
</tr>
<tr>
<td>Shibayama, Takehide</td>
<td>A1.1</td>
</tr>
<tr>
<td>Shin, Dongwan</td>
<td>D8.3</td>
</tr>
<tr>
<td>Shiomi, Akichika</td>
<td>D8.1</td>
</tr>
<tr>
<td>Shirakawa, Isao</td>
<td>A1.6</td>
</tr>
<tr>
<td>(A1.8)</td>
<td>15</td>
</tr>
<tr>
<td>Sikdar, Biplab K.</td>
<td>D4.2</td>
</tr>
<tr>
<td>Smith, Ross</td>
<td>E5.2</td>
</tr>
<tr>
<td>Sotiriadis, Paul P.</td>
<td>A2.1</td>
</tr>
<tr>
<td>Sowmya, A.</td>
<td>D5.3s</td>
</tr>
<tr>
<td>Sretasereekul, Nattha</td>
<td>E5.3</td>
</tr>
<tr>
<td>Srinivas, Prasanna V.</td>
<td>B5.1</td>
</tr>
<tr>
<td>Srivastava, Ankur</td>
<td>D7.2</td>
</tr>
<tr>
<td>Stangier, Christian</td>
<td>D1.3</td>
</tr>
<tr>
<td>Stroobandt, Dirk</td>
<td>B7.1</td>
</tr>
<tr>
<td>Su, Chauchin</td>
<td>D6.2</td>
</tr>
<tr>
<td>Suetake, M.</td>
<td>B1.1</td>
</tr>
<tr>
<td>Sunaga, Kazuhisa</td>
<td>C4.2</td>
</tr>
<tr>
<td>Svarstad, Kjetil</td>
<td>C1.3</td>
</tr>
<tr>
<td>Swaminathan, Vishnu</td>
<td>D3.3s</td>
</tr>
<tr>
<td>Sze, Chin-Ngai</td>
<td>C6.2</td>
</tr>
<tr>
<td>Takahara, Atsushi</td>
<td>C7.1</td>
</tr>
<tr>
<td>Takai, Kouksume</td>
<td>A1.1</td>
</tr>
<tr>
<td>Takeuchi, Yoshinori</td>
<td>D8.1</td>
</tr>
<tr>
<td>Taki, Daisuke</td>
<td>A1.8</td>
</tr>
<tr>
<td>Tanaka, Masakazu</td>
<td>A5.1</td>
</tr>
<tr>
<td>Tang, Xiaoping</td>
<td>A7.4</td>
</tr>
<tr>
<td>Tani, Kumiuki</td>
<td>B4.1</td>
</tr>
<tr>
<td>Tarui, Masaya</td>
<td>A1.8</td>
</tr>
<tr>
<td>Thornton, Mitch</td>
<td>B8.2</td>
</tr>
<tr>
<td>Ting, Ivor</td>
<td>C6.3</td>
</tr>
<tr>
<td>Togawa, Nozomu</td>
<td>C2.2</td>
</tr>
<tr>
<td>Tomiyama, Hiroyuki</td>
<td>D5.1</td>
</tr>
<tr>
<td>Tsai, Ching-Hong</td>
<td>D4.3</td>
</tr>
<tr>
<td>Tsui, Chi-Ying</td>
<td>A1.10</td>
</tr>
<tr>
<td>Tsukiyama, Shuji</td>
<td>A5.1</td>
</tr>
<tr>
<td>Ulyanov, S. L.</td>
<td>B3.2</td>
</tr>
</tbody>
</table>
V
Vahid, Frank ................... (C4.4s) 306
Vanmeerbeeck, Geert .......... (C7.2) 558
Vaya, Shailesh ................. (B2.1) 133
Veneris, Andreas .............. (C6.3) 479
Vernalde, Serge ............... (C7.2) 558

W
Wada, Atsushi ................. (B4.1) 269
Wada, Hiroki ................. (D4.4s) 331
Walker, Duncan M. H. ....... (D2.3) 181
Wang, Li-C. ................. (A7.3) 515
Wang, Ting-Chi .............. (A7.3) 515
Wang, Zeyi .................. (B3.3) 214
Wang, Zhi-Hong ............. (C8.2) 635
Watanabe, Katsumasa ........ (A1.16) 31
(5.2s) 396
Wehn, Norbert ............... (C5.3s) 400
Wong, D. F. ................. (A3.3) 198
(7.4) 521
(7.2) 533
(8.1) 589
Worm, Alexander ........... (C5.3s) 400
Wu, Allen C.-H. ............ (C2.3) 162
Wu, Cheng-Wen ............. (D4.3) 325
(5.1) 391
Wu, Chung-Hsien ............ (C5.1) 391
Wu, Weimin ................. (A8.4s) 605
Wu, Youliang ............... (A8.3s) 601
Wu, Yu-Liang ............... (C6.2) 473
(8.3s) 641

X
Xiao, Liyi ...................(B4.4) 287
Xie, Xiaofeng .............. (B1.2) 45

Y
Yamada, Akihisa .......... (C2.1) 151
Yamada, Mitsuru .......... (A1.4) 7
Yamaguchi, T. ............ (B1.1) 39
Yamaoka, Hiroaki ......... (A1.2) 3
Yamashita, K. ............ (B1.1) 39
Yan, Kenneth ............ (C3.3s) 231
Yanagisawa, Masao ...... (C2.2) 156
Yang, Cliff ............... (D4.2) 319
Yang, Wooseung .......... (B6.3) 462
Yang, Zhaozhi .......... (B3.3) 214
Yang, Zhilian ........... (B1.2) 45
Yasuda, Takeo .......... (B4.2) 275
Yin, Liang ............... (B5.3) 385
Yizheng, Ye ............. (B4.4) 287
Yoneda, Tomohiro ....... (E4.2) 341
Yoo, Hoi-Jun .......... (A1.5) 9
Yoo, Sungjoo .......... (C1.2) 63
Yoshimura, Masayoshi .... (D6.1) 485
Young, Fung Yu .......... (A7.1) 503
Yu, Hong ................ (A8.4s) 605
Yu, Hyeongseok ....... (C5.4s) 404
Yu, Wenjian ........... (A5.3) 366
Yuen, Wing Seung ....... (A7.1) 503

Z
Zammit, Vince .......... (C2.1) 151
Zelikovsky, Alexander ... (A2.3) 120
(B2.1) 133
(B2.2) 139
Zhang, Wenjun ........... (B1.2) 45
Zhang, Yumin ........... (B8.1) 609
Zharov, M. M. ........... (B3.2) 209
Zhou, Hau-Zen ........... (D6.2) 492
Zheng, Hao ............... (E4.1) 335
Zhou, Bin ............... (E4.2) 341
Zhou, Hai ............... (A3.2) 192
Zhu, Jianwen ........... (C1.1) 57
Zhu, Qiang ............ (A1.16) 31
(C5.2s) 396
CALL FOR PAPERS AND PARTICIPATION

A Joint Conference in 2002

The Seventh Asia and South Pacific Design Automation Conference

TOPICS OF INTEREST: Papers are invited on topics related to, but not limited to, the following areas: System-on-a-chip design, IP based design, DSP design, processor design, ASIC design, analog/mixed-signal design, VLSI in specific domains such as wireless communication, broadband access, multimedia, networking, etc., low power design, hardware/software co-design, high level synthesis, logic synthesis, simulation, formal verification, static timing analysis, interconnect analysis, issues in deep submicron VLSI, design for reliability, design for manufacturability, all aspects of test and DFT, physical design, programmable devices, reconfigurable architectures, CMOS devices, integrated circuits manufacturing, device modeling and simulation, MEMS, design methodologies, electronic design automation algorithms and tools.

PAPER SUBMISSION: Please submit previously unpublished papers electronically (as postscript or pdf files) on the conference website by July 14, 2001. The manuscript should clearly state the novel ideas, results and applications of the contribution. Please identify the contact author and include the complete mailing address, e-mail address, telephone and/or fax numbers of the authors. Papers should not exceed 15 double-spaced pages including figures and references. The papers will be selected on the basis of peer reviews. Authors will be notified of acceptance by August 31, 2001. Camera-ready papers should be submitted on the conference web site by September 28, 2001.

TUTORIALS: This conference will dedicate two days to six full-day tutorials on recent topics in VLSI Design and EDA. Topics are open at this time, and speakers are encouraged to submit proposals in any area of VLSI design and EDA. Please submit proposals on the conference website by May 25, 2001.

SPECIAL SESSIONS: Proposals for special sessions (a set of related papers on a subject) will be considered for inclusion in the technical program. Special session proposal should include a two-page summary of the session and a list of papers on the conference website. Papers in the list should be submitted according to the paper submission guidelines. This material should be submitted on the website by July 14, 2001. Papers that are part of the special session will go through the same peer review process as regular papers.

EXHIBITS: The conference provides a unique opportunity for vendors of VLSI design tools and services to display their products/services. Exhibition space is limited and those interested should immediately contact the Exhibits Chair.

AWARDS: A Best Paper Award (Prof. A. K. Choudhury Award), a Best Student Paper Award and two Honorable Mention Awards will be given. Student authors should be identified on the manuscripts. Papers with first author as a student author will be eligible for the Best Student Paper Award. The conference will also run a design contest. Please check conference website for contest rules and submit contest entries by September 28, 2001.

FELLOWSHIPS: The Steering Committee will award fellowships, based on need and merit, to partially cover expenses of attendees. Application forms will be available at the conference website. Completed applications should be submitted on the website by October 15, 2001. Travel grants are also available for ACM SIGDA members.

IMPORTANT DATES:
Conference dates : January 7-11, 2002
Tutorial proposals submission : May 25, 2001
Regular papers submission : July 14, 2001
Acceptance notification to authors : August 31, 2001
Camera-ready papers : September 28, 2001
Design contest entries : September 28, 2001

For more information, please visit the website:
CALL FOR DESIGNS AND PARTICIPATION

A Joint Conference in 2002

The Seventh Asia and South Pacific Design Automation Conference

ASPDAC 2002

The Fifteenth International Conference on VLSI Design

VLSI DESIGN 2002

January 7-11, 2002, Bangalore, India

In Cooperation with: (under approval)

IEEE

Sponsored by: (under approval)

VLSI Society of India (VSI)
Department of Electronics, Government of India
IEEE Circuits and System Society
ACM SIGDA

As a unique feature of 2002, ASPDAC and VLSI Design will be held as a single joint conference. Accordingly, the design contests associated with these two conferences are also being merged.

The aim of the Contest is to encourage education and research in state-of-the-art in VLSI design and its realization at universities and other educational organizations.

Original VLSI circuit designs that meet some of the following conditions are highly solicited for submission from students worldwide:

(1) Designed, and actually implemented on chips or other educational organizations during the last two years.
(2) Designs that report actual measurements from implementations
(3) Innovative design prototypes

Interesting or excellent designs selected will be honored by providing opportunities for presentation in a special session at the conference. Awards will be given to outstanding designs selected from those presented at the conference.

Based on the merit of the design submitted from within India, it might be possible to offer fabrication support for selected submissions.

Areas of Design:
Application areas, or types of circuits, include (not limited to):
(1) Analog and Mixed-Signal Circuits
(2) Digital Signal Processing
(3) Microprocessors
(4) Custom Application Specific Circuits

Methods, or technology, used for implementation include (not limited to):
(a) Full Custom and Cell-Based LSIs
(b) Gate Arrays
(c) Field Programmable Devices, including FPGA/PLDs
(d) Hardware-Software Co-Design

Submission of Design Descriptions:
It is requested to send to the Conference Secretariat, 10 copies of the summary in camera-ready format in English, that satisfy the following conditions:

(1) The cover page should include
(i) indication that it is an application for University LSI Design Contest
(ii) title of the design
(iii) authors and affiliations
(iv) speaker
(v) mailing address, Phone No., Fax No., and e-mail address of the contact author
(vi) area of the application and implementation method, expressed using the codes shown in the above Areas of Design (e.g. “3-a” for a full custom microprocessor)
(vii) clear and brief description on the application, originality, and other features of the design
(viii) contribution of each author, if the LSI is jointly developed with non-academic parties

(2) The summary is requested to be written within 2 pages, including figures, tables, and references. Specification of the camera-ready format is available at our web site http://www.aspdac.com.

(3) It is strongly recommended that measured experimental results and a chip micrograph should be included. If the experimental results and the chip micrograph have not been prepared before the deadline of submission, the authors can send the revised paper including them later.

Review process:
The following criteria will be applied in the selection of designs:
(1) Reliability of design and implementation
(2) Quality of implementation
(3) Performance of the design
(4) Novelty of application, algorithm, architecture

Interesting or excellent designs selected will be presented at a special session of the conference.

Awards:
Also, the following awards will be given to a few number of outstanding designs, selected from those presented at the conference.

(1) Outstanding design award
(2) Special feature awards

Presentation:
An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2002/VLSI DESIGN 2002. A digest of each design to be presented will be included in the conference proceedings.

Important dates:

Summary submission: July 28, 2001
Experimental results and chip micrograph submission: September 8, 2001
Acceptance notification to participants: October 13, 2001
Camera-ready papers: November 17, 2001

For more information, please visit the website:
Session Index

Session A1 - (Special Session) University LSI Design Contest
Session B1 - Device/Circuit Co-designing for Advanced Technologies
Session C1 - System Level Specification and Simulation
Session D1 - Issues in BDD and Sequential Verification
Session A2 - Interconnect Design Optimization (I)
Session B2 - Design for Manufacturability
Session C2 - System Level Design
Session D2 - Important Problems in Equivalence Checking
Session A3 - Interconnect Design Optimization (II)
Session B3 - Parasitic Extraction and Reduced Order Model
Session C3 - Functional Decomposition and PLA-based Logic Synthesis
Session D3 - Low Power Techniques for Embedded Software
Session E3 - (Special Session) Asynchronous System Design: Architecture and Low-Power Design
Session A4 - (Panel) Beyond the Red Brick Wall: Challenges and Solutions in 50nm Physical Design
Session B4 - Analog Design Methodology
Session C4 - Low Power Design Methodology
Session D4 - Advanced BIST: Methodology and Applications
Session E4 - (Special Session) Asynchronous System Design: Verification
Session A5 - DSM Design and Analysis
Session B5 - Signal Integrity and Analysis
Session C5 - Design Experiments for Mobile Applications
Session D5 - Compilation Techniques for Embedded Software
Session E5 - (Special Session) Asynchronous System Design: Synthesis
Session A6 - Design Technology Productivity in the DSM Era
Session B6 - System Level Power Optimization
Session C6 - Multi-level Logic Optimization for Logic Circuits
Session D6 - Practical and High Level DFT
Session A7 - Performance Driven Floorplanning and Placement (I)
Session B7 - Improving Delay and Power Estimation
Session C7 - Networked Reconfiguration and Systems
Session D7 - Advances in Timing Optimization of Logic Circuits
Session A8 - Performance Driven Floorplanning and Placement (II)
Session B8 - Logic Synthesis for Low Power and Design Space Exploration
Session C8 - Optimization Technique for FPGAs
Session D8 - Processor Synthesis