

Simulating Frequency-Dependent Current Distribution for Inductance Modeling of On-Chip Copper Interconnects

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ABSTRACT

500+ MHz designs using deep-submicron (DSM) copper interconnects require accurate and efficient modeling of cladding-metals' frequency-dependent impedance [1]. In this paper, for the first time, we simulate and describe the current distribution inside a copper-based interconnect in a rich set of multi-line structures. The difference of the resistivities of copper alloy and the cladding metals causes a non-monotonic current density versus cross-wire axis relation. The same situation does not occur for the state-of-the-art aluminum processes. It enlarges the inductance by more than 12 percent. Simulating the frequency dependence of the inductance with this property, we find that PEEC [2][3] can simulate cladded wire profile to achieve accurate inductance extraction. Other approximate methods result in inaccurate and lower inductance values. A new modeling methodology based on library look-up is then proposed to make an efficient field-solver based extraction flow for realistic DSM designs.

KEYWORDS

Copper interconnect, skin-effect current distribution, cladding material, electromagnetic field solvers.

1. INTRODUCTION

Copper is becoming a promising material for interconnects of high-speed VLSI chips. However, copper cannot be manufactured the same as aluminum-based interconnect because of possible oxide poisoning, among other effects. The copper interconnect process introduces a "cladding" that envelops the copper wire, as depicted in Figure 1 (a). Cladding typically consists of titanium nitride (TiN), tantalum nitride (TaN), or tungsten nitride (WN). All are about five to ten times as resistive as copper. For DSM copper on-chip interconnect, Figure 1 (a) provides a practical but idealized cross-sectional profile of the barrier metal in each copper interconnect. Nevertheless, this paper provides useful and insightful data based on the idealized cross-sections.

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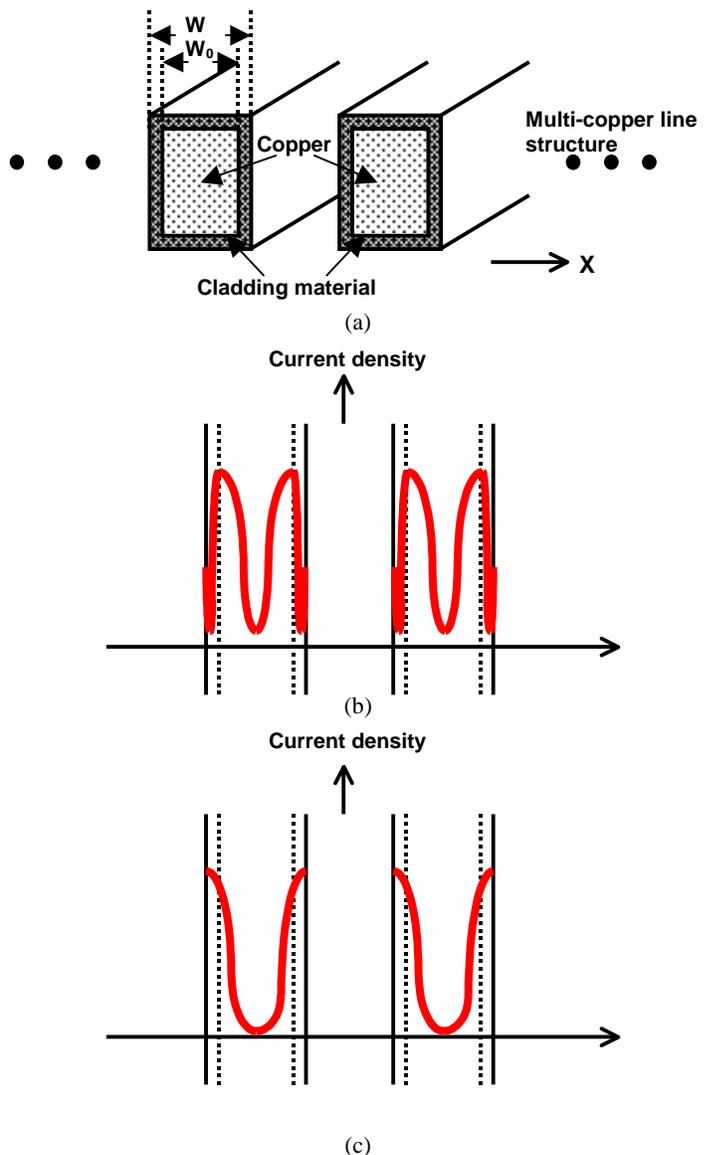


Figure 1. (a) Profile of cladded copper-alloy wire in a multi-line structure. (b) Current density versus line-axis relation for the cladded copper wire. (c) Current density function for aluminum based wires.

DSM technologies provide the advantage of using same-layer interconnect neighbors as shields and current return paths to control the dominating inductance effect [4][5]. Therefore, the cladding metal on the sidewalls is more important in influencing the electrical performance of the wire than the cladding metal on the top or the bottom as shown in Figure 1 (a). Not only does the cladding increase the wire's sheet- ρ significantly [1], it also changes the current distribution and the skin effect significantly compared with the traditional aluminum-based interconnects.

Inside a copper-base wire, the current distribution through electromagnetic field simulations has an oscillatory relation with the wire's horizontal axis, as depicted in Figure 1 (b). The maximum current density is located near the copper-cladding metal boundary instead of the outer surface of the cladding metal. That is to say, electrons traveling in a copper wire tend to flow in the copper boundary, even under skin effect. Electrons behave in this way to minimize the total impedance. Therefore, the current-distribution profile is very different from the intuitive, monotonic current distribution profile for aluminum-based wires, as shown in Figure 1 (c). The implication of inductance modeling in the cladding areas in Figure 1 (b) is the relatively sparse electrons crowd more at the outer surface than the inner one to increase the mutual inductance of the wire. By the way, the current distribution is dependent on frequency and on several interconnect process parameters.

In this paper, for the first time, we simulate the frequency dependence of the inductance effect of DSM copper-based interconnects with consideration of non-monotonic current distribution. We find that the simulated current distribution in Figure 1 (b) enlarges the inductance from other approximate methods such as the effective-resistivity method, to be detailed in the next section. A rigorous PEEC method was used to impose the material profile to enable uneven current flow and produce accurate result. For densely spaced DSM interconnects, this physics results in a new EDA software solution.

2. SIMULATING FREQUENCY DEPENDENCE of INDUCTANCE FOR COPPER INTERCONNECTS

We set up three different multi-line structures for the simulation of copper-based interconnects. In Figure 2, we show the profile of (a) simple brick-structure wires with only copper, (b) brick-structure wires with an effective sheet- ρ obtained from (c), and (c) cladded copper wires. Converting the parallel copper and cladding resistivities into an effective sheet- ρ , the simplified brick model in Figure 2 (b) is often used to represent the actual copper wire in (c). Cladding in Figure 2 (c) is $0.05 \mu\text{m}$ thick, and is ten times as resistive as copper. Because the central signal lines in Figure 2 are about $10 \mu\text{m}$ above the substrate, they must use the neighboring grounded shielding lines [3] to conduct inductive return current. The width of the signal and shielding lines and the inter-line spacing are both $0.5 \mu\text{m}$. With these setups, we simulate both the resistance and inductance for various harmonic frequency [1] values for the signal line.

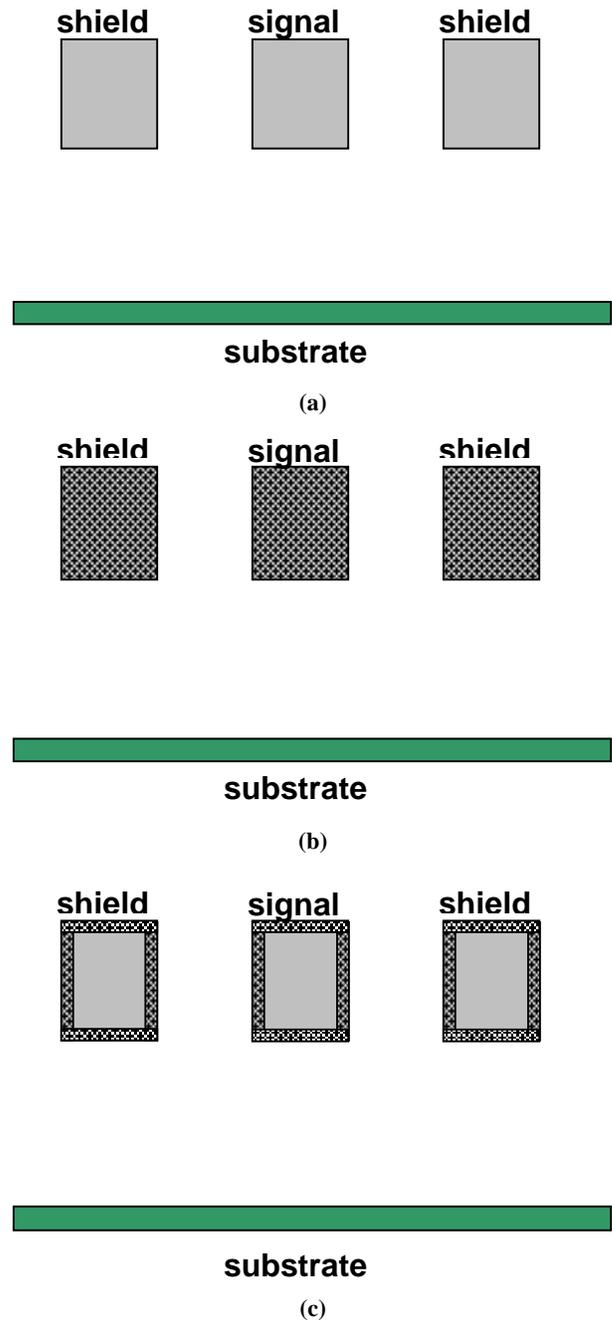


Figure 2. Multi-line inductance and resistance test structures representing (a) simple brick all-copper structure, (b) effective sheet- ρ structure, and (c) cladded copper structure.

We must caution to incorporate the correct current distribution profile for copper wires in Figure 1 (b). Calculation of both self-partial and self-mutual inductances requires a uniform electrical

current flowing through the current filament being considered in the field solver. We have used a piecewise constant current subbar consideration, as shown in Figure 3. In Figure 3, we show the current element we put on the cross section for a cladded copper wire (shown for a corner of the wire). Both the cladding area and the copper area are sufficiently cut into constant-current subbars to accurately carry the varying current distribution shown in Figure 1. With this treatment, a PEEC algorithm can be built into a field solver [6][7] to calculate the inductance and resistance of a copper line.

3. RESULTS AND DISCUSSION

We find that the cladded copper structure depicted in Figure 2 (c) yields more than 12 percent higher inductance than either all-copper (depicted in Figure 2 (a)) or effective-sheet- ρ structure (depicted in Figure 2 (b)) throughout the frequency range of which we are concerned, namely from 10 MHz to 100 GHz. The cladded copper wire has higher inductance because its current distribution profile elevates the self-partial inductance (L_{ii}) for the signal line and reduces the mutual inductance (L_{jk}) between the signal and the shields, compared with the traditional profile.

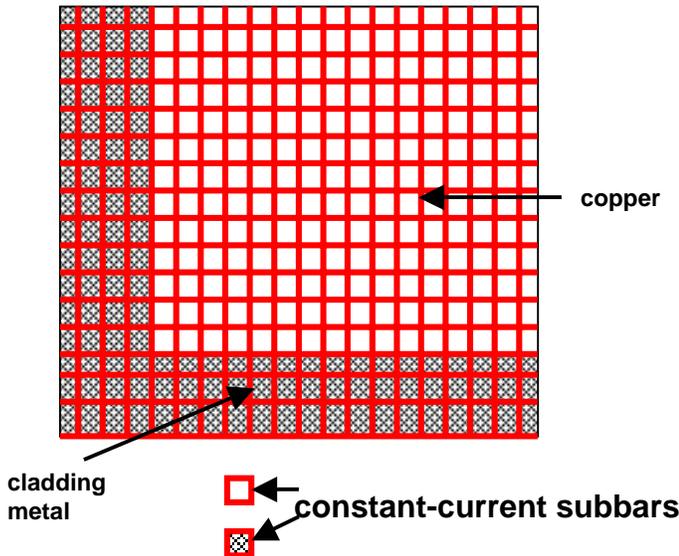


Figure 3. The cross section of a cladded copper wire is sectioned into n subbars. This is the model suitable for a PEEC algorithm for inductance and resistance calculation.

These factors combine to increase the total loop inductance because the total inductance is always a function of L_{ii} and L_{jk} as

$$L_{loop} = \sum_{i=1}^n F(L_{ii}) - \sum_{j,k=1}^n F(L_{jk}) \quad (1)$$

In Equation (1), n is the number of interacting signals, and $F(L_{ii})$ ($F(L_{jk})$) is a linear function of L_{ii} (L_{jk}). On the other hand, both the all-copper and the effective-sheet- ρ structures have the monotonic current distribution depicted in Figure 1 (c) and thus

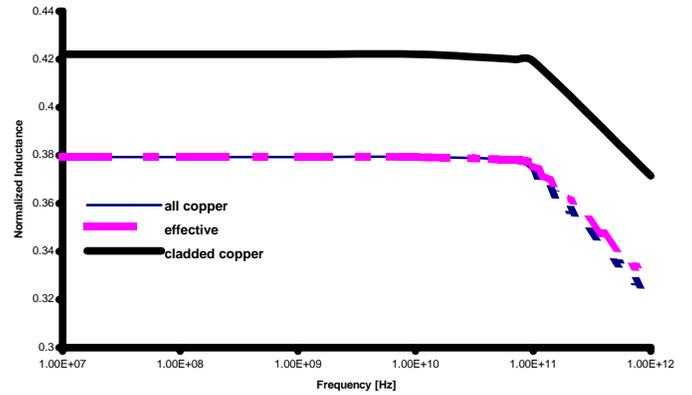


Figure 4. Inductance versus frequency relation for the three different wire structures.

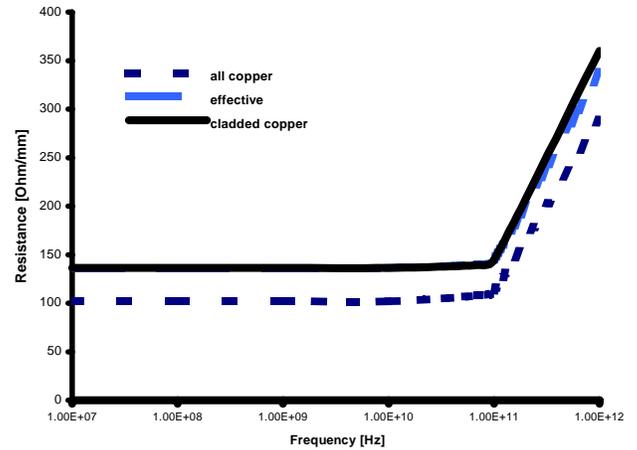


Figure 5. Resistance versus frequency relation for the three different wire structures.

have lower inductance. For the same reason, the inductance will be even higher if the cladding is more resistive. The findings we obtained here are not unique for copper; any cladded metal on the sidewall with a significant (5-10 times) higher sheet resistivity should yield a similar outcome for inductance.

In Very Deep-Submicron technologies (VDSM, feature size $\leq 0.18 \mu\text{m}$), the phenomenon of increased inductance becomes more obvious. Because both the width and the spacing are already very narrow in VDSM designs, the peak current-distribution is moved from the outer surface to the inner one. It makes a greater impact on the increase of inductance. The investigation for inductance effects in this regime without rigorous physical considerations and an accurate field solver will be risky for designers.

In Figure 5, we show the result of resistance versus frequency relation. In Figure 5, all resistance curves start with their DC values before skin effect takes place at about 100 GHz. The all-

copper structure described in Figure 2 (a) has smaller resistivity than the structures in both (b) and (c). After frequency is larger than 10 GHz, skin effect causes the resistance to rise. If the line is wider, the skin effect takes place at a lower frequency, e.g. 500 MHz. Throughout the sweep of frequency, field calculation for the effective-sheet- ρ model and the actual cladded model yields very similar results.

A multi-line structure suitable for most aluminum-based interconnect skin-effect modeling is shown in Figure 6. There are cladding metals only on the top and the bottom of the wires, not on the sidewalls. Because the resistivity is constant along the horizontal wire axis, there is no significant inductance increase for this case. An effective-sheet- ρ structure can be sufficient for an accurate extraction of frequency dependence of both inductance and resistance.

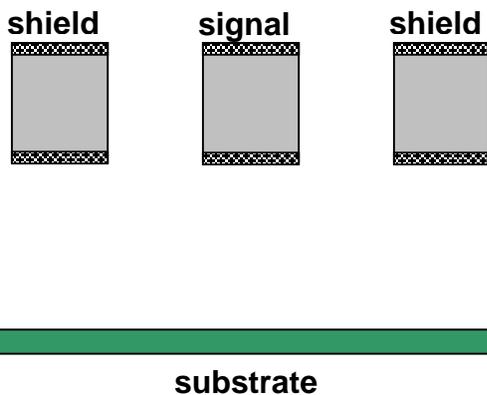


Figure 6. Multi-line wire structure with cladding metals placed on only the top and bottom of the wires. This structure represents aluminum-based interconnects.

4. AN INTERCONNECT LIBRARY METHOD

Considering the complex current distribution phenomenon and the unusual frequency dependence of inductance for copper-based interconnects, we therefore propose a new methodology in this section that can enable accurate and efficient VLSI interconnect modeling for today's and future process technologies. This methodology also includes a solution to the varying DC sheet resistivity problem discussed in [1]:

Step 1. For each cladded metal layer in a DSM/VDSM technology, specify a sufficient set of structures with line widths/spaces and neighbors that can be used by designers;

Step 2. Adequately construct electrical current subbars for each test structure with accurate sheet resistivity of both core metal (e.g. copper) and the cladding metals.

Step 3. Use PEEC-based field solvers [6][7] to simulate the effective resistance and inductance for each structure and store them in a library [8].

5. CONCLUSIONS AND FUTURE WORK

We have studied the current distribution and frequency dependence of inductance for copper-based interconnects. Using rigorous physical considerations, we find the current distribution for copper wire is very different from the traditional one produced by simple skin-effect theory. The current distribution shows a non-monotonic, oscillatory profile along the horizontal wire axis. The novel current distribution for copper wire leads to an increased inductance for a shielded line structure compared to structures based on the traditional current distribution profile. We have explained the physics behind all these findings in detail. We have also proposed a new library methodology to achieve accurate and efficient skin effect modeling for DSM and VDSM technologies.

Different field solvers use different methods to discretize a conductor in simulation. Each method attempts to provide physics-based inductance and resistance values. So far, the consistency among them is satisfactory. As for the exact amount of current being distributed for the cross-section, it is not commonly provided and it has to be indirectly derived by the end user. We plan to work with the authors of the field solvers more closely within the next three months and plan to present our results during the conference.

6. ACKNOWLEDGMENT

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