Voltage Dependent Gate Capacitance and its Impact in Estimating Power and Delay of CMOS Digital Circuits with Low Supply Voltage

Koichi Nose, Soo-Ik Chae* and Takayasu Sakurai
Institute of Industrial Science, University of Tokyo, 7-22-1 Roppongi, Minato-ku, Tokyo, 106-8558 Japan
Phone: +81-3-3403-1643, Fax +81-3-3403-1649, nose@iis.u-tokyo.ac.jp
*) School of EE, Seoul National University, Rm.804, Bldg.301, San 56-1, Shinlim-dong, Kwanak-gu, Seoul 151-742 Korea

ABSTRACT
Gate capacitance has complex voltage dependency on terminal voltages but the impact of this voltage dependency of gate capacitance on power and delay has not been fully investigated, especially, in low-voltage, low-power designs. Introducing an effective gate capacitance, \( C_{G,\text{eff}} \), it is shown that the power and delay of CMOS digital circuit can be estimated accurately. \( C_{G,\text{eff}} \) is a strong function of \( V_{\text{TH}}/V_{\text{DD}} \) and \( V_{\text{TH}}/V_{\text{DD}} \) tends to increase in low-voltage region. Hence, the effective capacitance relative to oxide capacitance, \( C_{\text{OX}} \), is decreasing in low-voltage, low-power designs. Therefore, considering \( C_{\text{G,eff}} \) in accurate power and delay estimation becomes more important in the future.

Keywords
Gate capacitance, low supply voltage, low-power design.

1. Introduction
Capacitance plays an important role in estimating power and delay of CMOS digital VLSI’s. Load capacitance of CMOS circuits, \( C_{\text{LOAD}} \), which determines the power and delay is expressed as follows.

\[
C_{\text{LOAD}} = \sum C_G + \sum C_J + \sum C_{\text{INT}},
\]

where \( C_G \), \( C_J \) and \( C_{\text{INT}} \) denote gate, junction and interconnection capacitance, respectively. In these capacitances, \( C_G \) and \( C_J \) have complex voltage dependency on terminal voltages but the impact of this voltage dependency of \( C_G \) and \( C_J \) on power and delay has not been fully investigated, especially, in low-voltage, low-power designs. In this paper, the effect of the voltage dependent gate capacitance on circuit behaviors is analyzed and an appropriate choice of the effective constant gate capacitance is discussed. The impact of the voltage dependent nature is investigated for low-voltage, low-power designs.

2. Voltage dependent capacitance of MOSFET
Gate capacitance seen from the input, \( C_G \), is a function of terminal voltages as is shown in Fig. 1. \( C_G \) is not equal to \( C_{\text{OX}} \), which is calculated from oxide thickness and is constant. In a subthreshold region, \( C_G \) is much smaller than \( C_{\text{OX}} \) and in an on-state, \( C_G \) is different between a linear region and a saturation region. If a CMOS inverter is formed, the input capacitance changes as in Fig. 2. In calculating the capacitance, the current flown into a gate terminal is integrated over time. It is obvious that the behavior of \( C_G \) changes depending on the threshold voltage. Since \( C_G \) is always smaller than \( C_{\text{OX}} \) and shows the minimum just before the threshold voltage, the effect of \( C_G \) is expected to decrease when \( V_{\text{TH}}/V_{\text{DD}} \) gets larger.

There is also a gate-drain overlap capacitance, \( C_{\text{OV}} \), associated with a MOSFET. Since the overlap capacitance is not voltage dependent, it is not considered in this paper. The overlap capacitance effect can be considered by just adding \( 2C_{\text{OV}} \) in an estimation process.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.

ISLPED ’00, Rapallo, Italy.
Copyright 2000 ACM 1-58113-190-9/00/0007…$5.00.
3. Definition of effective gate capacitance

Let us consider an NMOS case for simplicity. An extension to a PMOS case is straightforward. Considering an inverter turning on, in an initial state, \( V_{GS} \) is 0 and \( V_{DS} \) is \( V_{DD} \) and \( V_{GS} \) reaches \( V_{DD} \). Power and delay simulated into a gate terminal in circuit operation, which determines power and delay of digital circuits.

In calculating \( \Delta Q_{G} \), the current flown into a gate terminal can be integrated over time as is shown in Fig. 3. As is seen from the same figure, \( \Delta Q_{G} \) is not path dependent so that any waveforms for \( V_{OS} \) and \( V_{DS} \) can be used to obtain \( \Delta Q_{G} \).

It should be noted that \( C_{Geff} \) is defined for an NMOS and a PMOS transistor. Thus, the number of simulations needed to extract \( C_{Geff} \) for an LSI is limited to the number of kinds of transistors in a design, which is usually two or a little more for most digital designs. Input gate capacitance of a complex gate can be calculated by adding \( C_{Geff} \) of MOSFET’s.

Junction capacitance is also voltage dependent but it is a two-terminal device and the definition of the effective capacitance, \( C_{Geff} \), is trivial as follows.

\[
C_{Geff} = \frac{1}{V_{DD}} \int_{0}^{V_{DD}} J_{G}(V) dV = \frac{Q_{G}(V_{DD}) - Q_{G}(0)}{V_{DD}} \frac{\Delta Q_{G}}{V_{DD}}
\]

\( A \) is not dependent on voltage wave shape and well-defined.

4. Application of effective gate capacitance

The effective gate capacitance, \( C_{Geff} \), is applied to estimate power and delay of a CMOS inverter in Figs. 4 and 5. Power and delay simulated by using constant \( C_{OX} \) and \( C_{Geff} \) as gate capacitance are denoted as \( P(C_{OX}) \), \( t_{d}(C_{OX}) \), \( P(C_{Geff}) \), and \( t_{d}(C_{Geff}) \), respectively. Power and delay simulated by using real MOS gate is denoted as \( P(MOS) \) and \( t_{d}(MOS) \), which are supposed to be true. Two different device models are used to check the effectiveness of the proposed \( C_{Geff} \). Both models are based on BSIM model and charge conservation in capacitance models is observed [2]. In order to concentrate on the gate capacitance effect, \( C_{J} \) and \( C_{INT} \) are set zero in the simulations.

\[
\frac{P(MOS)}{P(C_{OX})} \quad \text{and} \quad \frac{t_{d}(MOS)}{t_{d}(C_{OX})} \quad \text{are less than 0.5 when} \quad V_{TH}/V_{DD} \quad \text{is above 0.6. This means that constant} \quad C_{OX} \quad \text{approximation for a gate capacitance becomes poor when} \quad V_{TH}/V_{DD} \quad \text{increases. The discrepancy is mainly due to the smaller capacitance in the subthreshold region. If we use} \quad C_{Geff} \quad \text{instead of} \quad C_{OX}, \quad P(C_{Geff}) \quad \text{and} \quad t_{d}(C_{Geff}) \quad \text{can reproduce} \quad P(MOS) \quad \text{and} \quad t_{d}(MOS) \quad \text{well.}
\]

In order to check the validity of the \( C_{Geff} \) approximation, a more complex circuit, 4-bit counter, is analyzed. Again, simulations are carried out using \( C_{Geff} \), \( C_{OX} \) and real MOS gate for gate capacitances. Circuits shown in Fig. 6 are adopted to represent three cases. Each gate in a counter is substituted by one of the three types of gates. The results are shown in Fig. 7. In both power and delay comparison, \( C_{Geff} \) reproduce well the real gate for gate capacitance, while \( C_{OX} \) approximation gives larger power and delay by a factor of more than two.

Slight disagreement in power and delay between \( C_{Geff} \) approximation and the MOS gate simulation is due to the fact that the operation of MOSFET does not always start with \( V_{GS} = 0 \) and \( V_{DS} = V_{DD} \) and end with \( V_{GS} = V_{DD} \) and \( V_{DS} = 0 \). This situation is observed in series connected MOS structures in NAND and other complex gates. The disagreement is also due to the substrate bias effect in the stacked structure. It can be said, however, that the disagreement is small and using \( C_{Geff} \) is much more accurate than to use \( C_{OX} \) as a constant capacitance in estimating power and delay.
5. Discussion

A future trend of an optimum threshold voltage has been discussed in a previous publication [3]. The trend in optimum $V_{TH}$ is calculated using the device parameters given in the ITRS Roadmap[6]. Figure 8 shows the calculated result of the trend of the optimum threshold voltage. Supply voltage, $V_{DD}$, will be decreased in the future to cope with the power increase problem and to guarantee sufficient reliability. Low $V_{DD}$ is also used for achieving low-power CMOS VLSI’s. The threshold voltage, however, cannot be decreased with the same rate as $V_{DD}$ decreases due to the exponential increase of subthreshold leakage. As a result, $V_{TH}/V_{DD}$ tends to increase in the future and the discrepancy between $C_{G,eff}$ and $C_{OX}$ gets bigger.

Although CAD tools take the voltage dependent capacitance effect correctly, designers use $C_{OX}$ instead of $C_{G,eff}$ as an effective gate capacitance from time to time and it seems working well at present. This is because $V_{TH}/V_{DD}$ is about 0.15 and the discrepancy between $C_{G,eff}$ and $C_{OX}$ is about 10%, that is, small.

Moreover, although the power and delay are estimated a little larger than reality, this effect is being canceled out by neglecting short-circuit current component which tends to increase the delay and the power by about 10% [4]. In low-voltage designs, however, $V_{TH}/V_{DD}$ becomes larger and the short-circuit current tends to diminish while the discrepancy between $C_{G,eff}$ and $C_{OX}$ tends to increase. Then the cancellation does not take place. Consequently, the constant capacitance approximation using $C_{OX}$ becomes less and less accurate and $C_{G,eff}$ should be used instead in the future.

CINT is dominant in $C_{LOAD}$ in many cases, and in that situation, the accuracy of the gate capacitance approximation is less important but there are cases where CINT is small and gate capacitance affects the circuit behavior much like in some hand crafted data-path circuits.

6. Conclusion

Appropriate effective gate capacitance, $C_{G,eff}$, has been defined and a method is proposed to extract the value by using SPICE. It is shown that the power and delay of CMOS digital circuit can be estimated accurately by introducing $C_{G,eff}$. $C_{G,eff}$ helps designers give insights into the circuit behavior more accurately. Since $C_{G,eff}$ is $V_{TH}$ dependent so is the power. This is one source of fluctuation in power for mass produced VLSI’s.

The discrepancy between $C_{G,eff}$ and $C_{OX}$ is increasing in low-voltage regime and adopting $C_{G,eff}$ in accurate power and delay estimation becomes more important in the future.

Acknowledgement

Useful discussions with K.Sasaki, and K.Ishibashi from Hitachi and T.Kuroda from Toshiba are appreciated.

This work is carried out under Mirai-Kaitaku project.

References


