A 1.5V Low-Power Third Order Continuous-Time Lowpass ΣΔ A/D Converter

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ABSTRACT

This paper presents the design of a 3rd-order lowpass ΣΔ analog-to-digital (A/D) converter using a continuous-time (CT) loopfilter. The loopfilter has been implemented by using active RC-integrators. The influence of the low supply voltage on the building blocks such as the amplifier and the common mode feedback as well as on the overall ΣΔ modulator is discussed. Simulation results of the $1.5V$ CT ΣΔ A/D converter show a 75 dB dynamic range in a bandwidth of $25kHz$. The expected power consumption is less than $300\mu W$.

1. INTRODUCTION

The rapid growing market of portable electronic systems such as wireless communication devices, consumer electronics or battery powered medical devices increases the demand for developing low-voltage and low-power circuit techniques and building blocks. Low-voltage circuit design is desirable to reduce the number of battery cells for low weight- and small system size. Another driving force for low-voltage CMOS design arises from the continuing trend towards deep submicron transistor dimensions.

Reducing the power dissipation in integrated circuits is required to minimize the recharging cycles or extend the battery lifetime as much as possible. Furthermore, the increasing complexity on a chip results in an increase of power density and consequently the demand for power reduction.

An important building block of such systems is an analog-to-digital converter (ADC). Sigma-Delta (ΣΔ) A/D converters are very attractive because they achieve high accuracy for narrow band signals with only a few critical analog components [4]. The use of CT loop filters provides several advantages over switched capacitor implementations. The required GBW of the integrators for a fixed sampling frequency (f_S) is approximately a factor of 3 lower compared to the DT counterparts. This results in further power savings or otherwise a CT A/D converter can operate at higher frequencies. CT loop filter realizations have an implicit antialias filter [4]. On the other hand CT ΣΔ ADC are more sensitive to clock jitter [5] and extra loop delay [4].

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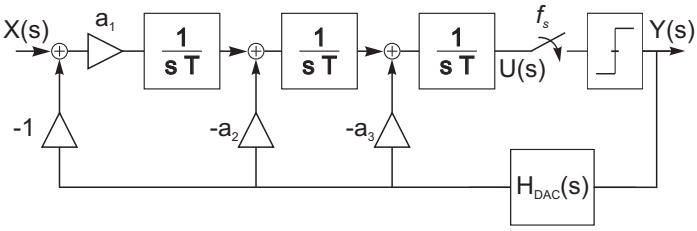

Figure 1: A general structure of a 3rd-order CT ΣΔ modulator. X(s) is bandlimited within f_B.

For low-voltage/low-power applications the single loop architecture as shown in Fig. 1 is the preferred structure over cascaded stages [2], because single loop topologies do not have stringent requirements (e.g. on the DC-gain) for the amplifiers except for the first stage. Further power savings can be achieved by using relatively low oversampling ratios ($OSR = \frac{f_S}{2\,f_B}$). Based on these criteria a third order CT single loop modulator with an $OSR = 32$ is used.

2. DT/CT MODULATOR EQUIVALENCE

The overall behavior of a CT ΣΔ modulator loop is nonetheless discrete time due to the fact that the loop is sampled in time by the clocked quantizer (Fig. 1). For this reason the CT open-loop filter $\hat{H}(s)$ can be replaced by a DT equivalent $H(z)$ with respect to the DAC feedback impulse response. Thus design and simulation of the ideal CT ΣΔ modulator can be done in discrete time domain [4].

The coefficients a_i of the continuous-time modulator can be calculated as a function of the DT integrator coefficients b_i by using the modified Z-transform. The loop filter for the CT third-order modulator results in:

$$\mathcal{Z}(\hat{H}(s)) = \mathcal{Z}_{m1}\left(\frac{-a_1}{Ts^2} + \frac{-a_2}{T^2s^3} + \frac{-a_3}{T^3s^4}\right) - \mathcal{Z}_{m2}\left(\frac{-a_1}{Ts^2} + \frac{-a_2}{T^2s^3} + \frac{-a_3}{T^3s^4}\right) \quad (1)$$

with $m_1 = 1 - \frac{t_d}{T}$ and $m_2 = 1 - \frac{t_d}{T} - \frac{\tau}{T}$ where t_d is the DAC delay and τ the DAC pulse width. Using Tab. 1 and the NRZ-DAC feedback scheme ($m_1 = 1,\ m_2 = 0$), the coefficients a_i are:

Table 1: Modified Z-transform

$Z_m(1/s^2)$	$\frac{mT}{z-1} + \frac{T}{(z-1)^2}$
$Z_m(1/s^3)$	$\frac{T^2}{2}[\frac{m^2}{z-1} + \frac{2m+1}{(z-1)^2} + \frac{2}{(z-1)^3}]$
$Z_m(1/s^4)$	$\frac{T^3}{6}[\frac{m^3}{z-1} + \frac{3m^2+3m+1}{(z-1)^2} + \frac{6m+6}{(z-1)^3} + \frac{6}{(z-1)^4}]$

$$
\begin{aligned}
a_{1_{NRZ}} &= b_1 b_2 b_3 & a_{1_{RZ}} &= 2b_1 b_2 b_3 \\
a_{2_{NRZ}} &= b_1 b_2 b_3 + b_2 b_3 & a_{2_{RZ}} &= 2b_1 b_2 b_3 + 2b_2 b_3 \qquad (2) \\
a_{3_{NRZ}} &= \frac{b_1 b_2 b_3}{3} + \frac{b_2 b_3}{2} + b_3 & a_{3_{RZ}} &= \frac{35}{48} b_1 b_2 b_3 + b_2 b_3 + 2b_3
\end{aligned}
$$

3. ANALOG CIRCUIT DESIGN

The power dissipation of the first integrator is the major contributor to the overall power dissipation in $\Sigma\Delta$ modulators, therefore a substantial amount of power can be saved by a proper circuit design. On the other hand the nonidealities in the input transconductor (distortion and noise) and the first integrator (finite DC-gain, distortion and noise) reduce the performance of the entire A/D converter since these errors add directly to the input signal.

3.1 Leaky CT Integrator

Leakage in CT integrators causes the zeros of the NTF to move from DC to higher frequencies. In presence of this finite amplifier gain A_V one can express the in-band noise power at the output of the third order single-bit modulator as follows [1]:

$$
\begin{aligned}
P_{Q,in} = \frac{\Delta^2}{12} \times [& \frac{\pi^6(-1+\epsilon_1)^6}{7OSR^7} + \frac{\pi^4\epsilon_1^2(-1+\epsilon_1)^4}{5OSR^5} \\
& + \frac{\pi^2\epsilon_1^4(-1+\epsilon_1)^2}{3OSR^3} + \frac{\epsilon_1^6}{OSR}] \qquad (3)
\end{aligned}
$$

with $\epsilon_1 = a_{int}/A_V \cong 1/A_V$. In order to minimize the additional noise caused by integrator leakage one can compute the critical DC-gain value where the excess parasitic noise degrades the signal-to-noise ratio (SNR) by 1 dB. For the 3rd-order modulator this critical gain is equal to:

$$
A_{V,1dB} \approx \sqrt{\frac{21}{5}} \cdot \frac{OSR}{\pi}. \qquad (4)
$$

Eq. (4) shows the minimum gain if only leakage is considered. Taking also distortion into account the required transconductance and bias current of the input transistors has to be much higher (Sec. 3.2).

3.2 Distortion

As far as distortion is concerned, primarily that of the first integrator has to be considered. Figure 2 shows the amplifier used for the first integrator. The dominant sources of distortion are the PMOS input devices which are biased in strong inversion. The third harmonic distortion of the first integrator yields [1]:

$$
HD_3 \approx \frac{\hat{V}_{in}^2}{64\ g_{m2}\ R_{in}^3\ I_{ds2}^2} \cdot (1 + \frac{R_{in}}{R_{dac}}) \qquad (5)
$$

[1] The nonlinear quantizer is modelled by a white-noise source and the NTF denominator is replaced by a constant gain term.

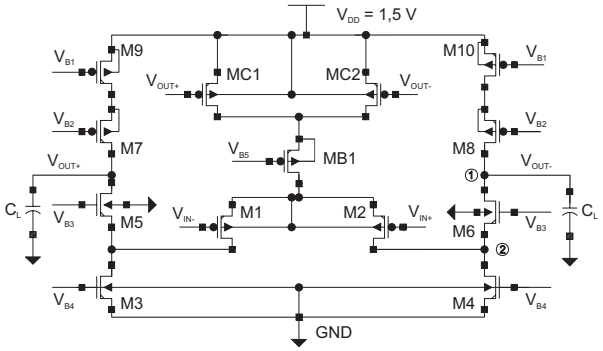

Figure 2: Schematic of the implemented amplifier.

Eq. (5) shows the effect on the harmonic distortion resulting from the input transconductance g_{m2}, the input resistance R_{in} and the bias current I_{DS2}. Furthermore, the bias current and the transconductance of the first integrator are determined by the dynamic range requirements of the overall A/D converter. This results in the following power consumption:

$$
P \approx \frac{V_{dd}\hat{V}_{in}^2}{4R_{in}} \cdot \sqrt{\frac{1}{g_{m2}\ HD_3} \cdot (\frac{1}{R_{in}} + \frac{1}{R_{dac}})}. \qquad (6)
$$

Power minimization can be done by increasing R_{in} up to the thermal noise limit in the same way as R_{dac}. Moreover, the power consumption is reduced by a large g_{m2}.

3.3 First Integrator Realization

Besides the DC-gain and distortion there are still further key design parameters for the first integrator (e.g. GBW or noise) and especially for low-voltage operation the input and output swing (IS, OS) is important, since $SNR \propto OS^2$. In order to combine the high gain and low- power requirements a single stage folded-cascode amplifier has been chosen (Fig. 2).

To enhance the OS of the used amplifier the transistors (M3-M10) have the same low $V_{DS,sat} = 100mV$ except the input devices (M1-M2). If the input transistors are biased in strong inversion they require twice as much $V_{DS,sat}$ [3], however for low-voltage circuit design operating in moderate inversion (MI) is recommended ($V_{DS,sat} \approx 0$) to enhance the input swing. The CMFB of an amplifier is a critical element in CT low-voltage/low-power applications, because it should not reduce the output swing and not considerable increase the power consumption. Accordingly, a simple CMFB with two transistors (MC1, MC2) biased in the triode region has been chosen. The complete simulation results are shown in Tab. 2.

4. LOW POWER CT $\Sigma\Delta$ MODULATOR

In a third order $\Sigma\Delta$ modulator the SNR is limited by circuit noise. Consequently, the ADC resolution can be calculated with the following relationships (Fig. 2). The input-referred

Table 2: Specifications of the first amplifier if the input transistors are biased in strong inversion (SI) and moderate inversion (MI).

	SI	MI
GBW $(C_L = 5pF)$	$4\ MHz$	$5.2\ MHz$
A_V	$70\ dB$	$72\ dB$
φ_M	80°	80°
$\bar{v}_{in,rms}$ $(inband)$	$43.8\ \mu V$	$31.6\ \mu V$
$V_{in,diff}$	$1\ V_{pp}$	$1.5\ V_{pp}$
ΣI	$80\ \mu A$	$80\ \mu A$

noise power density is approximately [2]:

$$S_i \approx 8kT(R_{in} + R_{DAC} + \frac{2\ n_f}{3\ g_{m2}}) \quad (7)$$

$$n_f = 1 + \frac{g_{m4}}{g_{m2}} + \frac{g_{m6}}{g_{m2}} \quad (8)$$

In (8) n_f describes the noise excess factor. Note that since the noise is not sampled until it has been filtered, the aliased noise components are attenuated by noise shaping. Therefore, the input-referred noise power that appears in the baseband is equal to:

$$\bar{v}^2_{in,therm} = S_i \cdot 2 \cdot f_B = S_i \cdot \frac{f_S}{OSR} \quad (9)$$

where f_B expresses the signal bandwidth. Substituting (7) into Eq. (9), and with $f_S = \frac{1}{T} = \frac{a_{int}}{RC}$ the input-referred noise power yields:

$$\bar{v}^2_{in,therm} = \frac{8kTa_{int}}{OSR\ R_{in}\ C_1}(R_{in} + R_{DAC} + \frac{2\ n_f}{3\ g_{m2}}). \quad (10)$$

The dynamic range of the $\Sigma\Delta$ modulator is determined by the ratio of the signal power and the circuit noise power ($\bar{v}^2_{in,therm}$).
Eq. (10) shows the different design parameters that can be used to obtain the required dynamic range.
Reducing the supply voltage demands a lower thermal noise contribution for the same DR. This requires smaller resistances (R_{in} and R_{dac} respectively) and a larger transconductance and consequently higher bias currents. Thus lowering the supply voltage in noise dominated circuits increases the power consumption.

5. SIMULATION RESULTS

The presented simulation result of the $1.5V$ 3rd-order CT $\Sigma\Delta$ modulator has been carried out for a sampling frequency of 1.6 MHz and a fixed OSR of 32, yielding a signal bandwidth of 25 kHz.
In order to verify the previously derived theoretical results, a behavioral simulation of the A/D converter has been done using MATLAB. The simulation considering the signal-to-noise-and-distortion ratio (SNDR) is shown in Fig. 3. The applied input signal frequency is 2.5 kHz and the inband noise is calculated from 500 Hz on. Moreover, Fig. 3 displays a peak SNDR of 63 dB and a dynamic range of approximately 75 dB. The maximum stable input signal is about -6.1 dB, respectively half of full-scale.

[2]In the following equations it is assumed that the amplifier has negligible flicker noise.

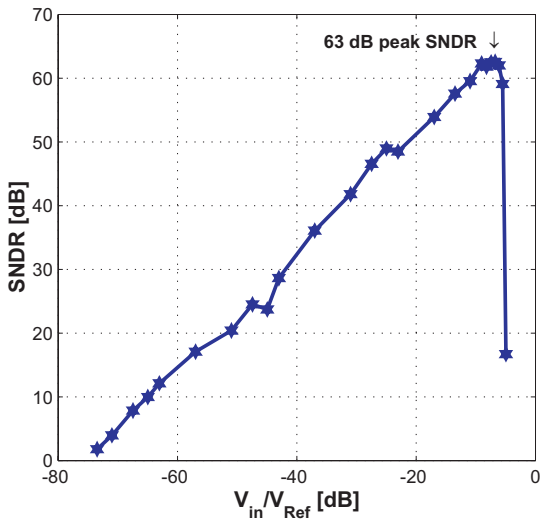

Figure 3: Simulated SNDR of the CT $\Sigma\Delta$ A/D converter.

The continuous-time third order A/D converter is implemented in a $0.5\mu m$, triple-metal standard analog CMOS technology, with $V_{Tp} = 0.58\ mV$ and $V_{Tn} = 0.62\ mV$.

6. CONCLUSION

A design strategy of a low-voltage/low-power third order continuous-time $\Sigma\Delta$ modulator has been presented. The implementation has been done without using a multi-threshold technology or voltage multiplication.
A standard method has been used to determine the integrator gains and feedback coefficients. The influence on circuit nonidealities like integrator leakage, distortion and noise on the overall A/D converter have been studied. Furthermore, the effects of low-supply voltages on the integrator as well as on the entire $\Sigma\Delta$ converter have been shown. The modulator has been designed in a $0.5\mu m$ CMOS technology. As a result the low-power consumption shows that the proposed implementation is a good alternative to DT realizations.

7. REFERENCES

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