Low-Power Sensing and Digitization of Cardiac Signals based on Sigma-Delta Conversion

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ABSTRACT
In this work we propose an architecture for the acquisition and digitization of cardiac signals in a pace-maker, based on $\Sigma\Delta$ modulation. Due to the characteristics of such an application, the proposed system presents the typical design challenges of low-voltage, low-power circuits. The work demonstrates that, thanks to the narrow bandwidth typical of biological signals (50-150 Hz), oversampling conversion techniques can be advantageous in terms of power dissipation at a given dynamic range. The converter is designed in a 0.8$\mu$m CMOS technology using the switched Op-Amp technique. The $\Sigma\Delta$ converter is a third order modulator with an oversampled frequency of about 8KHz and the circuit can operate at a minimum supply voltage of 2 V, while dissipating 2 $\mu$W at most. According to simulation results the dynamic range is larger than 50 dB.

1. INTRODUCTION
Modern pace-makers are responsive devices, meaning that in response to the sensed heart activity, they may trigger or inhibit a pacing pulse [1]. In this context, it is really interesting to insert an analog-to-digital converter (ADC) in the sensing chain: indeed such an approach allows to obtain the digitized version of the complete cardiac signals. This information can be easily post-processed by an embedded microprocessor, likely to be present in advanced pace-makers, increasing the pace-maker capabilities.

Considering that the frequencies of interest in cardiac pacemaking are in the range of 100 Hz, or even lower, the use of a $\Sigma\Delta$ converter becomes really attractive. Beyond the fact that this kind of converter supports the demand for a very low power consumption, coming from the constraint of an acceptable battery duration, the $\Sigma\Delta$ modulator can also be easily fully integrated. The chance to fully integrate the converter (as well as all the other building blocks), possibly on the same chip containing the digital logic, is desirable, since it allows to shrink the pacemaker size and to reduce its cost [2].

This work proposes an 8-bit sigma-delta ($\Sigma\Delta$) ADC [3] for a pace-maker sensing stage. The modulator is realized using Switched Capacitor (SC) circuits. Particularly the Switched Op-Amp (SO) [4] technique is used, in order to manage the typical impairments of low-voltage/low-power systems. Namely the modified SO technique has been exploited, in order to avoid any extra SC integrating stage [4]. The system is designed in a standard 0.8$\mu$m CMOS technology, can operate with a supply voltage down to 2V and dissipates 2 $\mu$W.

The paper is organized as follows: Section 2 introduces the characteristics of the converted signal and presents the ADC architecture. Section 3 describes the circuit design, while the simulation results are discussed in Section 4. Finally conclusions are presented in Section 5.

2. THE $\Sigma\Delta$ CONVERTER
The heart signal, delivered by the catheter, has a peak value within a voltage range from 100$\mu$V up to 4mV. It is therefore necessary to amplify such signal before the conversion is performed. This task is realized by two blocks: the first is a fixed-gain low noise pre-amplifier, which multiplies the input signal by a factor of about 100. The second block is a variable gain amplifier (VGA), whose task is to reduce the wide range of variation of the signal peak. The VGA has three possible settings, constraining the signal peak within $V_{FS}$ and $V_{FS}$/4, where $V_{FS}$ is the full-scale voltage of the $\Sigma\Delta$ converter.

While the fixed-gain pre-amplifier can be conceptually considered a separate block, although integrated on the same chip, and it is not treated in this paper, the variable gain amplification has been actually included in the $\Sigma\Delta$ modulator. Finally it is worth to specify that significant cardiac signal components are within a bandwidth of 150Hz.

2.1 The $\Sigma\Delta$ modulator design
The most important step in the $\Sigma\Delta$ ADC design is of course the design of the loop transfer function. This has been done imposing the desired mask for the noise transfer function (NTF) [5]. Considering the required 8 bit resolution a modulator of second or third order should be effective [3]. In fact, according to simulations, a second order modulator matches
the required resolution with a very tight safety margin. As a consequence we chose to implement a third order modulator, which is also more robust with respect to spurious tone in the modulated signal spectrum.

The stability of the modulator, whose characteristics are summarized in Tab. 1, has been checked by means of the root locus. In this way an in-band quantization noise attenuation, which corresponds to a stable poles configuration, has been imposed.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
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<tbody>
<tr>
<td>Sampling freq.</td>
<td>8.192 KHz</td>
</tr>
<tr>
<td>Order</td>
<td>3</td>
</tr>
<tr>
<td>Oversampling ratio</td>
<td>16</td>
</tr>
</tbody>
</table>

Table 1: main characteristics of the designed modulator

2.2 The decimator design

The decimator filter is a critical block, because a real decimator will not completely suppress the shaped quantization noise, hence the ADC resolution depends on the decimator architecture, too.

The typical sinc filter has been used; this kind of decimator can indeed be realized using comb filters that can be particularly simple, from the system point of view [3], allowing to minimize the power consumption. The main drawback of the sinc filter is that an attenuation in the signal band is present. In order to make this effect negligible, the final rate of the converter has been fixed at 512 Hz, which is about twice the lower limit imposed by the Nyquist theorem.

Fig. 1: circuit schematic of the converter

3. CIRCUIT DESIGN

The circuit design of the ADC proposed in Section 2 has been developed in a pure 0.8μm CMOS technology. It is well established that SC circuits are a suitable approach for the realization of the discrete-time loop filter of the ΣΔ converter. However, as mentioned in the Introduction, in the considered application the typical problems related to low voltage are present. For this reason the SO technique has been used [4]. It is worth to stress out that SO architecture requires to add extra SC integrating stages, unless the realized system is composed by the cascade of non-inverting (with delay) and inverting (with delay) integrators [4]. Since the extra power consumption introduced by the added stages would make the SO approach impractical, an architecture that satisfies the mentioned criterion has been chosen among the possible schemes for the implementation of the loop filter. Namely a CRFBD [3] architecture, whose circuit realization is depicted in Fig. 1, has been used. The SO schematic of Fig. 1 is drawn as a single ended circuit for the sake of clarity only, but the actual circuit is fully differential.

Fig. 2: circuit schematic of the OTA

The ratio between the capacitors reported in Fig. 1 is, of course, fixed by the loop filter transfer function; however it is important to remind that the ADC has to include a VGA at its input. This is obtained by making all the three capacitors (C1, C2, C3) connected to the input signal variable. Namely these capacitors can be programmed to three different values, according to the requirements for the VGA.

Although at this point the ratio between the capacitors are clearly defined, a suitable value for the reference capacitor, i.e. the feedback capacitor of the SC integrators, has to be chosen. Of course this has to be fixed as the best trade-off between the power consumption, increasing with the capacitor size, and the KT/C components of the circuit noise. Considering the limit of a supply voltage of 2V, imposed by the exhausted battery, the full scale voltage has been fixed to 2Vpp differential. Given this value, our calculations [5] and simulations (see Section 4) show that a good value for the integrating capacitor (C1) of the first stage is 0.6pF. The noise introduced by the following stages is also partially shaped by the modulator NTF, indeed an integrating capacitor of 0.4pF and 0.3pF for the second and third integrator respectively can be used. It is worth to note that these di-
5. CONCLUSIONS
This work has presented an 8-bit ΣΔ ADC converter for a pace-maker sensing stage. The typical challenges of low-voltage/low-power circuits have been faced, in the system integration on a 0.8μm CMOS technology, using the SO technique. Furthermore the realized ADC includes a VGA at its input. According to simulation results, the third order modulator, clocked at an oversampled frequency of about 8KHz, performs a dynamic range of 50 dB, considering the effects of a real decimator and of the main circuit impairments. Finally the converter can operate with a supply voltage down to 2 V, while it dissipates 2 μW, at the maximum battery voltage of 2.8V.

6. ACKNOWLEDGEMENTS
Authors would like to thank D. Dario for performing some simulations and Prof. E. Zanoni for useful discussions. The clarifications on pacing systems by A. Mozzi and L. Lentola from Medico S.p.A. are also acknowledged.

7. REFERENCES

Figure 3: spectrum of the modulator output signal

Figure 4: effect of the thermal noise and of the capacitor variations on the SNR curve

Table 2: main results of OTA simulations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>V_{DD}</td>
<td>2.8 - 2 V</td>
</tr>
<tr>
<td>settling time</td>
<td>39 μs</td>
</tr>
<tr>
<td>settling error</td>
<td>0.3%</td>
</tr>
<tr>
<td>current per stage</td>
<td>300 nA</td>
</tr>
<tr>
<td>Voltage Swing</td>
<td>&gt; 2V_{pp}/fiff</td>
</tr>
</tbody>
</table>

The spectrum of the signal before decimation is reported in Fig. 3. The achieved noise shaping is apparent; particularly the zero in the NTF around 120Hz can be singled out.

The effect of two additional impairments, i.e. noise and capacitor mismatch, has been tested via an high-level model of the whole converter, developed in MATLAB. Equivalent noise sources have been added at the input of each integrator, while a random variation on the filter coefficient has been considered.

The SNR curves resulting from this Monte Carlo simulation are reported in Fig 4. A maximum error of 3% on the capacitor ratio, which is actually worst than the precision usually obtained from standard processes has been considered. Anyway the designed ADC performs a DR greater than 50 dB, therefore the target of 8-bit resolution is achieved.