Low-Power Digital Filtering Using Multiple Voltage Distribution And Adaptive Voltage Scaling

Sandeep Dhar and Dragan Maksimović
Department of Electrical and Computer Engineering
University of Colorado, Boulder, CO 80309-0425

http://ece-www.colorado.edu/~pwrlect
{dhar,maksimov}@colorado.edu

ABSTRACT
This paper describes an adaptive power management architecture to reduce power consumption in digital filters. The proposed approach combines two low-power techniques which utilize supply voltage reduction. The first technique, multiple voltage distribution (MVD), attempts to reduce power consumption by assigning reduced supply voltages to circuit modules while satisfying timing constraints. The second technique, adaptive voltage scaling (AVS), dynamically adjusts these multiple voltages to meet throughput requirements resulting in further power reduction. An FIR filter application using the combined MVD-AVS power management scheme for two adaptively scaled supply voltages is shown to consume one-third the power of a fixed supply voltage scheme, and half the power consumed with a single supply AVS.

1. INTRODUCTION
The strong demand for low-power computing has been driven by a growing class of portable, battery-operated applications that demand increasing functionality. Digital signal processing is pervasive in such applications and digital filtering is often used. Use of multiple supply voltages [1, 4] and adaptive adjustment of supply voltage levels [2, 5] have been introduced as effective circuit-level techniques to reduce power consumption. The contribution of this paper is to introduce the theory and concept of an optimal power management scheme, utilizing a combination of multiple voltage distribution (MVD) and adaptive voltage scaling (AVS).

2. FIR FILTER APPLICATION
Fig. 1 shows a modular block diagram of a tapped delay line finite impulse response (FIR) filter implementation. The multipliers (adders, delay elements) are identical in the structure (though this is not a restriction). Input to the filter is at a fixed data rate $f = 1/T$ which determines the computation latency. The coefficients to the filter, determined by symmetric windowing of ideal filter impulse responses are assumed fixed. This allows for lower order filters to be configured as subsets of higher order filters and for the filter order $N$ to be adjusted by means of SEL1 and SEL2. Such an approach leads to frequency selective solutions where for the same cutoff frequency, the stopband energy of the filter output is kept below a specified threshold while $N$ is minimized. This was described in [3] which also proposed an approximate method of determining the filter order from the input data. Having an on-chip filter structure implementation with a large $N$ consumes substantial chip area. Chip area can be traded for increased power consumption by designing a reusable filter architecture as shown in the block diagram of Fig. 2. Here the idea is to reuse the multiplier and adder hardware to mimic a tapped delay line filter. An internal clock generator runs at a frequency $N_f/N_r$, where $N_r$ is the order of the reusable filter. Filter coefficients are pre-assigned and can be stored in a ROM array. The input signal memory array (which corresponds to the delay elements of a tapped delay line filter) presents the appropriate input values to the filter arithmetic block at a rate of $N_f/N_r$.

2.1 Energy Model
The average energy consumption, $E^N$ of a tapped delay line FIR filter of order $N$ can be expressed as

$$E^N = \sum_{i \in add} C_i E_i + \sum_{i \in shift} C_i E_i + \sum_{i \in delay, logic} C_i E_i$$

where $E_i$ is the average energy consumption of a module and $C_i$ is the number of times a module is used for computation.
in time $T$. $C_i = 1$ for the tapped delay line filter. To apply MVD or AVS to the filter we need to model the average energy consumption $E_i$ of a circuit module as a function of delay $d_i$:

$$E_i = F_i(d_i)$$

To obtain a realistic model a 8 bit multiplier and a 8 bit carry look ahead adder were implemented in a standard CMOS technology. Using a model extracted from layout, extensive simulations with random input vectors were done to evaluate an averaged energy consumption value at a particular $V_{DD}$. This was repeated for various $V_{DD}$ between 1 V and 3.3 V. The results were graphed against the worst-case module delay giving an energy-delay plot. The energy-delay model relating average energy consumption and delay for a module is assumed to be:

$$E_i = \frac{K_i}{d_i - d_{O_i}} + E_{O_i}$$

where $K_i, d_{O_i}$, and $E_{O_i}$ are chosen for a close fit to the energy-delay curves.

3. **POWER MANAGEMENT TECHNIQUES**

Scaling down the energy consumption (reducing supply voltage levels) results in longer delays. The circuit techniques in this paper attempt to reduce the total average energy consumption $E^N$ while satisfying the timing constraints.

3.1 **Power down of filter structure**

A power reduction technique by dynamically adjusting the filter order with fixed values for the filter coefficients was presented in [3]. Power down can be done by either the external supply voltage distribution or by gating the clock to selected taps. For phase linearity to be maintained power down is to be applied equally at both ends.

3.2 **Adaptive Voltage Scaling with power down**

Further improvement over the simple power down scheme for a variable order filter is possible by adaptively scaling the supply voltage. The computation requirement is decreased with a reduced filter order allowing more delay per module. The energy-delay model indicates that an increased delay allows for reduced energy consumption.

3.3 **MVD and AVS with power down**

The tapped delay line filter structure can be readily exploited towards the use of multiple supply voltages. As seen from Fig. 1, the critical path for a filter of order $N$ consists of the multiplier for the first filter tap, a chain of $N$ adders and the output multiplexer. At adder $A_2$, signal $X_2$ has an arrival time $t_{a2}$ greater than signal $Y_2$ ($t_{a2}$). This implies that multiplier $M_2$ can operate at a lower supply voltage satisfying $t_{b2} = t_{a2}$. Applying the same reasoning to all filter taps, we see that multiplier supply voltages are successively reduced down the tapped delay line to satisfy $t_{b_i} = t_{a_i}$. Since the energy consumption ($E \propto V^2$) in a multiplier, $E_{mult}$ far exceeds that of an adder, $E_{add}$, this results in reduced power consumption.

3.3.1 **Optimal assignment of voltages**

The problem of multiple voltage scheduling (MVS) [1, 4] is the assignment of multiple supply voltages to a circuit, from a given set of fixed voltage levels. This problem was shown to be NP-complete. We instead consider a simpler problem of multiple voltage distribution (MVD) that allows multiple supply voltages to take any value within a given voltage range. MVD is a constrained optimization problem which can be formally defined as follows: minimize $\sum_{i=1}^{m} E_i$ for $m$ modules along $p$ distinct paths from inputs to outputs, where the path delay $D_j = \sum d_i$, $d_i \in \text{path } j$ is subject to the timing constraints $D_j = T$, $j = 1, 2, ..., p$. Here $d_i$ is the delay of module $i$. This problem can be analyzed by setting up the Lagrangian,

$$G(d_i, \lambda_j) = \sum_{i=1}^{m} F_i(d_i) + \sum_{j=1}^{p} \lambda_j (T - D_j)$$

(4)

The method of Lagrange multipliers ($\lambda_j$) reduces (4) to a system of $(m + p)$ algebraic equations which are solved for ($\lambda_j, d_i$). Thus,

$$\frac{\partial G}{\partial d_i} \equiv \frac{\partial F_i(d_i)}{\partial d_i} - \sum_{j=1}^{p} \lambda_j \frac{\partial D_j}{\partial d_i} = 0$$

(5)

where $i = 1, 2, ..., m$ provide $m$ algebraic equations, and

$$\frac{\partial G}{\partial \lambda_j} \equiv (T - D_j) = 0$$

(6)

where $j = 1, 2, ..., p$ provide $p$ path constraint equations.

Here it is assumed that the $p$ path constraints used allow a solution to be found. Optimal voltage assignments $V_{DD,i}$ to the modules are then obtained as a function of the solved delays. For a given filter order $N$, the algorithm finds a set of $2N + 1$ optimal supply voltages. Starting from an initial assignment of $V_{DD,i}$, AVS is then applied to each $V_{DD,i}$ as $N$ varies, such that for each $N$ the supply voltages are maintained at the optimal values determined by the algorithm.

3.3.2 **MVD-AVS with two supply voltages**

A general MVD-AVS scheme as described above will have the lowest possible energy consumption for a given filter architecture that can be used as a reference for other schemes utilizing supply voltage reduction. However having individual and different $V_{DD,i}$ for each circuit module may not be practical. Hence it is useful to compare these results to a MVD-AVS scheme with only two supply voltages. Solving the optimization algorithm for $2N + 1$ voltages of the FIR filter showed that the optimum multiplier voltages had a
Figure 3: Variation in optimum supply voltage assignment for two adaptively scaled voltages, $V_{DD,1}$ and $V_{DD,2}$, as a function of filter order, $N$.

Figure 4: Average power consumption $P$ vs. filter order, $N$ for different power management techniques of,
(a) power down of filter taps with a fixed supply voltage,
(b) AVS with a single supply voltage,
(c) MVD-MVS with 2N+1 supply voltages,
(d) MVD-MVS with 2 supply voltages.

very small difference of values across filter taps. Hence for the two supply voltage scheme it is practical to assign $V_{DD,1}$ as the supply voltage to all multipliers, delay elements and control logic and $V_{DD,2}$ as the supply voltage to all adders and the output multiplexer. The optimization problem applied to the two supply voltage case requires the solution of:

$$\frac{\partial G}{\partial d_i} = \frac{\partial F_i(d_i)}{\partial d_i} - \lambda \frac{\partial D_{crit}}{\partial d_i} = 0,$$

(7)

$$\frac{\partial G}{\partial \lambda} \equiv (T - D_{crit}) = 0,$$

(8)

where $D_{crit}$ is the path delay along the critical path of the filter and is given by (cf. Fig. 1):

$$D_{crit} = d_{MO} + \sum_{i=1}^{N} d_{A_i} + d_{MUX}$$

(9)

Fig. 3 shows the assignment of supply voltages $V_{DD,1}$ and $V_{DD,2}$ obtained by applying the algorithm for various $N$.

4. COMPARISON RESULTS

Fig. 4 shows the average power consumption for the different power management techniques. The data rate $f$ was

Figure 5: Power consumption vs. filter order $N$ for a reusable tapped delay line filter configuration of order, $N_r = 10$, for different power management techniques of,
(a) fixed supply voltage,
(b) AVS with a single supply voltage,
(c) MVD-ABS with 2N+1 supply voltages,
(d) MVD-ABS with two supply voltages.

assumed to be fixed at 1.25 MHz. The filter order was varied from $N_{min}$ to $N_{max} = (10, 100)$ in steps of 10. Curve (a) corresponds to a simple power down structure (cf. Section 3.1) with a fixed $V_{DD}$ of 2.38 V satisfying timing constraints at $N = 100$. Curve (b) corresponds to a single supply voltage AVS (cf. Section 3.2) with the supply voltage adaptively adjusted from 1.31 V to 2.38 V. Curve (c) corresponds to a combination of MVD and AVS, the result of applying 2N+1 supply voltages obtained by the optimization algorithm (cf. Section 3.3.1). Of interest is curve (d) which represents a practical implementation for MVD-ABS with two supply voltages. It shows only a small penalty compared to the optimum MVD-ABS scheme. For $N = 60$ this scheme takes 66% less power than a fixed voltage scheme and 45% less power than AVS (losses in power supplies ignored).

Fig. 5 shows the power consumption using a reusable filter (cf. Fig. 2) of order $N_r = 10$ with different power management techniques: (a) fixed supply voltage, (b) single supply AVS, (c) MVD-ABS scheme with 2N+1 supply voltages and (d) MVD-ABS with 2 supply voltages. Even with substantially increased power levels, a MVD-ABS scheme shows its advantages over the other two techniques.

5. REFERENCES


