"Cool Low Power" 1 GHz Multi-Port Register File and Dynamic Latch in 1.8 V, 0.25 μm SOI and Bulk Technology

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ABSTRACT

This paper describes power analysis at sub-zero temperatures for a high performance dynamic multiport register file (6 Read and 2 Write ports, 32 wordlines x 64 bitlines) fabricated in 0.25 μm Silicon on Insulator (SOI) and bulk technologies. Based on the hardware it is shown that the performance of both register file and latch improves by 2-3.5% per 10^0 C reduction in temperature. The standby power for SOI reduces by 1.5% to 3% per 10^0 C temperature drop down to -30^0 C. The SOI chip is shown to have more significant performance improvement at low temperatures compared to bulk chip due to the floating body effect which partially offsets the increase in the threshold voltages (Vt). The low temperature performance gain is attributed to reduction in capacitance (around 7-8%) and rest is due to dynamic threshold voltages. At -30^0 C the register file is capable of functioning close to 1.02 GHz for read and write operations in a single cycle.

I. INTRODUCTION

Recently SOI has emerged as a technology for mainstream digital applications as the bulk silicon technology is approaching scaling limits rapidly [1, 2]. Partially-depleted SOI offers reduced source-to-drain resistance and dynamic threshold voltages which result in higher performance over fully depleted SOI technology. Also the process and device designs for partially depleted SOI are much more compatible with the bulk CMOS. However, the floating body in partially depleted device can accumulate or lose charges. This causes high device leakages during standby or in the high temperature burn-in conditions. The amount of charge in the body depends on the initial conditions of source, drain and gate of the device. This results in variable body potentials and dynamic threshold voltages which cause variable device delays known as "history effect". Such SOI specific issues pose multitudes of design challenges. Especially dynamic circuits are very sensitive to such process variations which can result in inter or intra macro timing problems, race conditions, high leakages/power and reduced noise margins.

In this work for the first time we have analyzed the power of a register file and evaluated the performance and history effect as a function of temperature down to subambient temperatures. Also we have proposed modification of power equation to account for collision power for "self resetting" circuits due to race conditions especially at higher frequencies. In addition, we have quantified the performance gain of SOI over bulk due to junction capacitance reduction and dynamic threshold voltages. The history effect is shown to be significantly reduced at sub-zero temperatures. We have demonstrated that using SOI the power consumption is reduced by 7-8% compared to bulk technology at low temperatures. The analysis used in this paper can be very well extended to other circuit families.

II. CIRCUITS

Here we concentrate mainly on the analysis of performance power, and history effect especially at low temperatures using 0.15μm Leff SOI technology.

The main components of register file are shown in Fig. 1 [3]. The general functioning of the register file takes place by writing the data into a single ended cell by triggering the write wordline. The data is read by muxing the data from the cell with the read wordline of the selected port. Since the input of the register file is dynamic the chopping function provided in Fig. 1 by means of reset renders the output pulses with the desired pulsewidth. The dynamic output of the register file is converted to static by a dynamic latch. For the proper functionality of the latch and the register file the inputs are in "standby" when they are "high" and active when they are "low".

III. HARDWARE AND SIMULATION RESULTS

The register file, designed in bulk, is fabricated in a 1.8 V, 0.25μm bulk and SOI technology with Leff of 0.15 μm and gate oxide of 40 nm and 5 levels of Aluminum wiring. The partially-depleted SOI device and its model (used for simulation) is shown in Fig. 2. The register file with area 1.5 mm x 1.8 mm is measured using HP83000/F660 tester and is shown to be fully functional down to sub-zero temperatures.

The total simulated power including one read and write port along with arrays and I/O is calculated at -30^0 C, 1.9V, 1 GHz. The total power is around 332 mW and shows a slight increase (3-4%) over room temperature.

The total simulated power can be used to correlate the measured values. The measured total power can be best
analyzed through power equations. Conventionally the total power \( P_{\text{total}} \) can be written as a function of \( V \) and \( f \) [4].

\[
P_{\text{total}} = P_d + P_{\text{sc}} + P_s + P_{\text{dpc}} \quad (1)
\]

The dynamic power is given by

\[
P_d = \frac{1}{2} f C V^2_{dd} \quad (2)
\]

Where \( f \) is the frequency, \( C \) is the capacitance, \( P_{\text{sc}} \) is the short circuit power which is small at low voltages and small transition times and \( P_s \) is the leakage power in standby mode (i.e when \( f=0 \)). For "self-timed" or "self-resetting" circuits the above equation can be modified to include pulse-collision power \( P_{\text{dpc}} \). When evaluation and precharge are active simultaneously due to timing mismatchs there is a direct path between the supply voltage and ground. This may occur at high frequencies especially beyond the operating range of the circuit or if the circuit is mapped from one technology to another technology. At this point the total power may deviate from the linear regime of power-frequency curve. Thus with the modified term the equation can be written as follows:

\[
P_{\text{total}} = P_d + P_{\text{sc}} + P_s + P_{\text{dpc}} \quad (3)
\]

The simulated average power due to pulse collisions is shown in Fig. 3a. As the frequency approaches to 1 GHz the total power actually deviates from linear regime (power vs. frequency curve). Due to collisions the evaluation "nfet" transistors have to fight against the "simultaneous" precharging of the node resulting in larger transition times and thereby larger access times. Fig. 3b shows exactly the same effect. As the frequency approaches to 1 GHz the access time increases which is an indication of pulse collisions. The simulation data (not shown here) further proves the point that indeed the collision occurs at the read wordline and its reset. At that point the drop in power from the linear curve can be attributed to power loss due to collision.

Power of SOI and bulk wafers is compared using chips with similar room temperature leakages. The power analysis of such chips at \(-30^\circ\) C is shown in Fig. 4. A power reduction of 7-8% for SOI is observed over bulk above 400 MHz. Below 400 MHz bulk power is slightly smaller. This is because as the temperature is lowered the \( V_t \) of bulk device increases (because the Fermi levels move towards the band edges) and the sub-threshold slope improves. Thus the leakage for bulk device decreases significantly with the lowered temperature. On the other hand for the SOI device the dc equilibrium body potential increases slightly by lowering the temperature. For example consider nmos (device model shown in Fig. 2) with the gate "low" and drain at "Vdd". Its equilibrium body voltage is determined by the balance of the back-to-back drain-to-body diode and the body-to-source diode. As the temperature is lowered the reversed-biased drain-to-body diode has a relative weak temperature dependence, while the forward biased body-to-source diode has a negative temperature dependence (i.e its \( V_{FB} \) increases for the same diode current). The increase in the body voltage for SOI device at lowered temperature offsets a portion of the increase in \( V_t \), thus resulting in lower \( V_t \) and higher leakages compared with the bulk device. As a result the standby power for SOI is slightly higher resulting in the cross-over point in the power vs frequency curve.

The performance (access time for register file and CLKG to latch out ) of bulk and SOI is compared at \(-30^\circ\) C with chips having similar room temperature leakages at standby conditions. (Fig. 5a and b). Access time gain of 20% for register file (from the least significant bit "RB2<4>" to the output "OB2<0>") and CLKG-DD<0> delay of 19% is realized for dynamic latch in SOI compared to bulk. The cycle time for read and write operation in the same cycle for SOI is around 1.02 GHz at \(-30^\circ\) C. Also the access times as low as 480 ps are achieved for "faster" SOI chips. The enhanced performance improvement of SOI over bulk at lowered temperature is primarily due to the less \( V_t \) increase from the earlier discussions.

The access time is plotted as a function of temperature in Fig. 6. The improvement in the access time is around 3.4% over a decade of temperature drop compared to 1.6% per decade of temperature for the bulk.

The performance improvement can be attributed quantitatively to two factors - capacitance reduction and dynamic \( V_t \) changes. Following method is adopted to differentiate the effects of these two on the performances. Assuming non-collision regime (i.e linear regime, \( P_{\text{dpc}} = 0 \)) and small transition times ( \( P_{\text{sc}} = 0 \) ) the equation (2) can be written as follows

\[
P_{\text{total}} = \frac{1}{2} f C V^2_{dd} + P_s \quad (4)
\]

Thus the slope of \( P_{\text{total}} \) vs \( f \) line gives the value of

\[
\frac{1}{2} f C V^2_{dd} \quad (5)
\]

For SOI,

\[
C_{\text{soi}} = C_w \quad (6)
\]

while for bulk,

\[
C_{\text{bulk}} = C_w + C_d \quad (7)
\]

where \( C_w \) - capacitance due to wire and \( C_d \) - capacitance due to devices. Subtracting (6) from (7) gives the net reduction due to \( C_d \). By comparing the slopes of power-frequency curves for bulk and SOI chips at a fixed \( V_{dd} \) the reduction in the device capacitance can be obtained. This value is directly related to the performance gain. From the slopes a reduction of 7-8% in capacitance is observed for SOI chip. The rest of the gain is attributed to dynamic \( V_t \) of SOI due to charge accumulation. Using the same analysis it is to be noted that the reduction
in capacitance (i.e. derived from the slopes of power frequency curves (not shown) changes marginally from room temperature down to sub-zero temperatures (i.e. 0.3, 0.50 and 0.8 mW/MHz for 1.5 V, 1.9 V and 2.3 V respectively). This indicates that the reduction of junction capacitance in the case of SOI remains unchanged across the temperature.

The access time is plotted as a function of frequency for various temperatures (Fig. 7). This indicates the history effect i.e. the variation of delays depending on the charge accumulation and discharge in the body. For higher temperatures (85° C) at 1.9 V the history effect is close to 12-13% while at lower temperatures (−30° C) it drops to 3-4%. This is because at the lowered temperature, the impact ionization current (which charges the body) decreases, the reversed-biased drain-to-body junction current (which charges the body) remains relatively constant and the forward-biased body to source junction current (which discharges the body) decreases due to increased diode idealities. Thus the net charges gained/lost through a switching cycle is reduced. The smaller amount of body charge can be readily removed/restored even at high frequencies resulting in less history effect.

IV. CONCLUSIONS

Power, performance and history effect are analyzed for dynamic multi-port register file and latch (mapped in SOI) at sub-zero temperatures. It is demonstrated that the leakage power can be significantly suppressed for SOI with the gain in access time and cycle time. The substantial performance improvement of SOI over bulk chip at lower temperatures is related to the floating body effect which partially offsets the Vt increase. The history effect for register file fabricated in SOI is significantly reduced at lower temperatures. Register file speeds over 1.02 GHz are demonstrated at −30° C with access time as low as 480 ps.

REFERENCES

Fig. 3b Simulation data showing increase in access time as a function of frequency.

Fig. 4 Power vs. frequency for bulk and SOI at -30°C.

Fig. 5a Comparison of performance for dynamic register file and latch at -30°C using SOI chips.

Fig. 5b Comparison of performance for dynamic register file and latch at -30°C using bulk chips.

Fig. 6 Performance vs. temperature for SOI.

Fig. 7 History effect at different temperatures.