A Micro-Power Mixed Signal IC for Battery-Operated Burglar Alarm Systems

Silvio Bolliri
Microelectronic Laboratory,
Department of Electrical and Electronic Engineering
University of Cagliari
Cagliari, Italy
bolliri@diee.unica.it

Paolo Porcu
ELSA SPA - Security Systems
Cagliari, Italy
paoloporcu@tiscalinet.it

Luigi Raffo
Microelectronic Laboratory,
Department of Electrical and Electronic Engineering
University of Cagliari
Cagliari, Italy
luigi@diee.unica.it

ABSTRACT

The design of the standard CMOS IC core of a commercial wireless burglar alarm system is presented as an example of a very low-power analog VLSI design for battery-operated systems. The main constraint is battery life, which must be at least five years (with standard camera-battery). The chip is composed of a digital (decision) part and an analog interface with sensors. The entire chip absorbs 10 μA. Measures on each single component and test on working environment show full functionality and complied with specifications. Even though the example is application specific, the design solutions and each single element can also be utilized in many other battery-operated low-frequency devices (e.g. environmental parameter monitoring).

1. INTRODUCTION

In this paper we consider the design of a mixed signal ASIC for a battery-operated burglar alarm system developed to upgrade a commercially available product. The main constraint is battery life, which must be at least five years. In such situations, each part of the circuit must be optimized to achieve the objective. In particular, we must limit performances to the minimum required by the specifications (in terms of precision, stability, adaptability, etc.) to reduce power consumption [8].

In the design description that follows, the critical analog parts of the ASIC are reported starting from the specifications. These circuits have been designed to limit any power consumption not strictly needed to comply with specifications.

The basic device must be able to receive input signals from an IR sensor, process and recognize it as an alarm. To consider the use of the chip in other situations the device should be able to work also with shutter sensor, magnetic perimetrical sensor and ON/OFF signals in general.

An analog interface translates the IR signal into an ON/OFF signal processed by the digital part. The digital part tries to remove false alarm with specific statistical algorithm and translate the signal for the transmitter. The signal transmitted is composed of the replica of a string of bits containing an unique identification code stored in a PROM and the kind of alarm. Proper periodic life-signals should be transmitted to the central unit.

2. SPECIFICATIONS

In stand-by conditions (no alarm) the IR sensor output signal has a constant value of about 0.6 V but this value may vary between 0.3 and approximately 1 V. When a heating source (e.g. a human body) passes in front of the IR sensor an impulse is generated. A signal is considered a valid alarm when its amplitude is greater than about 0.35 mV. The impulse frequency is given by the speed at which the heating source passes in front of the IR sensor. Considering the application and typical speed of human (burglar) movements a signal is considered a valid alarm when its frequency is in the range 0.15-12 Hz.

The IR output impedance is about 10^5 Ω.

The digital part needs a 5 kHz clock. Precision with such a value is only required to have a transmission time reference and to schedule periodic operation (e.g. life signal transmission). According to these tasks, a 30% precision setting is required. There are no constraints on the duty cycle.

The circuit must be able to work with a power supply voltage that ranges from 4 to 6 volts. The ASIC must detect when the power supply voltage falls below 4.25 $\pm$0.25 V.

In working condition the whole ASIC (analog and digital part) must absorb a maximum of 15 μA, but a smaller value is desired and strongly recommended.

3. SYSTEM OVERVIEW

Fig. 1 shows the schematic diagram of the ASIC's analog part. It consists of three parts: a signal processor (SP), a clock generator (CKG) and a power supply monitor (SM).

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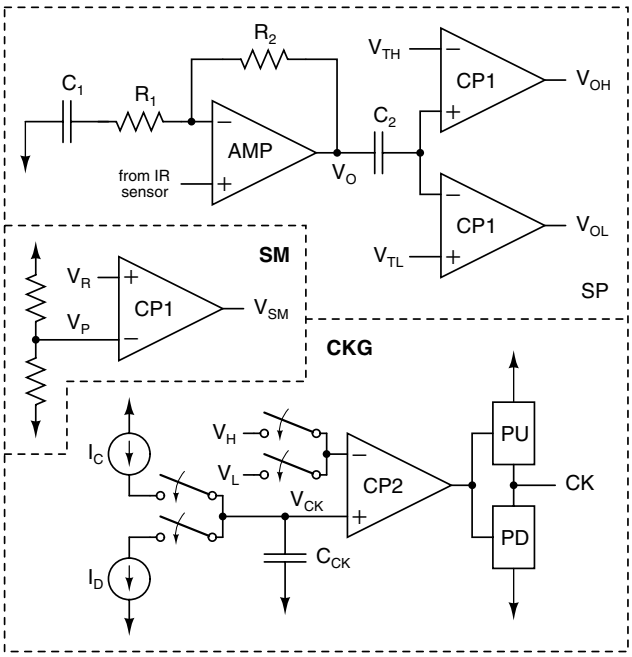

Figure 1: Schematic diagram of the ASIC's analog part.

The signal processor pre-amplifies the IR sensor signal and detects if it has the characteristics (amplitude and frequency) to be considered a valid alarm. The clock generator creates the clock needed by the digital part of the ASIC. The power supply monitor detects when the battery charge is low and must be changed.

Due to power consumption specifications, each of these parts required specific circuit solutions.

3.1 Signal Processor

The signal processor consists of two blocks: a processing and a detection unit. The first (AMP with feedback network) acts as: (a) an interface with the high impedance IR sensor output; (b) a filter to remove very low frequency components (less than 0.3 Hz) and higher frequency interference; (c) an amplifier to make the signal suitable for detection. The second is a window comparator.

To meet the requirements the IR sensor is directly connected to the non-inverting input of the amplifier. Amplification is performed through a resistive feedback network R_1 and R_2 while C_1 determines the low cut-off frequency (0.15 Hz). The high cut-off frequency is determined by the inner capacity of the AMP. The capacitor C_2 removes the DC component of the amplified signal (including the offsets) and centers it into the comparator window.

The amplifier gain is determined by the minimum value that the window comparator can safely detect. In this case a valid alarm (amplitude 0.35 mV) must be amplified to about 50 mV. This implies a closed loop gain of 145.

The low cut-off frequency (0.15 Hz) is determined by R_1C_1. To realize such a small cut-off frequency the capacitor C_1 must be around the μF and cannot be implemented on-chip.

The amplifier must be able to drive the resistive feedback network and must have a low current consumption. In literature many solutions [4, 7, 10, 5, 11] have been implemented to solve this problem.

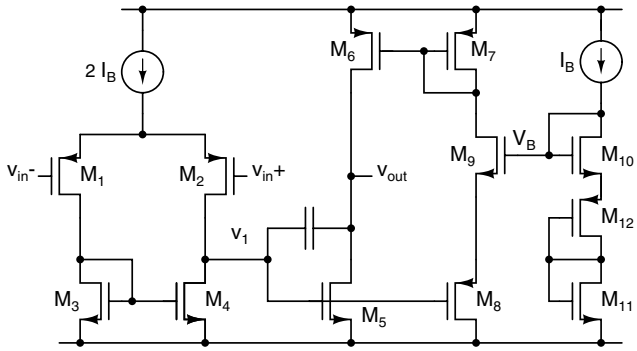

Figure 2: Amplifier schematic circuit.

Fig. 2 shows the schematic circuit of the amplifier used. Its architecture is similar to the Miller OTA but has a second stage with active bias. The active bias of transistor M6 is performed by means of the voltage V_B-V_1 across the gate-source voltages of transistors M_8 and M_9. The constant voltage V_B is generated by means of the three diode connected transistors M_{11}=M_4, M_{12}=M_8 and M_{10}=M_9. Without signal the same amount of current flows through M_5 and M_6. When a signal is applied and the first stage output V_1 goes down, the voltage V_B-V_1 increases, as well as the current flowing through them (and, consequently, through M_6). The output current I_6-I_5 varies exponentially according to the voltage V_1 (because of the control by means of the gate-source voltages of M_5, M_8 and M_9). In this way the amplifier can drive very high current not only as a sink (through M_5), like the Miller OTA, but also as a source (through M_6). This behaviour allows for a very small bias current. The current is increased only when needed. In this manner it is possible to drive the load of the feedback network.

In principle the amplifier must be stable in every working condition. In our application the amplifier is used only in a closed loop configuration, so open loop stability is not really needed. From this observation we can limit the power consumption even further: setting the 60° phase margin limit to only closed loop gain greater than 10, we can use a bias current I_B of only 100 nA, thus reducing the power consumption.

The comparators that form the window comparator consist of a simple OTA with 10 mV of hysteresis.

3.2 Clock Generator

The circuit behaviour is based on a capacitor C_{CK} that is charged/discharged [3] at constant current while the voltage V_{CK} across it is compared with a voltage reference V_H or V_L. Initially, V_{CK} and V_{out} are 0, the inverting input of the comparator CP2 is at V_H and C_{CK} is charged at constant current I_C. When V_{CK} becomes larger than V_H CP2

switches and C_{CK} is discharged at constant current I_D=I_C. When V_{CK} becomes smaller than V_L CP2 switches again, and so on.

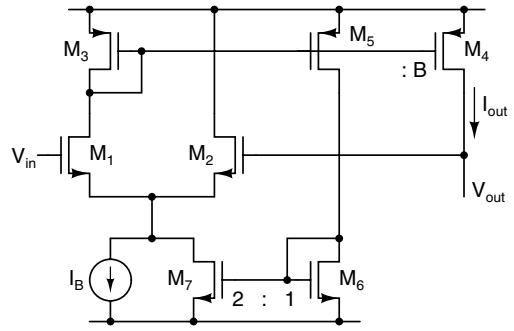

Figure 3: Pull-up schematic circuit.

A non-inverting output buffer has been added to increase the fan-out of CP2. It consists of two complementary circuits: a pull-up circuit (PU) and a pull-down circuit (PD) [1]. Fig. 3 shows the pull-up circuit. The circuit uses an active bias to quickly *pull-up* the output node V_{out}. When V_{in} is 0 no current flows in the circuit, except perhaps I_B through M_2. The output voltage V_{out} is at 0 (due to the action of the pull-down circuit). When V_{in} is high all the current I_B flows through M_1. This current, multiplied by 2, is added to I_B and increases the bias current flowing through M_1. The output current I_{out} quickly becomes very large (its value is B times the current flowing through M_1) and pulls-up the output voltage. When V_{out} reaches V_{in} the current flows also through M_2 so the current through M_3 decreases drastically. The circuit can work with very small bias current I_B (on the order of nano-amps).

To obtain a clock frequency of 5 kHz we chose a capacitor C_{CK}=4.5 pF, a charge/discharge current I_C=I_D=45 nA and a voltage window V_H-V_L=1 V. We chose a pull-up/pull-down bias current I_B=5 nA.

3.3 Power Supply Monitor

The power supply monitor unit consists of a resistive divider connected to the supply and a hysteresis comparator [2, 6]. The comparator output V_{SM} switches from 0 to supply voltage V_{DD} when V_P becomes smaller than the reference voltage V_R (V_R=2 V). The resistors are made with strips of high resistive poly. The strips are made at a minimum width, the precision is reduced, but the power consumption and the area are also reduced.

3.4 Current and Voltage References

The current references are generated by means of a MOS transistor mirror operating in weak inversion and a resistor [9].

To reduce power consumption and considering the precision required, all ASIC voltage references are created by means of diode connected BJT (lateral PNP) biased at constant current.

3.5 Digital Part

To reduce the complexity of the design the digital part has been realized with standard cells.

4. EXPERIMENTAL RESULTS

The circuits have been integrated in 0.8-μm double-metal double-poly CMOS technology. Fig. 4 shows the microphotograph of the test chip. The total area of the analog part (without pads) is 0.53 mm^2, while the whole test chip (including pads) has an area of 4.8 mm^2.

The supply voltage is 5 V. Ten samples were measured.

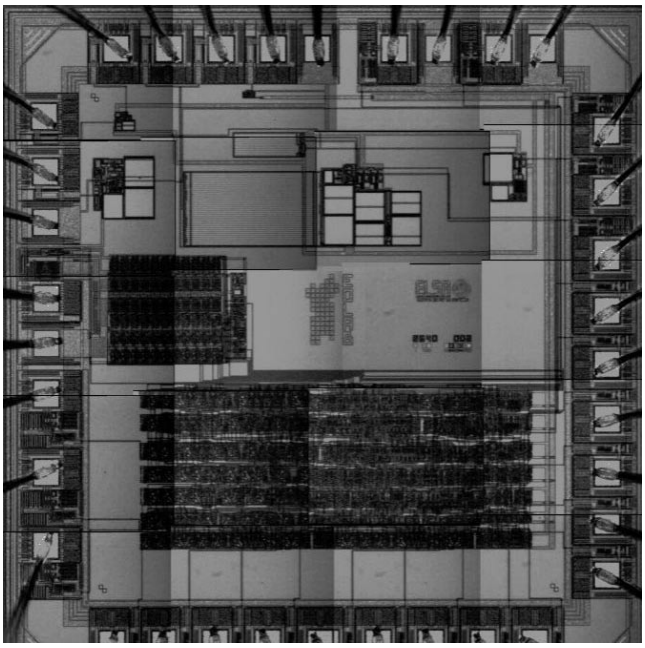

Figure 4: Microphotograph of the test chip.

4.1 Signal Processor

The measured open loop DC gain of the amplifier is 83.9 dB, while the -3 dB bandwidth is 16.7 Hz. In a closed loop configuration (and gain equal to 146) the amplifier has a phase margin greater than 80 degrees with a unity gain frequency of 183 kHz. Its -3 dB bandwidth is equal to 0.15 Hz (lower limit) and 1.9 kHz (upper limit).

Fig. 5 shows the measured output signals in a closed loop configuration. The lower screen shows the closed loop output signal V_O corresponding to typical alarm signals from the IR sensor, while the upper screen shows the corresponding window comparator outputs V_{OH} and V_{OL}. The whole signal processor unit area is 0.3 mm^2. The amplifier absorbs 1.5 μA while the overall signal processor unit absorbs 2.5 μA (maximum value for the ten samples measured).

4.2 Clock Generator

The measurements were made with a 50 pF capacitive load. Fig. 6 shows the measured clock signal. Its frequency is 4.6 kHz and its duty cycle is 58%. The clock frequency has a 20% variation (around 5 kHz) from chip to chip, while the duty cycle is almost constant.

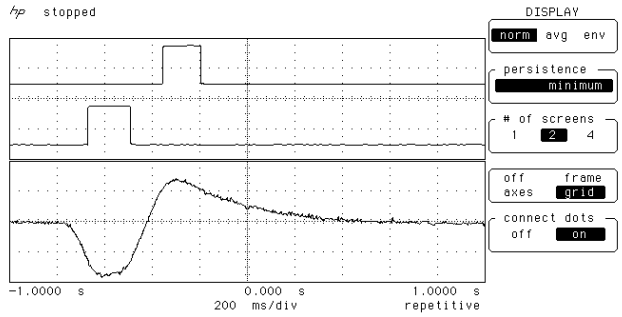

Figure 5: Signal processor outputs: V_{OH} and V_{OL} (upper screen, 4 V/div) and V_O (lower screen, 40 mV/div).

The entire clock generator circuit has an area of 0.05 mm^2 and absorbs 0.8 μA.

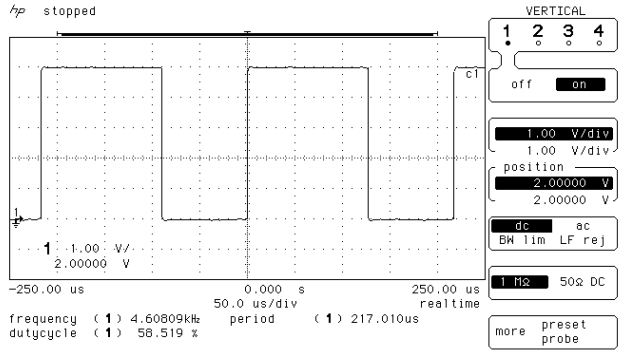

Figure 6: Clock signal.

4.3 Power Supply Monitor

Fig. 7 shows the measured output (V_{SM}) of the power supply monitor unit. V_{SM} switches from 0 to supply voltage V_{DD} when the supply voltage becomes smaller than 4.15 V. From chip to chip the variation is $\pm$0.2 V around 4.25 V.

The power supply monitor circuit has an area of 0.03 mm^2 and a current consumption (including the 10.8 MΩ resistive divider) of 0.7 μA.

The total current absorbed by the analog part is 4 μA (worst case), while the whole chip absorbs 10 μA (working conditions).

The full functionality of the ASIC and its noise immunity at such low currents and frequencies was tested. A test board was developed to test it in the field together with the digital part.

Conclusions

The design of a mixed analog-digital ASIC for a commercial battery-operated burglar alarm system was presented in this paper. To reduce the complexity of the design and using a standard CMOS technology the digital part has been realized with standard cells. So the focus of the low power design

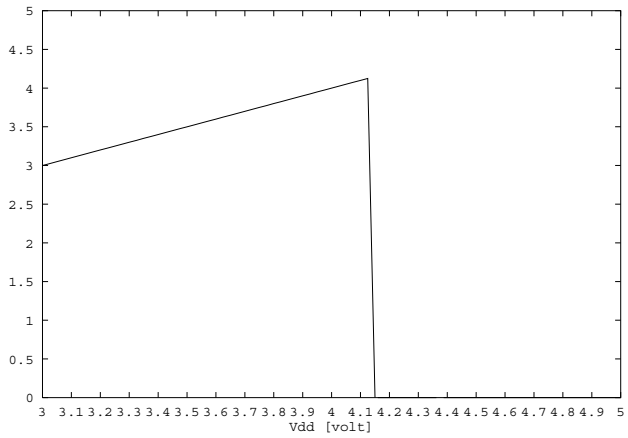

Figure 7: Power supply monitor output versus supply voltage.

is on the analog part. Many techniques have been used and presented here to dramatically limit the power consumption of the device in order to improve battery life and to operate with different supply voltages (battery discharge). All the allowable approximations have been implemented to obtain a more challenging design. Measurements on each single components showed full functionality and complied with specifications.

The analog part absorbs 4 μA, while the whole chip absorbs 10 μA. Even though the example is application specific, the design solutions and each single element can also be utilized in many other battery-operated low-frequency devices (e.g. environmental parameter monitoring).

5. ACKNOWLEDGMENTS

This project has been partially supported by the European Union.

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