Low Power Mixed Analog-Digital Signal Processing

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ABSTRACT

The power consumption of mixed-signal systems featured by an analog front-end, a digital back-end, and with signal processing tasks that can be computed with multiplications and accumulations, is analyzed. An implementation is proposed, composed of switched-capacitor mixed analog/digital multiply-accumulate units in the analog front-end, followed by an A/D converter. This implementation is shown to be superior in respect of power consumption compared to an equivalent implementation with a high-speed A/D converter in the front-end, to execute signal processing tasks that include decimation. The power savings are only due to relaxed requirement on A/D conversion rate, as a direct consequence of the decimation. In a case study of a narrowband FIR filter, realized with four multiply-accumulate units, and with a decimation factor of 100; power saving is 54 times. Implementation details are given, the power consumption, and the thermal noise are analyzed.

1. INTRODUCTION

The rapid evolving CMOS technology offers digital signal processing resources for a lower cost each year. However, the world is still dominated by objects and processes that are analog in nature – analog circuitry is thus still needed. Traditionally, mixed analog/digital systems are implemented with an A/D converter in the analog front-end, followed by a digital signal processor for executing signal processing tasks – often with very high performance requirements on the A/D converter. In recent publications however, the requirements on the A/D converter have been relaxed with sampled analog preprocessing – with decreased power consumption as a result. A low-power QPSK matched filter for DS-CDMA receivers, implemented with a sampled analog multiplier, a ΔΣ modulator, and a digital accumulator, is reported in [1]. Image processing operations are implemented in the analog domain using sampled data multiplications and accumulation as reported in [2].

This paper shows how the power consumption of mixed-signal systems, where the output values are computed as linear combinations of input values and digital coefficients, can be reduced by analog preprocessing. The proposed implementation consist of front-end mixed analog/digital multiply-accumulate units [3] and an A/D converter in the back-end.

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2. BASIC ANALOG AND DIGITAL BUILDING BLOCKS

Digital circuitry in CMOS can take full advantage of the present process scaling, but it's benefit for analog circuitry in CMOS is limited. Therefore, it is interesting and not obvious, how to partition the analog and the digital parts in mixed-signal systems, now and in the future.

The mixed analog/digital (MAD) multiply-accumulate (MAC) unit [3] consists of a multiplying D/A converter (MDAC) [4] and a polarization switching network. This unit, which is modeled as shown in Figure 1, is featured by a continuous-time analog input port and a discrete-time analog output port. The basic operation is as follows: the analog input signal is sampled and stored as a charge on the programmable capacitor array (PCA). A fraction of this charge, proportional to the desired multiplicative factor, is transferred to the accumulation capacitor. This operation is repeated M times for each output value and ended by a reset operation. Implementation details, a noise analysis, and a power analysis can be followed in Section 5.

All-digital MAC units in CMOS can well exploit the process scaling, which implies lower power consumption and higher clock frequency [5]. That is, the energy required for an all-digital MAC operation E_{DMAC} is decreasing with process scaling. For example, the average power consumption of an all-digital low-power 16-bit Wallace tree MAC unit in 0.5µm CMOS technology, reported in [6], is 16.6mW at the maximum clock frequency 67MHz. The calculated average energy per MAC operation is E_{DMAC} = 248 pJ.

The power consumption required for A/D conversion depends on the quantization accuracy (number of bits), the sampling rate, the A/D converter topology, and the circuit technology used, i.e. the general speed-accuracy-power trade-off [7]. The relation between the A/D converter power consumption P_{AD} and the sampling rate f_s

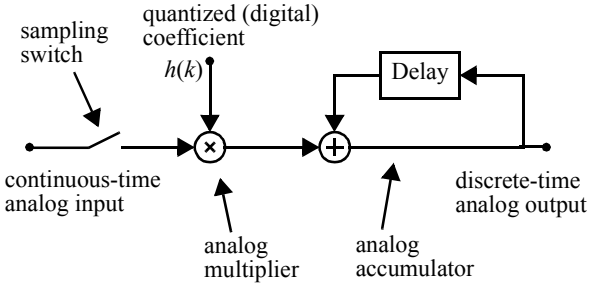

Figure 1: Signal flow graph of the mixed analog/digital MAC unit.

can be assumed to be approximately linear [7] and [8]. That is, for a specific A/D converter topology and circuit technology, the energy required for analog-to-digital conversions E_{AD}, is approximately constant. The general relation between power, energy, and sampling rate is

$$P_{AD} = E_{AD} \cdot f_s \ . \qquad (1)$$

The power consumption of a 12-bit 65MSample/s A/D converter in 0.5µm CMOS reported in [9], optimized for low power consumption, is 480mW only. The average energy per sample is calculated $E_{AD} = 7.4$ nJ.

3. POWER CONSUMPTION OF MIXED-SIGNAL SYSTEMS

The power consumption of mixed-signal systems featured by an analog input port and a digital output port is analyzed. The output values are assumed to be calculated as a linear combination of sampled input values and quantized, digital controllable coefficients.

Denote the input and the output sampling rates of the system, $f_{s,in}$ and $f_{s,out}$ respectively, and define it's decimation factor

$$D = \frac{f_{s,\,in}}{f_{s,\,out}} \ . \qquad (2)$$

Assume that each output value is computed with $M+1$ multiplications and accumulations of input values and coefficients, and that the system is realized with K MAC units. If the MAC units are assigned new computation tasks when old tasks are finished, see Figure 2, the number of MAC units required to sustain the output sampling rate is

$$K = \frac{(M+1)}{D} \ . \qquad (3)$$

3.1 Traditional Implementation using All-Digital MAC Units

The Mixed-signal system I, shown in Figure 3, consists of a high-speed, high-accuracy A/D converter in the front-end, followed by K all-digital multiply-accumulate units. The analog input signal is sampled by the A/D converter and processed in the digital domain. Denote the required energy for an A/D conversion $E_{AD,I}$. The total power consumption of system I becomes

$$P_I = E_{AD,\,I} \cdot f_{s,\,in} + E_{DMAC} \cdot (M+1) \cdot f_{s,\,out} \ . \qquad (4)$$

The expression can be combined with (2) and (3) to result in

$$P_I = (K \cdot E_{DMAC} + E_{AD,\,I}) \cdot f_{s,\,in} \ . \qquad (5)$$

When K is sufficiently small ($K < 30$ when using the data in [6] and [9]), the A/D converter will dominate the system's power consumption.

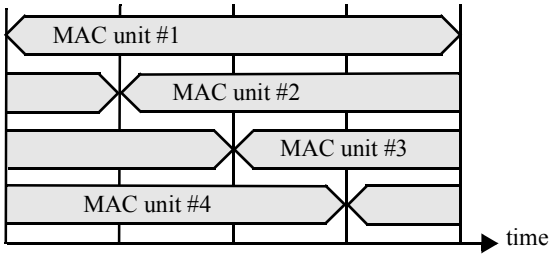

Figure 2: Scheduling of computations on four MAC units. Each output value is a linear combination of sampled input data and digital controllable coefficients.

3.2 Implementation using Mixed Analog/Digital Multiply-Accumulate Units

The mixed-signal system II, shown in Figure 4, is implemented with K mixed analog/digital multiply-accumulate units, which include sample-and-hold circuits in the analog front-end, and a slow A/D converter or quantizer in the back-end. The analog input signal is sampled in parallel, and processed in the analog domain with quantized coefficients. The result is finally quantized in the A/D converter.

The mixed analog/digital MAC unit operates in the analog domain, and thus the output signal-to-noise ratio is limited by thermal

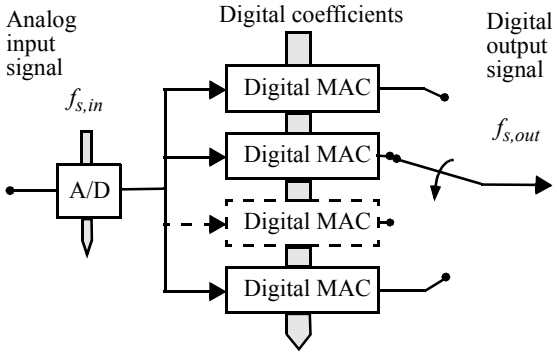

Figure 3: Mixed-signal system I. The traditional realization of a mixed-signal system comprises an A/D converter in the front-end and *K* parallel all-digital MAC units.

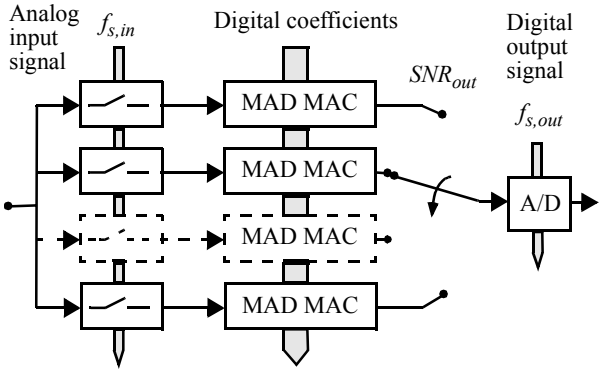

Figure 4: Mixed-signal system II. The proposed realization of a mixed-signal system comprises *K* parallel MAD-MAC units, and an A/D converter or a quantizer in the back-end. The MAD-MAC units include track-and-hold circuits.

noise, see Section 5. The average energy required for a single MAC operation to achieve the maximum output signal-to-noise ratio $SNR_{out,max}$, is calculated by combining (26) and (31) as

$$E_{MADMAC} \leq \frac{12(2M+3)k_B T}{\alpha} \cdot SNR_{out,max} , \qquad (6)$$

where T is the circuit temperature, and $k_B = 1.38 \cdot 10^{-23}$ J/K is the Boltzmann constant.

Denote the energy required for an A/D conversion by this system $E_{AD,II}$. The total power consumption is

$$P_{II} = K \cdot E_{MADMAC} \cdot f_{s,in} + E_{AD,II} \cdot f_{s,out} . \qquad (7)$$

This expression can be rewritten with (2) to result in the power consumption of system II,

$$P_{II} = \left(K \cdot E_{MADMAC} + \frac{E_{AD,II}}{D} \right) \cdot f_{s,in} . \qquad (8)$$

3.3 Power Consumption Comparison

When, and under which circumstances, is the power consumption in mixed-signal system II lower than in mixed-signal system I? The ratio of the power consumption of system II to the power consumption of system I is

$$\frac{P_{II}}{P_I} = \frac{\left(K \cdot E_{MADMAC} + \frac{E_{AD,II}}{D} \right) \cdot f_{s,in}}{(K \cdot E_{DMAC} + E_{AD,I}) \cdot f_{s,in}} . \qquad (9)$$

Assume that the signal processing operation, e.g. channel selection or pattern matching, decreases the dynamic range requirement on the A/D conversion. That is, the dynamic range required on the A/D converter is lower in system II than in system I. Dynamic range is paid with power consumption [7]. This leads to that the required A/D conversion energy is lower in system II than in system I,

$$E_{AD,II} \leq E_{AD,I} . \qquad (10)$$

Assume that all-digital MAC operations are for free, i.e. $E_{DMAC} = 0$, and combine (9) and (10). This leads to an overestimation of the power ratio in favor of system I,

$$\frac{P_{II}}{P_I} \leq \frac{K \cdot E_{MADMAC}}{E_{AD,I}} + \frac{1}{D} . \qquad (11)$$

The average energy required for a MAC operation depends on the maximum output SNR as stated in (6). The combination of (3), (6), and (11) leads to an expression of the power ratio with respect to the output SNR,

$$\frac{P_{II}}{P_I} \leq \frac{12k_B T \cdot K(2KD+1)}{\alpha E_{AD,I}} \cdot SNR_{out,max} + \frac{1}{D} , \qquad (12)$$

where $12k_B T / \alpha E_{AD,I}$ is of order 10^{-11}. By inspection of (12), we conclude: signal processing tasks that can be realized with a low number of MAC units *K,* with large decimation factor *D*, and with moderate requirement on maximum SNR of the desired signal, can with advantage of low power consumption be implemented as a mixed-signal system II.

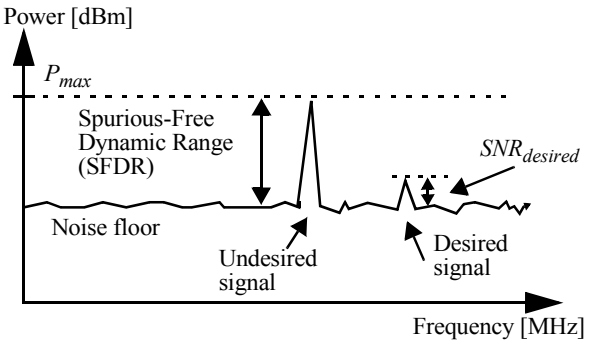

Figure 5: Typical environment with a weak desired signal and a strong undesired signal. P_{max} is the maximum power allowed.

4. CASE STUDY

Suppose that a mixed-signal system is to be implemented, where a weak desired signal is to be selected from one or several strong interfering signals. Define the spurious-free dynamic range (SFDR), the ratio of the strongest allowed signal to the noise and distortion floor, see Figure 5, and denote the signal-to-noise ratio (SNR) required for detection of the desired signal $SNR_{desired}$; which is typical far less than the required *SFDR*,

$$SNR_{desired} \ll SFDR . \qquad (13)$$

Suppose that the desired ultimate rejection of out-of-band signals is 70dB, and that the desired signal bandwidth $B_{desired}$ is a fraction of the bandwidth where interfering signals can occur B_{in},

$$B_{desired} = \frac{B_{in}}{D} . \qquad (14)$$

Undesired signals can be filtered with a narrowband FIR filter of high order, and since the desired bandwidth is less than the bandwidth where interfering signals can occur; the filtered signal can be decimated. This implies that although the FIR filter is of high order, only a few MAC units are required for the computation [10]. Suppose that $D = 100$, that a sufficiently narrowband 400-tap FIR filter with sufficient ultimate rejection is utilized, and that $K = 4$ MAC units are required for its computation. The input sampling rate is related to the input bandwidth $f_{s,in} = 2 \cdot B_{in} = 65$ MSample/s.

Mixed-signal system I implementation:

Position the 12-bit 65MSample/s A/D converter with 82dB SFDR, reported in [9], in the analog front-end, and use $K = 4$ all-digital MAC units with sufficient resolution. The energy per A/D conversion is calculated $E_{AD} = 7.4$ nJ, but the energy per all-digital MAC is assumed to be for free, i.e. $E_{DMAC} = 0$. The total power consumption of the system (5) becomes $P_I = 480$ mW.

Mixed-signal system II implementation:

Place $K = 4$ mixed analog/digital MAC units in the analog front-end, and use a 12-bit 6.5MSample/s A/D converter in the back-end. The required energy per A/D conversion is estimated $E_{AD} = 7.4$ nJ [9]. Assume that the mixed analog/digital MAC

unit linearity is sufficient, and that signed 8-bit coefficient resolution is sufficient to obtain the desired ultimate rejection 70dB. Assume that the operating temperature is $T = 298$ K, the supply voltage is $V_{cc} = 3.3$ V, and that the usable voltage swing is $\alpha = 0.33$ times the supply voltage. The mixed analog/digital MAC unit is implemented with a capacitor array that consisting of $N = 255$ unit capacitors, $C_{unit} = 5.6$ fF. The unit capacitors are designed in double poly with minimum feature size of typical 2.2×2.2 μm^2, and connected to minimum size switches that typical provides a 150mV charge injection error on each unit capacitor. This charge injection error has to be cancelled out using a proper circuit technique. The combination of (17) and (31) leads to the required energy per MAC operation $E_{MADMAC} = 15$ pJ. With 65MSample/s sampling rate, the total power consumption of the system (8) becomes $P_{II} = 9$ mW. The desired signal is typically amplified by the signal processing task, and thus an external automatic gain/attenuator control circuitry may be necessary to prevent that the usable voltage swing is exceeded. The maximum output SNR, limited by the usable voltage swing and the thermal noise, is calculated with (3), (17) and (26) $SNR_{out,\,max} = 51$ dB.

This case study that for some applications, considerable power saving is possible, 54 times for system II compared to system I. However, if several narrowband signal are desired, the system I implementation can be utilized more efficiently in respect of power consumption.

5. MAC UNIT IMPLEMENTATION

The MAD-MAC unit [3] is suitable for implementation with switched capacitors in the CMOS technology. The MAC unit comprises a multiplying D/A converter (MDAC) [4] and a polarity switching network as shown in Figure 6. The MDAC comprises a programmable capacitor array (PCA) [11] and an SC integrator. The PCA is an array of elements, each element consists of a unit capacitor and three switches, as shown in Figure 7. The elements are connected in parallel to the nodes v_{in}^+, v_{in}^-, and $v_{op,in}^-$ or $v_{op,in}^+$. A MAC operation is performed by the following procedure: at the multiply phase, the analog differential input voltage v_{in} is sampled, and the whole PCA is charged. The coefficient sign $s(k)$ is implemented by choosing one of the clock waveforms Φ_m^+ or Φ_m^- at the sampling instant, see Figure 8. At the accumulate phase, $r(k)$ unit capacitors C_{unit} out of N in the capacitor array are discharged to the accumulation capacitor C_2, which corresponds to a multiplication. The multiplicative factor becomes

$$h(k) = \frac{s(k) \cdot r(k) \cdot C_{unit}}{C_2}. \qquad (15)$$

The MAC unit is zeroed when the switches controlled by the waveforms Φ_m and Φ_2 are closed. The waveforms Φ_m^+, Φ_m^- and Φ_2 are delayed compared to Φ_m and Φ_{i1} to reduce the charge-injection errors.

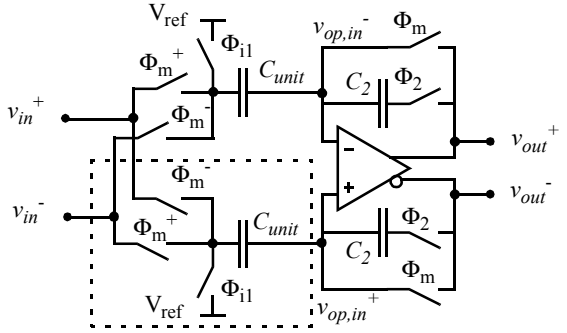

Figure 6: A fully differential MDAC with a PCA consisting a single element.

5.1 Thermal Noise

The thermal noise in switched-capacitor (SC) circuits is referred to as k_BT/C noise. This noise is generated by the closed switch and attach to the connected capacitor C when the switch opens. The resulting noise charge Q_n on a capacitor C, at absolute temperature T, can be modeled as a normally distributed stochastic variable with zero mean and variance

$$Var(Q_n) = k_BTC. \qquad (16)$$

A calculation of the thermal noise that accumulates in the MAC unit follows. Consider the single-ended circuit shown in Figure 9, where the opamp is ideal, and that the switches are modeled as resistors. The PCA is built with N unit capacitors, and in order to achieve a proper feedback factor β, $0.5 \le \beta < 1$ at the accumulation phase, and thereby avoids high requirements on the opamp bandwidth, we choose

$$C_2 = N \cdot C_{unit}. \qquad (17)$$

At the multiplication phase, the switches S_1 through S_N and S_G are closed, see Figure 10a. The switches attached to the unit capacitors on the right hand side generates a noise charge at each unit capaci-

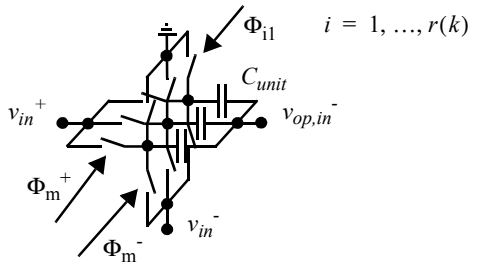

Figure 7: Elements in the programmable capacitor array (PCA), attached to the node $v_{op,in}^-$.

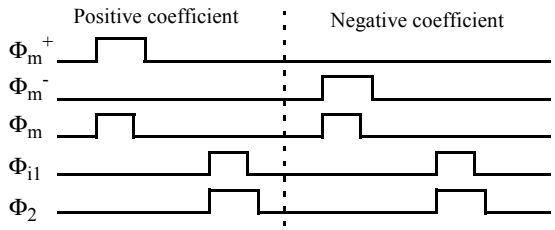

Figure 8: Clock waveforms to perform a MAC operation with positive and negative coefficients.

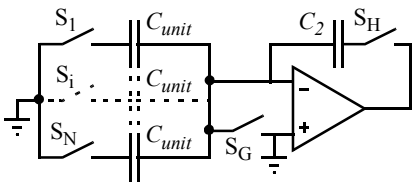

Figure 9: The single-ended SC circuit used for thermal noise analysis.

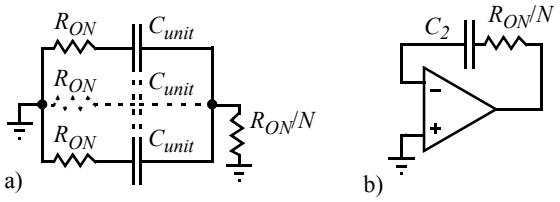

Figure 10: The simplified SC circuit in its a) multiplication and b) accumulation phase.

tor. At the accumulation phase, only the switch S_H contribute to noise since it opens first, see Figure 10b.

Denote the total number of unit capacitors used to represent coefficient values during the $M+1$ accumulations L,

$$L = \sum_{k=1}^{M+1} r(k). \tag{18}$$

L is upper bound by the maximum coefficient value and lower bound by the coefficient zero as

$$0 \le L \le N(M+1). \tag{19}$$

The single-ended mean-square noise charge on capacitor C_2, based on $M+1$ accumulations, becomes

$$Var(Q_{n,final}) = Lk_BTC_{unit} + (M+2)k_BTC_2 . \tag{20}$$

The combination of the charge-voltage relation of a capacitor $Q = VC$ and (17) result in the accumulated noise voltage

$$Var(V_{n,final}) = \frac{(L+(M+2)N)k_BT}{NC_2} . \tag{21}$$

The corresponding differential output mean squares noise of the MAC unit becomes

$$N_{out} = 2Var(V_{n,final}) = \frac{2(L+(M+2)N)k_BT}{NC_2} \tag{22}$$

Obviously, the accumulated thermal noise is proportional to the number of accumulations, and inversely proportional to the accumulator capacitor size C_2.

Independent of the actual coefficients used, the combination of (19) and (22) leads to an estimation of the output noise

$$2 \cdot \frac{(M+2)k_BT}{C_2} \le N_{out} \le 2 \cdot \frac{(2M+3)k_BT}{C_2} . \tag{23}$$

5.2 Output Signal-to-Noise Ratio

The output power P_{out} of a fully differential sinusoidal waveform with a voltage swing V_{pp} per terminal is

$$P_{out} = \frac{V_{pp}^2}{2} . \tag{24}$$

Define the output signal-to-noise ratio: the ratio of the output signal power P_{out} to the mean-square output noise N_{out} as

$$SNR_{out} = \frac{P_{out}}{N_{out}} . \tag{25}$$

When the full output voltage swing $V_{pp,max}$ is utilized, maximum signal-to-noise ratio $SNR_{out,max}$ is obtained. The combination of (23), (24) and (25) result in an expression of the maximum output signal-to-noise ratio,

$$\frac{\alpha^2 V_{cc}^2 C_2}{4(2M+3)k_BT} \le SNR_{out,max} \le \frac{\alpha^2 V_{cc}^2 C_2}{4(M+2)k_BT} . \tag{26}$$

5.3 Power Consumption

The major power consuming device in the mixed analog/digital MAC unit is the operational amplifier. The operational amplifier has the purpose to transfer charges from several capacitors to another capacitor in a certain amount of time. Other sources of power consumption are switch drivers, bias, and reference circuitry. A calculation of the required power drain to able charge transfers follows. Denote the maximum output voltage swing and the maximum output current per terminal, $V_{pp,max}$ and $I_{out,max}$ respectively. Consider a class-A operational amplifier with a continuously current drain $I_{out,max}$ from the power supply. The slew rate required to fulfill the charge redistribution at the accumulation phase is

$$SR = \frac{V_{pp,max}}{T_{SR}} = \frac{I_{out,max}}{C_2} , \tag{27}$$

where T_{SR} is the charge-redistribution time. The charge-redistribution time is typically

$$T_{SR} = \frac{1}{3f_{s,in}} \tag{28}$$

if considering the multiplication phase, the accumulation phase, and the idle time between these phases. Cascode operational amplifiers are operational when the output voltage swing per terminal V_{pp} is limited as

$$V_{pp,max} = \alpha \cdot V_{cc} , \tag{29}$$

where α is the usable voltage swing per terminal of the supply voltage V_{cc}. Assume that a differential structure is utilized. The power consumption is computed by combining (27), (28), and (29) to result in

$$P_{SR} = V_{cc} \cdot I_{out,max} = 3\alpha V_{cc}^2 C_2 f_{s,in} . \tag{30}$$

Not surprisingly, the power consumption can be decreased to the cost of increased output noise, by decreasing the size of the accumu-

late capacitor C_2 (22), or to the cost of lower input sampling rate $f_{s,in}$, which affects the usable input bandwidth. The combination of (1) and (30) leads to the energy required for a single mixed analog/digital MAC operation,

$$E_{MADMAC} = \frac{P_{SR}}{f_{s,in}} = 3\alpha V_{cc}^2 C_2 \ . \qquad (31)$$

6. CONCLUSIONS

The power consumption of mixed analog/digital systems, realized with multiply-accumulate units and an A/D converter, is analyzed. It is found that the energy required for A/D conversions is much higher than the energy required for mixed analog/digital, or all-digital multiply-accumulate operations, and thus the power consumption of the system can be decreased by relaxing the requirement on the A/D conversion rate. A proposed implementation of a mixed-signal system with mixed analog/digital MAC units in the analog front-end and an A/D converter in the back-end, is shown to be superior in respect of power consumption, compared to the traditional implementation with an A/D converter in the front-end and all-digital MAC units – even though the all-digital MAC operations are assumed to be for free in respect of power consumption. In a case study of a narrowband FIR filter application, realized with four MAC units and with a decimation factor of 100, it is shown that power saving of 54 times are possible.

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