Power Consumption Reduction in High-Speed ΣΔ Bandpass Modulators

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Abstract

Power consumption is a key point in the design of high-speed switched capacitor (SC) circuits, which allow to efficiently implement a number of analog functions. Among them, SC ΣΔ modulators are very popular for A/D conversion: in this kind of circuits, operational amplifiers are the most consuming cells because of their requirements in terms of DC gain and unity-gain frequency. A new amplifier with 110dB DC gain and a unity-gain frequency of 250MHz is presented. The large power consumption (20mW) makes critical its use in commercial applications: however, combining this cell with a fast adaptive biasing circuit, high performance may be achieved with a reasonable dissipation.

This approach has been used in the design of a 6th-order bandpass ΣΔ modulator featuring 73dB DR and suitable for the conversion at IF (10.7MHz) of the FM radio signal.

1. Introduction

A key aim of digital radio receiver design is to place the analog-to-digital interface at as high frequency as possible, allowing most of the signal processing to be performed in the digital domain, giving better performance at lower cost. Therefore, high performance analog-to-digital converters (A/D) are highly desired in digital radio applications. The considerations reported in this paper are about high-frequency SC circuits. The design of A/D converters for the conversion of the radio signal at Intermediate Frequency (IF=10.7MHz, in FM broadcasting system) is taken for demonstrating the proposal. Digitizing the signal at IF allows to perform channel selection in the digital domain, taking the full advantage of CMOS scaling. In addition, digital channel selection allows to use programmable filter mask, which supports multi-standard receivers. Processing the signal in the digital domain offers several advantages:

1. I and Q components of the signal are separated in the digital domain, thus allowing a very high quality down-conversion;
2. Problems of 1/f noise and DC offsets are avoided;
3. Flexibility and testability of the system are improved.

Bandpass ΣΔ converters are good candidates for use in this application as they combine high resolution conversion of a relatively narrow frequency band with strong rejection of out-of-band signals from the digital filter stage.

Switched capacitor is the preferred analog technique for the implementation of ΣΔ modulators due to its high circuit accuracy. The operating speed of a SC circuit is determined by the settling time of the operational amplifier used in the circuit. The design of high-speed operational amplifiers with high DC gain and large output swing, implementing the integrators, is then a key point in the design of ΣΔ bandpass modulators to be used in digital radio applications.

In the following, the effects caused by non-ideal operational amplifiers on SC ΣΔ modulators will be deeply analyzed. Therefore, a new high-performance amplifier topology will be presented. Combining this cell with a fast adaptive biasing circuit, a 6th-order bandpass ΣΔ modulator operating at F_S=42.8MHz has been implemented. The ΣΔ bandpass modulator center frequency is $F_S/4$. The device features 73dB dynamic range (DR).

2. Non-idealities analysis in the two-integrator loop

The effect of non-ideal operational amplifiers on the behavior of SC circuits have been deeply analyzed [1][2]: these analyses can be applied to understand the behavior of two-integrator-loop resonator at high sampling rates in resonator-based bandpass ΣΔ modulators.

Since the SC integrator (depicted in Fig.1) is the key constituent of the $F_S/4$ resonator (Fig.2), degradation in the performance of such resonator can be studied by considering how non-idealities in the integrators induce errors into its transfer function. The main error sources of the operational amplifier are the limited unity-gain frequency, the finite DC gain and the limited output swing.

In presence of limited operational amplifier bandwidth, the SC integrator suffers for incomplete settling. If the integrator is assumed to settle linearly with a single-pole response, incomplete settling causes an integrator gain error. In this case the transfer function of the generic integrator is given by:

$$H_{INT\,(i)}(z) = \frac{C_{Si}}{C_{Ii}}(1-\varepsilon_i)\frac{z^{-1}}{1-z^{-1}} \qquad i = 1,2$$

where the gain error term is $\varepsilon_i = e^{-T/\tau_i}$ (τ_i is the closed-loop time constant of the integrator and T is the time allowed for the

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operational amplifier to settle). If the resonator is implemented using two-phase, non-overlapping clocks with 50% duty cycle, T has to be slightly lower than $T_S/2$, where $1/T_S=F_S$, that is the sampling frequency. As the sampling rate is increased, the available settling time, T, decreases, and the gain error becomes increasingly large. It should be noted however that, in practice, settling time in SC circuits is rarely governed by strictly linear, single-pole response. In fact, the settling process of the integrators may include an amplitude signal-dependent slewing component and/or may include a second "slow" settling component.

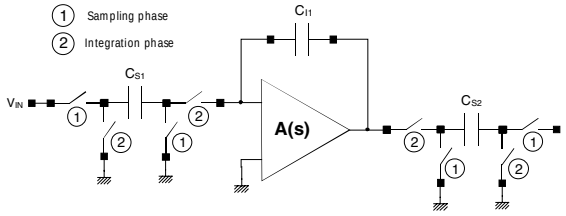


Fig. 1 – Single-ended SC integrator scheme

The effect of incomplete single-pole integrator settling on the resonator performance can be descripted by the following relation, which links the $F_S/4$ resonator transfer function, $H_{RES}(z)$, with integrator non-idealities:

$$H_{RES}(z) = (1-\varepsilon)\frac{z^{-1}}{1 - 2\varepsilon z^{-1}+z^{-2}}$$

where $\varepsilon = (\varepsilon_1 + \varepsilon_2)$. For simplicity, both the gains of the integrators (C_{Si}/C_{Ii}, i=1, 2) are chosen to be one. Thus, finite bandwidth (i.e., incomplete settling) in operational amplifiers causes a fractional shift in the resonator center frequency, f_0, that can be expressed by the following equation:

$$\frac{\Delta f_0}{f_0} = -\frac{2\varepsilon}{\pi}$$

Thus, the relative deviation (θ_{FB}) of the resonator center from $\pi/2$ (i.e, $F_S/4$) may be expressed as:

$$\theta_{FB} = \varepsilon$$

If the sampling frequency is increased, thus decreasing the time allotted for settling (T), the fractional shift of the center frequency f_0 becomes larger: this phenomenon causes an increment of the in-band noise, since the bound of the bandpass region moves slightly in the signal bandwidth.

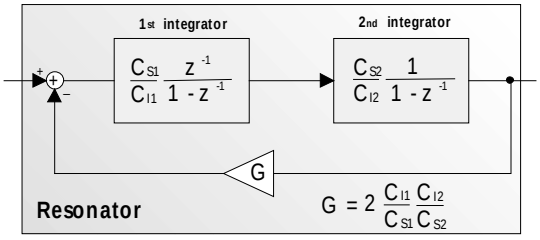


Fig. 2 – $F_S/4$ resonator implemented using a two-integrator loop

Fig.3 shows the effect caused by a finite operational amplifier bandwidth (150MHz) on the Noise Transfer Function (NTF) of a $F_S/4$ resonator-based 6th-order SC ΣΔ bandpass modulator operating at 42.8MHz.

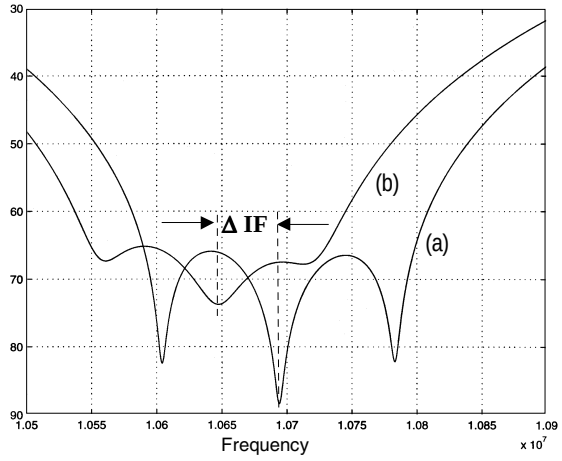


Fig. 3 – NTF of a resonator-based 6th-order SC ΣΔ bandpass modulator: (a) ideal case; (b) finite operational amplifier bandwidth

In presence of finite operational amplifier gain (A_i), the generic SC integrator implemetation has the following transfer function:

$$H_{INT\,(i)}(z) = \frac{C_{Si}}{C_{Ii}}\,(1-\delta_i)\frac{z^{-1}}{1 - (1-\gamma_i)\,z^{-1}}$$

where the terms δ_i and γ_i model perturbations in the gain and pole locations of the integrator i (i = 1, 2), respectively, and may be expressed as:

$$\delta_i = \frac{1}{A_i}\left(1 + \frac{C_{Si}}{C_{Ii}}\right)$$

and

$$\gamma_i = \frac{\frac{1}{A_i}\left(\frac{C_{Si}}{C_{Ii}}\right)}{1 + \frac{1}{A_i}\left(1 + \frac{C_{Si}}{C_{Ii}}\right)}$$

The effect of the finite gain of each operational amplifier on the behaviour of the resonator may be modelled by the following equation:

$$H_{RES}(z) = (1 - \delta)\frac{z^{-1}}{1 + (\gamma - 2\delta)\,z^{-1} + (1 - \gamma)\,z^{-2}}$$

where $\delta=(\delta_1+\delta_2)$ and $\gamma=(\gamma_1+\gamma_2)$.

This phenomenon causes the poles of the transfer function of the resonator, $H_{RES}(z)$, to shift away from $\pm F_S/4$ and out of the unit circle. The new pole locations of the non-ideal characteristic are, for small perturbations:

$$p_{i1}, p_{i2} = \frac{2\delta - \gamma}{2} \pm j\left(1 + \frac{\gamma}{2}\right)$$

The deviation (θ_{FG}) of the resonator center from $\pi/2$, due to finite gain, is:

$$\theta_{FG} = \delta - \frac{\gamma}{2}$$

for small perturbations. This means that the fractional deviation in the resonator center frequency may be expressed as:

$$\frac{\Delta f_0}{f_0} = \frac{\gamma + 2\delta}{\pi}$$

Therefore, both finite bandwidth and low DC gain cause a negative shift from $F_S/4$ in the frequency of the minimum of the NTF: this shift is frequency-dependent in case of finite bandwidth, while is frequency-independent in case of finite DC gain.

Notice that amplifier DC gain could appear not to be the limiting factor if only the previous equation is taken into account. However, DC gain becomes critical for harmonic distortion, which results in large intermodulation distortion (IMD) and reduced spurious-free dynamic range (SFDR), that are key parameters in the design of A/D converters for digital-radio receivers. The same phenomenon is also caused by an unsufficient output swing of the integrators [3]. In addition, high output swings in the operational amplifiers allow to reduce the contribution of the thermal noise caused by the switches and by the integrators, since high output dynamics of the integrators can be used.

Usually, the DR of a modulator is not limited by the quantization noise, but by the thermal noise of the first resonator (operational amplifiers and kT/C of the input sampling network). When the shaped quantization noise is well below the noise floor caused by the thermal noise, the shifts due to finite gain and finite bandwith in the operational amplifiers have a negligible effect on the total in-band noise. However, this is not true if the fractional shift $\frac{\Delta f_0}{f_0}$ becomes large enough to move the large out-of-band quantization noise into the signal passband.

Design centering can be effected by predistorting the capacitor values in order to cancel the effects of finite bandwidth on notch frequency: once the DC gain and the settling performance of each operational amplifier are determined, an artificial shift of the notch frequency of the modulator can be applied to the model. Of course, it is quite difficult to compensate precisely the effect of the non-linearities of the operational amplifiers, and therefore, the best solution is to integrate operational amplifiers with sufficient high DC gain and settling to make this phenomenon negligible. However, optimizing operational amplifiers for fast settling-time and high DC gain is a non-simple task, since both the aspects leads to contradictory demands: high-gain requirement leads to multistage designs, whereas the high unity-gain frequency requirement calls for a single-stage design.

Double-sampling technique allows to use the operational amplifier during both the phases of the clock, thus relaxing its requirements in terms of speed. Unfortunately, double-sampled SC circuits are sensitive to path mismatch and any mismatch between the two channels produces image problems: since linearity is a key parameter in digital-radio receivers, this technique can damage the overall performance of the modulator and then of the system, if F_S/IF is $4/(2n+1)$, n=0,1, … N, as in our case ($F_S/IF=4$). In fact, spurious signals limit the DR of the receiver.

Several circuit approaches may be used to achieve an high DC gain with an high bandwidth:

1. *Double-cascoding* enhances the operational amplifier DC gain without degrading its high-frequency performance. DC gain of about 60-70dB can then be achieved, but in most cases this is not enough;
2. *Triple-cascoding* arises the DC gain up to about 80-90dB, but it is limited by two significant disadvantages: it introduces an extra pole that degrades the phase margin and it reduces the output swing by at least the effective gate-driving voltage;
3. *Adaptive biasing* [4] allows to decrease the bias current as a function of time (during each clock period) or as a function of the amplitude of the input signal: this approach causes a non-linear behavior of the DC gain and a non-single-pole behavior of the settling;
4. *Negative active feedback* allows to boost the gain of an operational amplifier up to more than 100dB without degrading the high-frequency behavior. In addition, with particular implementations of the additional gain stages implementing the gain boosting, a very large output swing can be achieved.

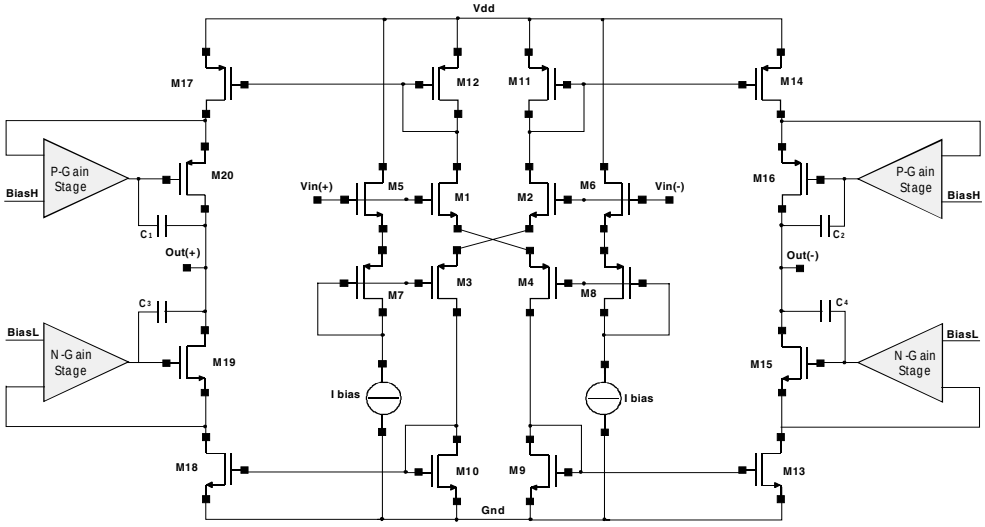


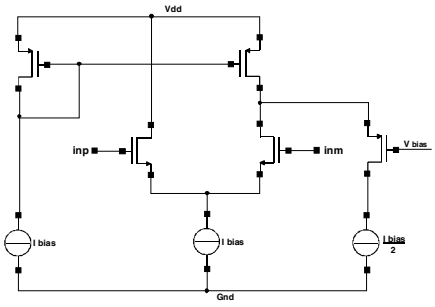
Fig. 4 – Operational amplifier scheme

The fourth approach, that looks very attractive for high-speed ΣΔ modulators, requires large power dissipations, since not only the main operational amplifier, but also the additional gain stages must be fed.

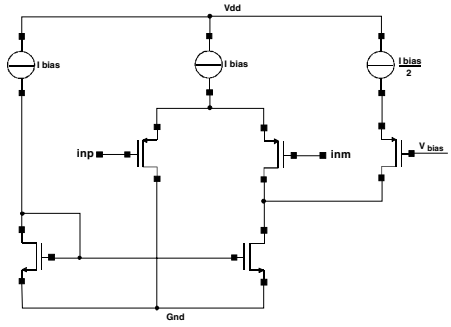
In this paper, we examine a new fully-differential amplifier architecture using a gain-enhancement cascode technique with a new compensation technique for the closely spaced pole-zero (doublet) introduced by the auxiliary feedback operational amplifiers. This architecture, combined with a new adaptive biasing scheme, allows to achieve a good trade-off between performance (DC gain, unity-gain frequency and output swing) and power consumption.

3. Operational amplifier architecture

The proposed fully differential operational amplifier is reported in Fig.4. The core of the circuit is the class AB input stage proposed by Castello and Gray [5]. The DC gain of this configuration is enhanced through auxiliary gain boosting stages, which have the advantage of allowing the maximum output swing possible.



(a) PMOS gain boosting stage



(b) NMOS gain boosting stage

Fig. 5 – Gain boosting stages

Fig.5 shows respectively the PMOS and the NMOS gain boosting stage. The simplified folded-cascode architectures, implementing the boosting stages, offer a large output swing and a high DC gain (40dB). Four small capacitors (C_1=C_2=C_3=C_4=200fF), connecting the outputs of the additional gain stages with the outputs of the main amplifier, compensate the doublet caused by the gain boosting technique.

It is well-known that a doublet can seriously degrade the settling behavior of an operational amplifier due to the introduction of a second slow settling component: other approaches [6] try to make this "slow" settling component fast enough: if the time constant of the doublet τ_{PZ} is smaller than the main time constant τ/β of the closed loop with feedback factor β, the settling time will not be damaged by the doublet, thus mantaining a single-pole behavior. Unfortunately, in a modulator, any operational amplifier has a different feedback factor: in this case, the best solution is then to compensate the doublet as previously proposed.

Of course, this approach reduces the unity-gain frequency of the operational amplifier, since the compensation capacitors load the output nodes, thus lowering the value of the dominant pole. In any case, their contribution is negligible in applications where the output loads are some pF's: that is the case of high-DR ΣΔ modulators, where the capacitors of the filter cannot be small because of the thermal noise.

The proposed architecture features over 110dB DC gain and a bandwidth of 250MHz (Fig.6) with a 30pF×2 load. Settling simulations show a fast single-pole settling behavior and a settling time of 10ns for 0.1% accuracy, with a 5pF×2 load. The output swing is 2.6V with a 3.3V power supply. The power consumption of the overall architecture is about 20mW (16mW are due to the main operational amplifier and 4mW to the gain boosting stages).

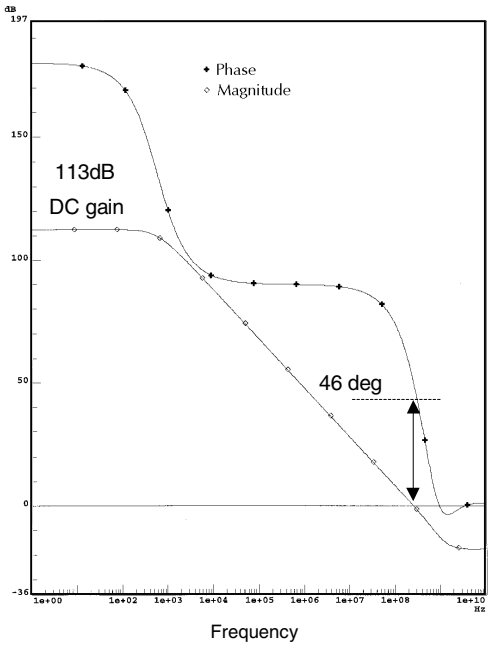


Fig. 6 – Frequency response of the operational amplifier

4. Adaptive biasing scheme

The proposed operational amplifier has been used as basic cell in the implementation of the resonators of a 6th-order bandpass ΣΔ modulator for the conversion at IF (10.7MHz) of the FM radio signal. The sampling frequency of the modulator is 42.8MHz and then, each integrator has to settle in less than 12ns with a good accuracy.

Because of its high requirements, the amplifier results by far the most consuming cell in the system: thus, reducing the power consumption of this cell means reducing almost linearly the overall consumption of the whole modulator.

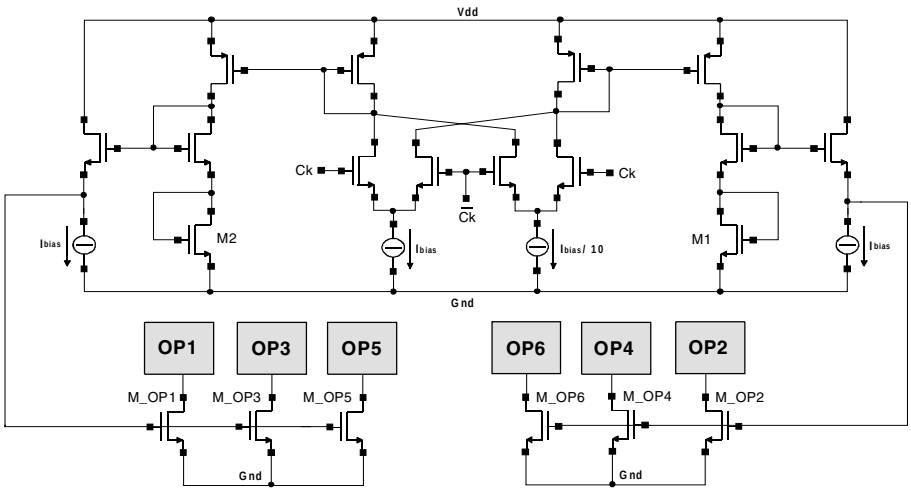


Fig. 7 – Adaptive biasing scheme

Since the high performance of the amplifier are required only during the integration phase, a fast clocked references generator, operating the integrators in different biasing conditions during the integration phase and the sampling one, has been exploited.

The proposed adaptive biasing scheme is shown in Fig.7: devices M_OP1, M_OP2, …, M_OP6 are the current generators of the six integrators of the modulator (and thus physically are part of the operational amplifiers, I_{bias} in Fig.4). In the high-current state, the generic M_OPi (i=1,2, …, 6) current generator mirrors the device M1 (or M2, for simmetry) and current I_{bias} (1-1.2mA, externally selectable) is fed to the correspondent operational amplifier. In the low-current state, the V_{GS} of the current generator is reduced, thus reducing the biasing current of the correspondent operational amplifier (in this design, the low-current value was set to $I_{bias}/10$=100-120μA): note that the bias current during the sampling phase cannot be turned-off but only reduced, in order to allow a fast recover of the operational amplifier during the following integration phase, thus preserving the high settling performance of the integrator.

Devices M3 and M4 act as source followers operating at constant current: I_{DS3} (or I_{DS4}) matches I_{DS1} (or I_{DS2}) in high-current mode. This solution guarantees a good speed and results suitable for high-frequency applications.

This technique allows also to achieve better stability conditions of the operational amplifier during the sampling-phase, which should be critical for two reasons: during this phase the cell has not the load of the following integration stage and it is operating with unitary feedback factor. Thus a larger phase margin can be achieved by reducing the bias current and, consequently, the bandwidth.

It is worth noting that the additional power overhead of the proposed biasing circuit is quite small, since the core of the circuit can work with a current that is lower than the biasing current of the operational amplifiers in the high-current mode.

In the implemented 6th-order ΣΔ modulator, during each clock phase, three integrators are in the sampling mode while the other three are in integration mode (Fig. 8): therefore, during each phase, the power consumption required by the modulator is approximately constant. Thus, the proposed technique does not induce unwanted bouncing of the analog power supply.

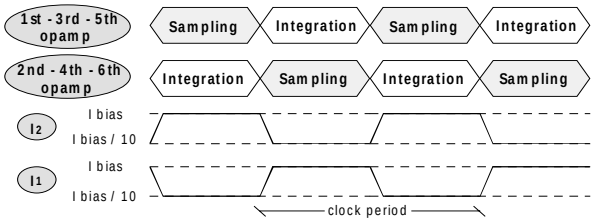


Fig. 8 – Timing diagram

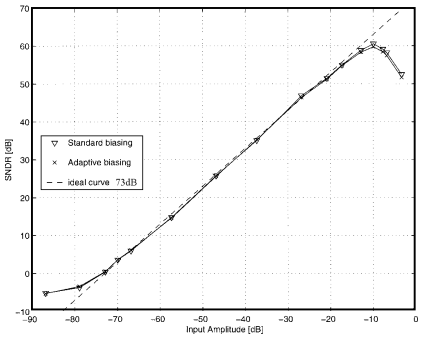


Fig. 9 – SNDR vs. input amplitude with and without adaptive biasing

5. Experimental results

The 6th-order ΣΔ bandpass modulator has been integrated in a standard 0.35μm 3.3V CMOS technology [7].In the developed test chip, it is possible to bias the integrators with the proposed adaptive biasing scheme or also to bypass it, thus feeding all the operational amplifiers with the maximum current (i_{bias}) during the whole sampling period.

The measured SNDR vs. input amplitude characteristic of the modulator (in both the biasing conditions) is plotted in Fig.9. The measured DR is 73dB in both the cases; this proves that the proposed solution does not degrade the performance of the

modulator. Fig. 10 shows the measured output spectrum of a 65536 samples bitstream (using Blackman window) for a –20dB input signal amplitude (0dB corresponds to a differential 4.4Vpp amplitude).

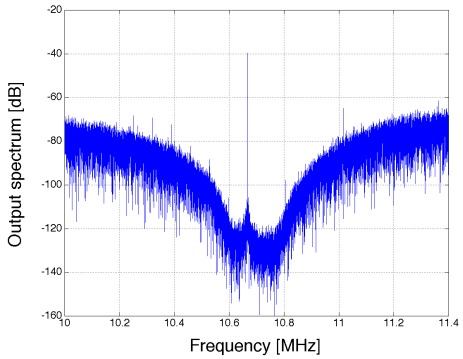


Fig. 10 – Output spectrum for a –20dB input signal

The linearity of the modulator has been evaluated with a two-tone intermodulation (IMD) test. The two tones are spaced by 30kHz and placed in the passband (f_1=10.67MHz, f_2=10.71MHz). At –7dBFS tones amplitude, the third order intermodulation products are suppressed by approximately 58dBc. When the two tones are below –15dBFS (or more), third order intermodulation products are suppressed by 78dBc. This corresponds to an IP3 of about 38dBm. Even disabling adaptive biasing, IMD performance does not change, since the performance is limited by the operational amplifier bandwidth. The power consumption without the adaptive biasing scheme is about 130mW, while enabling the clocked references generator, it results close to 75mW. Table 1 reasumes features and measured performance of the bandpass SC ΣΔ modulator. Fig.11 shows the photograph of the modulator.

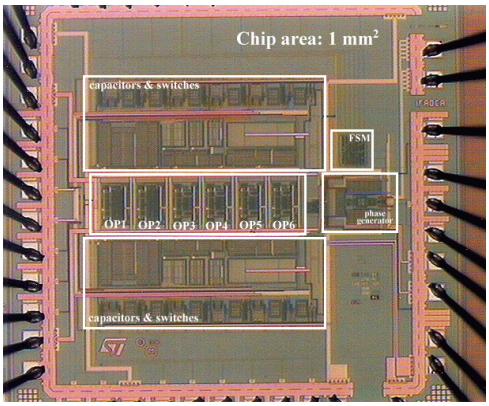


Fig. 11 – Chip photograph

6. Conclusions

Operational amplifiers suitable for high-speed SC circuits require large power dissipations because of their requirements in terms of DC gain, bandwidth and output swing. An amplifier with a DC gain of more than 110dB and a unity-gain frequency of 250MHz (with a 30pF×2 load) has been presented. Its large power consumption (20mW) makes critical its use in commercial high-speed modulators: however, combining this cell with the proposed fast adaptive biasing circuit, high performance may be achieve with a reasonable overall power consumption. This approach has been used in the implementation of a 6th-order ΣΔ bandpass modulator to be used for the conversion at IF (10.7MHz) of the FM radio signal and sampled at 42.8MHz: the proposed clocked biasing scheme has been proved to reduce the total power dissipation of about 40% with respect to a standard non-clocked solution, without degrading the overall performance of the structure.

Design approach	Switched capacitor
Order	6th
Architecture	Single-loop single-bit
Sampling frequency	42.8MHz
Center frequency	10.7MHz
Signal bandwidth	200kHz
Oversampling ratio	107
Dynamic range	73dB (200kHz – FM) 88dB (9kHz – AM)
Peak SNDR	61dB
IMD	-58dBc @ -7dBFS -78dBc @ -15dBFS
IP3	38dBm
Power consumption	75mW (adaptive biasing) 130mW (standard biasing)
Die area	1mm^2
Technology	0.35μm CMOS 3.3V

Table 1 – Features and measured performance of the bandpass SC ΣΔ modulator

7. Acknowledgments

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References

[1] K.Martin and A.Sedra, "Effects of the op amp finite gain and bandwidth on the performance of switched-capacitor filters", *IEEE Trans. Circuits Syst.*, vol. CAS-28, no. 8, pp. 822-829, August 1981.

[2] D.B.Ribner and M.A.Copeland, "Biquad alternatives for high-frequency switched-capacitor filters", *IEEE Journal of Solid-State Circuits*, vol. SC-20, no. 6, pp. 1085-1095, December 1985.

[3] K.L.Lee and R.G.Meyer, "Low distortion switched-capacitor filter design techniques", *IEEE Journal of Solid-State Circuits*, vol. SC-20, pp. 1103-1113, December 1985.

[4] M.G.Degrauwe, J.Rijmenants, E.A.Vittoz and H.DeMan, "Adaptive biasing CMOS amplifiers", *IEEE Journal of Solid-State Circuits*, vol. SC-17, pp. 522-528, June 1982.

[5] R.Castello and P.Gray, "A High-Performance Micropower Switched-Capacitor Filter", *IEEE Journal of Solid-State Circuits*, vol. SC-20, no. 6, pp. 1122-1132, December 1985.

[6] K.Bult and G.Geelen, "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain", *IEEE Journal of Solid-State Circuits*, vol. 25, no. 6, pp. 1379-1384, December 1990.

[7] D.Tonietto, P.Cusinato, F.Stefani and A.Baschirotto, "A 3.3V CMOS 10.7MHz 6th-order bandpass Sigma-Delta modulator with 78dB dynamic range", Proceedings ESSCIRC '99, pp. 78-81, September 1999.

[8] S.R.Norsworthy, R.Schreier and G.C.Temes, Eds., "Delta-Sigma Data Converters. Theory, Design and Simulation", Piscataway, NJ: *IEEE Press*, 1997.