Robust Ultra-Low Power Sub-threshold DTMOS Logic*

Hendrawan Soeleman, Kaushik Roy, and Bipul Paul
Purdue University
Department of Electrical and Computer Engineering
West Lafayette, IN 47907, USA
{soeleman, kaushik, paulb}@ecn.purdue.edu

ABSTRACT

Digital sub-threshold logic circuits have recently been proposed for applications in the ultra-low power end of the design spectrum, where the performance is of secondary importance. To improve switching performance of the sub-threshold logic family with comparable energy/switching, we propose the use of sub-DTMOS (sub-threshold Dynamic Threshold MOS) transistors. The stability of sub-threshold DTMOS logic to temperature and process variations eliminates the need of additional stabilization scheme that may be required for regular sub-threshold MOS logic families to ensure proper operation in the sub-threshold region.

1. INTRODUCTION

The increasing demand for portable applications has caused a significant growth of low-power design, from system level to device level. To achieve low-power requirement, various circuit design techniques have been employed, including voltage scaling and clock gating [1, 2]. These techniques work well in the medium-power, medium performance region of the design spectrum, where the delicate balance of power and delay is well maintained. However, in the *ultra-low power* end of the design spectrum, where speed is of secondary importance, a more rigorous approach is warranted. Digital sub-threshold circuits have recently been proposed to meet the ultra-low power requirement [3]. By operating in the sub-threshold region, digital sub-threshold circuits utilize the continuously flowing leakage current as the switching current. The minute sub-threshold current makes it possible to achieve ultra-low power dissipation. However, the performance of the digital sub-threshold circuits is several orders of magnitude lower than their normal strong-inversion counterparts. Hence, sub-threshold circuits are applicable to only specific classes of applications where ultra-low power is of primary importance. Such applications range from the implantable pace-makers and defibrillators to the recently emerging wearable, wrist-watch computers.

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Another important feature, which limits the robustness of the sub-threshold logic circuits using regular MOS transistors, is their extremely high sensitivity to the variation of temperature and process parameters. The exponential dependence of sub-threshold current on threshold voltage (V_{th}), which in turn depends on the temperature and process parameters, calls for additional stabilization scheme to ensure proper operation. To increase the robustness of the circuit, we adopt a self-adjusted threshold voltage (SAT) scheme [4, 5]. The technique monitors the change in leakage current and stabilizes it by applying appropriate bias to the substrate. A robust sub-threshold logic circuit thus can be achieved, however, this increases the design complexity to a significant extent. We propose another logic family in this paper using sub-threshold DTMOS transistors which shows a significant improvement in delay and excellent stability to temperature and process variations while maintaining the same ultra-low power design constraint.

The rest of the paper is organized as follows: section 2 explains sub-CMOS logic (sub-threshold CMOS) with SAT scheme and discusses its merits and demerits. In section 3, we explain the properties and performance of sub-threshold DTMOS logic family, and compare them with regular sub-threshold MOS logic circuits. Section 4 compares the stability of both logic families to the temperature and process variations. Finally, a conclusion is drawn in section 5.

2. SUB-CMOS LOGIC WITH SAT SCHEME

The leakage current of MOS transistor is extremely sensitive to the temperature and process variations, which in turn limit the robustness of the design. These variations result in V_{th} fluctuation which has a strong exponential effect on the sub-threshold current. One way to handle this limitation is to stabilize the leakage current by means of establishing a feedback to the device. This is done through adopting a SAT scheme to sub-threshold CMOS circuits. The SAT scheme monitors the leakage current and stabilizes any fluctuation in the leakage current by automatically biasing the substrates of the transistors via a negative feedback loop (Fig.1). There are two main components of SAT scheme, namely the leakage current monitor (LCM) and the self-substrate bias (SSB) circuit (Fig.2). LCM is used as a leakage current sensor and a control to the SSB circuit. SSB circuit contains a charge pump which is powered by pulses generated from a ring oscillator. The charges accumulated from the pump are used to bias the substrate. SSB circuit works intermittently and is activated by LCM when

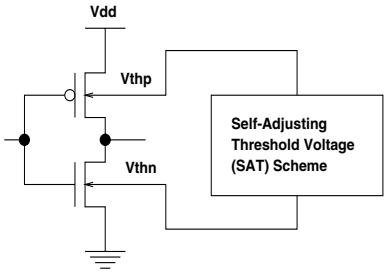

Figure 1: Self-Adjusting Threshold Voltage Scheme

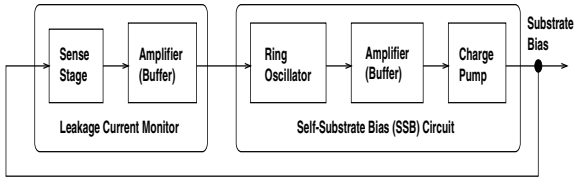

Figure 2: Components of SAT scheme

needed. Once the target substrate bias is reached, the SSB circuit is deactivated. LCM constantly monitors the leakage current and corrects the substrate bias by re-activating the SSB circuit. Thus, the LCM module analogously acts as a thermostat which regulates the temperature and process variations and sets the fluctuation to the pre-specified tolerable range.

With proper substrate biasing, a stable and efficient operation thus can be achieved in the sub-threshold CMOS logic using the SAT scheme, thereby increasing the robustness of the circuit. However, SAT scheme incurs an additional overhead in area and circuit complexity. In designing the SAT scheme, careful effort must be put in to ensure adequate leakage current magnification in the LCM and to balance the trade-off between the resolution of the charge-pump in SSB circuit with the time required to achieve the targeted bias.

While substrate bias is used in the SAT scheme to suppress the change in leakage current and to obtain a stable operation, there may be an alternative way to achieve the same stability with direct substrate biasing without using additional control circuitry. To achieve this goal, we study another logic family, namely sub-threshold DTMOS logic circuit, which is discussed in the following section.

3. SUB-THRESHOLD DTMOS LOGIC

DTMOS is a transistor whose gate is tied to its substrate (Fig.3). Thus, the substrate voltage in DTMOS changes with the gate input voltage, and causes V_{th} to change accordingly. In the off-state i.e. $V_{in} = 0$ ($V_{in} = V_{dd}$) for N-MOS (PMOS), the characteristics of DTMOS is exactly the same as regular MOS. Both have similar properties, such as the same off-current (I_{off}), sub-threshold slope, and V_{th}. In the on-state, however, the substrate-source voltage (V_{bs}) is forward-biased and thus, reduces V_{th} of DTMOS, resulting in higher on-current (I_{on}) than that of regular MOS. Furthermore, the sub-threshold slope (S) of DTMOS improves and approaches the ideal 60mV/decade which makes it more

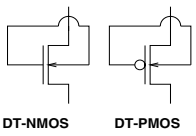

Figure 3: DT-NMOS and DT-PMOS

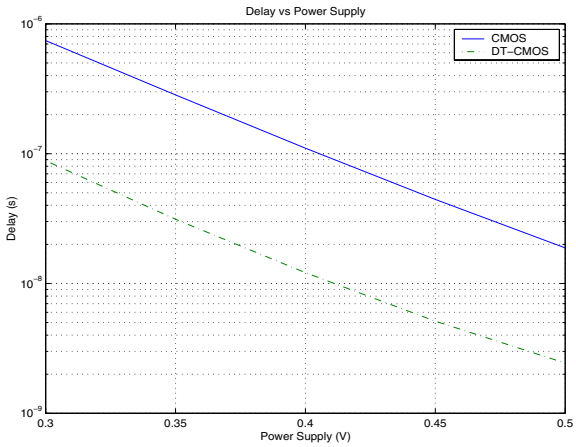

Figure 4: Delay vs. Vdd

efficient in sub-threshold logic circuits to obtain higher gain. This improvement is due to the increase in the inversion charge and the higher carrier mobility [6].

Another advantage of the sub-threshold DTMOS logic is that it does not require additional limiter transistors, which further reduces the design complexity. In contrast, in the normal strong inversion region, the limiter transistors are necessary to limit the forward-biased V_{bs} to be less than 0.6V. This is to prevent forward-biasing the parasitic PN junction diode, while allowing a much higher supply voltage V_{dd} used in the circuit.

3.1 Sub-threshold DT-CMOS Logic

Both DC and AC characteristics of the sub-threshold DT-CMOS logic are analyzed and compared with those of regular sub-threshold CMOS logic. Results are obtained from SPICE simulation using the TSMC $0.35\mu m$ process technology at 55°C. Fig.4 and 5 respectively show the delay and power consumption of CMOS Inverter connected in a ring-oscillator fashion as a function of V_{dd}. The higher I_{on} of sub-threshold DT-CMOS logic causes it to have a higher power consumption, but can switch much faster than regular sub-threshold CMOS circuits. Although DTMOS gate capacitance is larger than that of standard MOS gate capacitance, gate capacitance is only a portion of total switching capacitance and the increase in current drive of DTMOS far outweigh the increase in gate capacitance. Thus, DTMOS gate switches faster than regular MOS.

The power-delay product (PDP) is a measure of the amount of energy/switching and can be used to determine whether the increase of power consumption is more dominant than the delay improvement, or vice-versa. Fig.6 shows the PDP as a function of V_{dd} for both types of CMOS Inverter. The

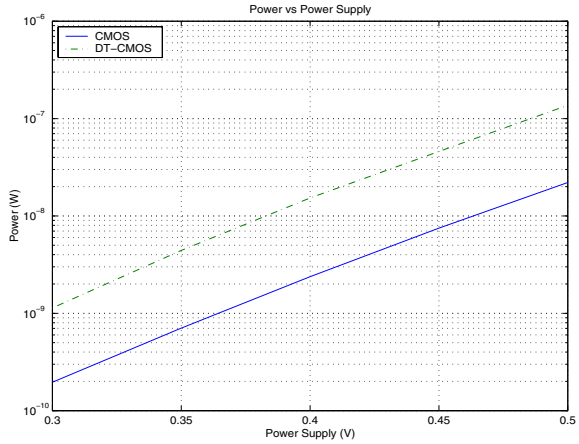

Figure 5: Power vs. Vdd

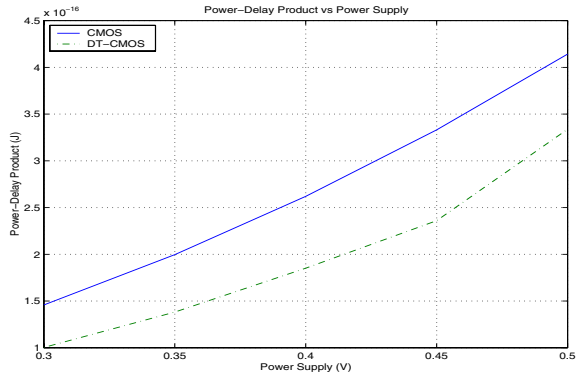

Figure 6: Power-Delay Product vs. Vdd

PDP of DT-CMOS is comparable to the PDP of regular CMOS. Thus, we can operate the circuit at much higher frequency while still maintaining the same energy/switching.

For the DC analysis, the voltage transfer characteristics (VTC) of both regular CMOS and DT-CMOS are simulated and shown in Fig.7. The VTC of both circuits are similar and mimic the ideal VTC. Both show very good noise margin and an exponentially high gain. Such characteristics are normally expected in all sub-threshold logic circuits.

Further, the higher drive current capability of DT-CMOS makes it advantageous to have higher number of fan-out. Moreover, more complex gates can be implemented in DT-CMOS without sacrificing the performance. Fig.8 shows the delay of an Inverter logic gate as a function of the number of fan-out. The superiority of DT-CMOS over regular CMOS in driving a large number of fan-out is clearly observed.

3.2 Sub-threshold DT-Pseudo-NMOS Logic

The effects of DTMOS implementation on sub-threshold Pseudo-NMOS circuit (DT-Pseudo-NMOS) are also analyzed. Two different types of DT-Pseudo-NMOS circuit implementations shown in Fig.9 are used in the analysis. All NMOS transistors in the pull-down network (PDN) are replaced with DT-NMOS transistors. However, regular PMOS and

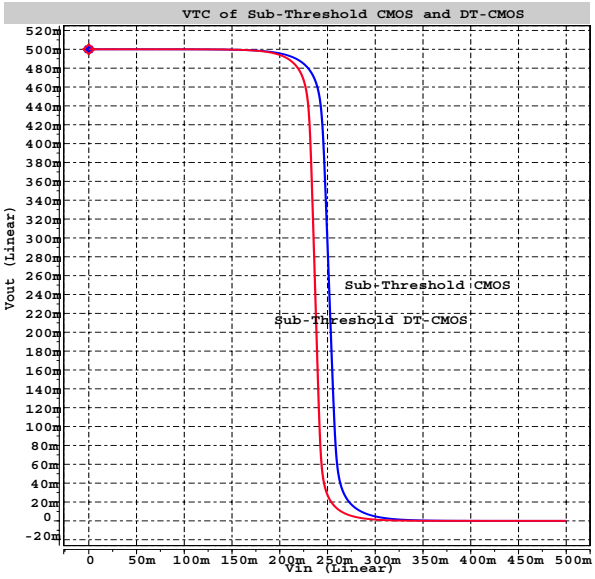

Figure 7: VTC of CMOS and DT-CMOS

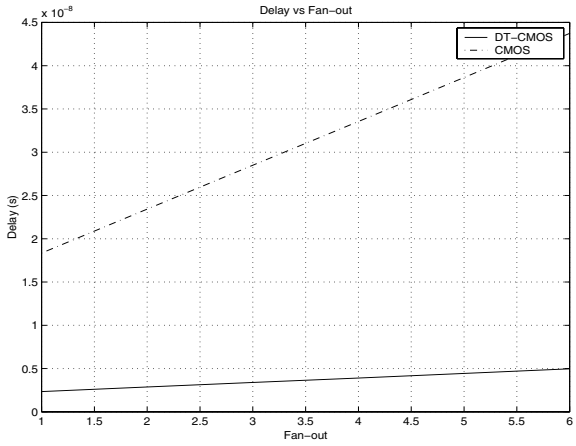

Figure 8: Delay vs. #Fan-outs

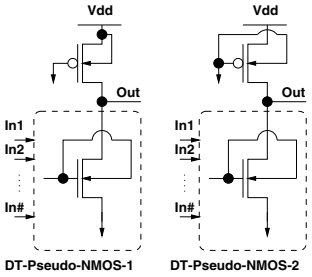

Figure 9: Sub-threshold DT-Pseudo-NMOS Logic

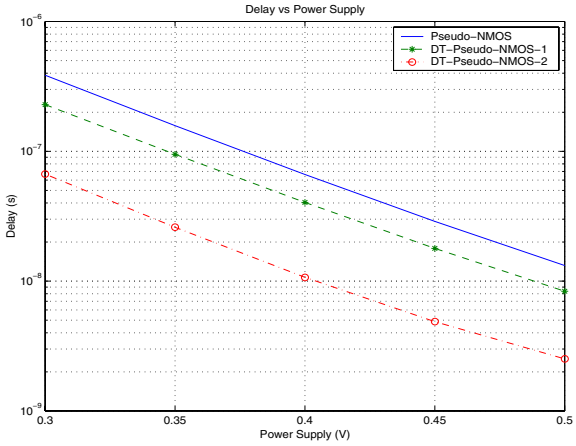

Figure 10: Delay vs Vdd

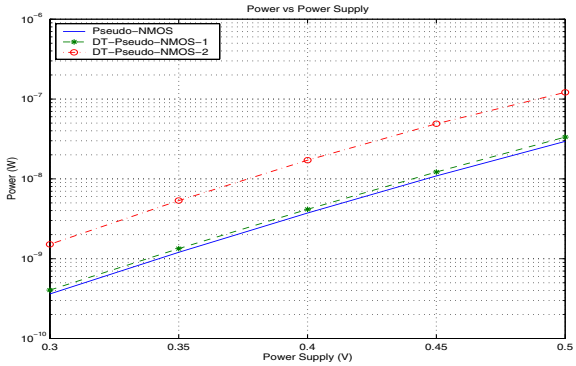

Figure 11: Power vs Vdd

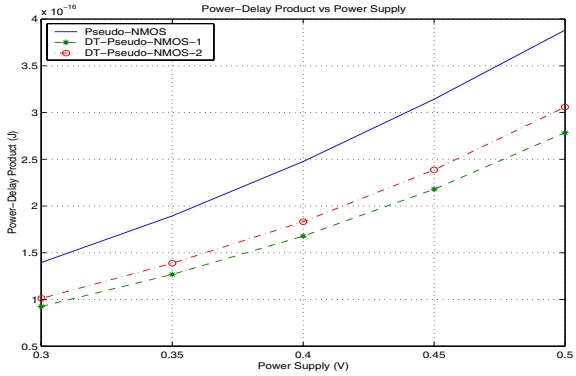

Figure 12: Power-Delay Product vs Vdd

DT-PMOS are used as the load in the first and second implementation, respectively.

Fig.10 and 11 respectively show the delay and power consumption as a function of V_{dd} for the two DT-Pseudo-NMOS logic implementations and regular Pseudo-NMOS logic. The power consumption in sub-threshold Pseudo-NMOS logic is comparable to that of sub-threshold CMOS logic, but it can be operated at a higher frequency. This is because the P-MOS transistors in the pull-up network (PUN) in CMOS logic are replaced with just a single PMOS transistor in Pseudo-NMOS logic. Thus, there is a significant improvement in performance due to the reduction of the load capacitance. Such improvement is even more evident in large fan-in NOR-like complex gates. Both DT-Pseudo-NMOS logic implementations have better delay, but higher power consumption as compared to regular Pseudo-NMOS logic.

Both DT-Pseudo-NMOS implementations have lower PDP (Fig.12) than the regular Pseudo-NMOS, implying that the delay improvement outweighs the increase in the power consumption. Hence, DT-Pseudo-NMOS logic can be operated at higher frequency and consume lower energy/switching than regular Pseudo-NMOS logic.

The voltage transfer characteristics of sub-threshold DT-Pseudo-NMOS logic (Fig.13) are obtained through the DC analysis and are compared with that of regular sub-threshold Pseudo-NMOS logic. It is seen that the VTC of sub-threshold DT-Pseudo-NMOS logic are shifted from the VTC of the regular sub-threshold Pseudo-NMOS logic. This is because we use the same size of the logic gate in our experiments for both DT-Pseudo-NMOS and regular Pseudo-NMOS logics. The shifting reflects the change in the switching currents. The exact replica of the VTC of regular sub-threshold Pseudo-NMOS logic can be obtained for sub-threshold DT-Pseudo-NMOS logic by merely re-sizing the transistors to compensate the change in the switching current. Thus, both implementations of the DT-Pseudo-NMOS logic can have the same DC characteristics as the regular Pseudo-NMOS logic. VTC of sub-threshold DT-Pseudo-NMOS and regular Pseudo-NMOS logic are similar to that of sub-threshold CMOS logic, and do not show any degradation as commonly seen in the strong inversion ratioed-logic. This is due to the sub-threshold characteristics of the transistors where I_{ds} saturates at about 3 kT/q (near-ideal rail-to-rail current source).

4. PROCESS VARIATIONS

It is seen that sub-threshold DTMOS logic circuits have comparable PDP with that of regular sub-threshold MOS circuits, however, can be operated at a higher frequency. It is also important to study the stability of sub-threshold DT-MOS logic to temperature and V_{th} variations to compare their robustness over regular sub-threshold MOS circuits. To compare the stability of different sub-threshold logic circuits, we analyze the effects of temperature and process variations on power and delay of both sub-threshold DT-CMOS and regular sub-threshold CMOS logics.

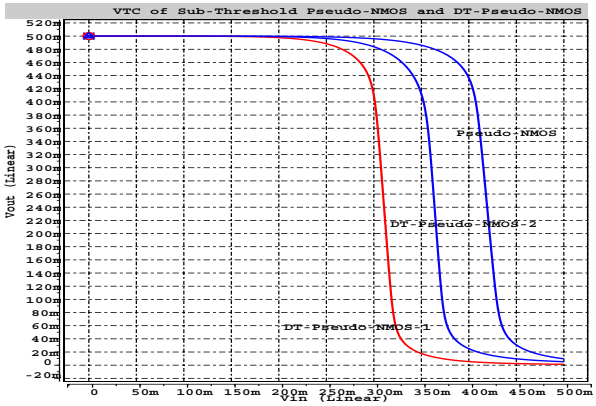

Figure 13: VTC of DT-Pseudo-NMOS

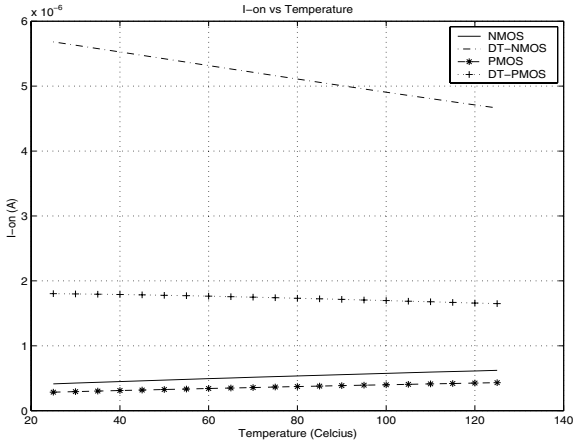

Figure 15: I-on vs. Temperature

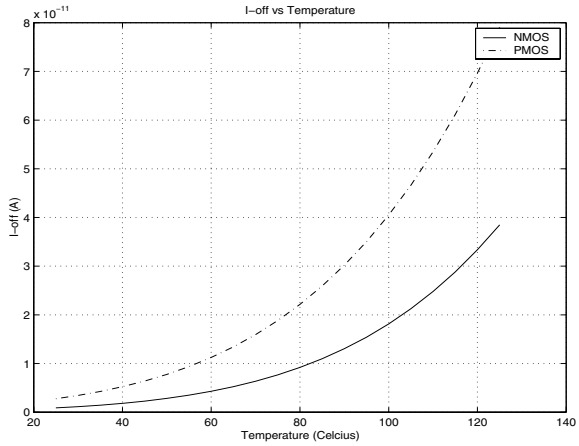

Figure 14: I-off vs. Temperature

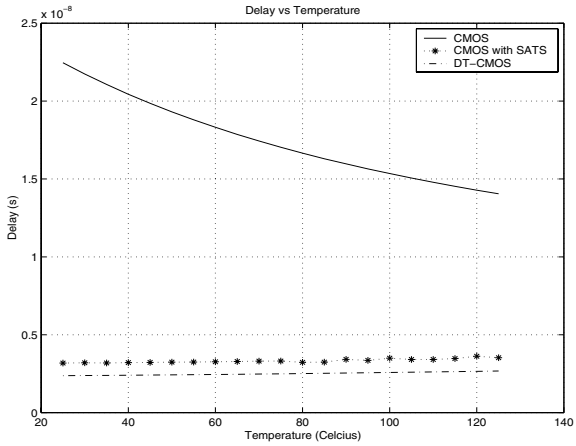

Figure 16: Delay vs. Temperature

4.1 Temperature Variations

The effect of temperature variation is analyzed using SPICE simulation from room temperature ($25°C$) to $125°C$. Fig.14 and 15 show the I_{off} and the I_{on} curves, respectively, for both MOS and DTMOS as a function of temperature. With increasing temperature, the threshold voltage reduces approximately at the rate of $349\mu V/°C$. The reduction in V_{th} causes I_{off} to increase accordingly. Both regular MOS and DTMOS have the same I_{off} value. The increase in sub-threshold slope with increasing temperature is more prominent in the regular MOS than that of DTMOS. Consequently, I_{on} of regular MOS increases with temperature, but that of DTMOS actually reduces with temperature.

The effect of temperature variation on the performance of a sub-threshold DT-CMOS Inverter is also simulated and compared with that of regular sub-threshold CMOS Inverter (with and without the stabilization scheme) (Fig.16). Both sub-threshold DT-CMOS and CMOS with the stabilization scheme are very effective over regular sub-threshold CMOS in maintaining a stable operating frequency over the range of temperature. Because of the substrate biasing (DTMOS and CMOS with SAT scheme), the effective threshold voltages come down to just below the supply voltage (Fig.17) and the devices operate at the onset of moderate inversion region. The currents in these cases are no longer exponentially dependent on V_{gs} and therefore less sensitive to temperature variation. The power-delay product for CMOS with stabilization scheme is better than that of DT-CMOS (Fig.18). This is because the SAT scheme has better control on substrate biasing. However, the design simplicity of sub-threshold DT-CMOS logic makes it more attractive for the ultra-low power operations.

4.2 Threshold Voltage Variations

The process variations on sub-threshold DTMOS logic are analyzed by varying the V_{th} of both NMOS and PMOS by $\pm 10\%$ from their designed values. Fig.19 shows the delay variation of sub-threshold DT-CMOS logic and regular sub-threshold CMOS logic (with and without the stabilization scheme). The inherent robustness of sub-threshold DTMOS logic is again proven to be as comparable and effective as the stabilization property of the SAT scheme associated with regular sub-threshold CMOS logic.

5. CONCLUSION

From the above discussion, it is clear that sub-threshold DTMOS logic can be used to speed up the frequency of

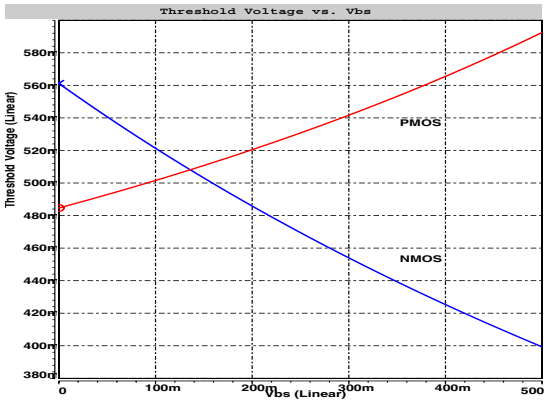

Figure 17: Threshold Voltage vs. Vbs

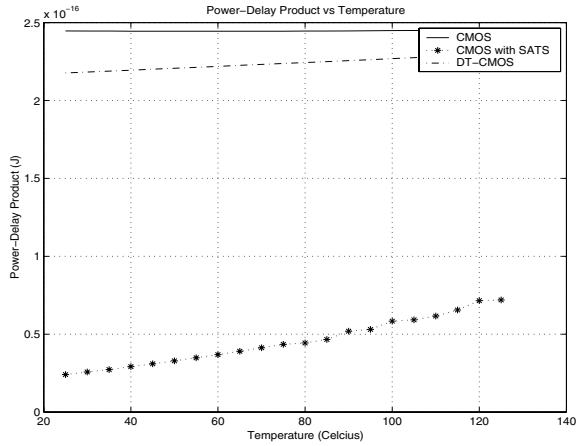

Figure 18: Power-Delay Product vs. Temperature

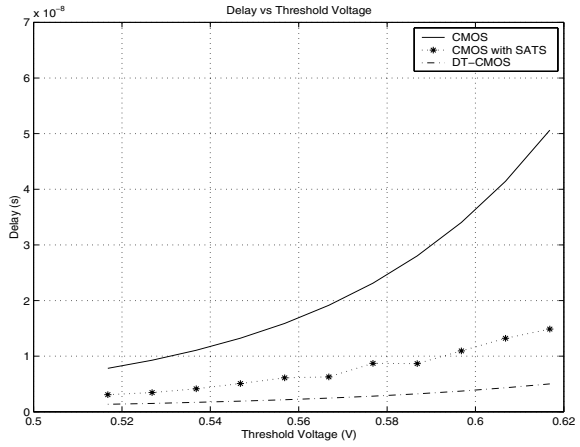

Figure 19: Delay vs. Threshold Voltage

operation up to an order of magnitude, while maintaining the same energy/switching as the regular sub-threshold MOS logic. The threshold voltage of DTMOS is intrinsically changed to achieve low-power, high performance characteristics. Furthermore, its better stability to temperature and V_{th} variations makes it more promising than regular sub-threshold MOS logic to achieve robust circuit without any additional control scheme such as SATS. Of course, there is an increase in process complexity due to the need of contacting and isolating the substrate. However, DTMOS has been successfully implemented in both SOI [7] and bulk Silicon [8]. Therefore, sub-threshold DTMOS logic circuits are more favorable than regular sub-threshold MOS logic due to their simplicity in design and better stability.

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