TUTORIAL 3
SYMBOLIC MODEL CHECKING: PRINCIPLES AND ADVANCED TECHNIQUES

Speakers:

Kenneth L. McMillan - Cadence Berkeley, Labs., Berkeley, CA
Fabio Somenzi - Univ. of Colorado, Boulder, CO

Background: By way of introduction, we will first briefly review the low power/low voltage problems and provide an outline of the rest of the tutorial, which will be in three parts.

Description: The first part is focused on design techniques. Several emerging technologies such as Multiple and Variable threshold CMOS enable low voltage/low power high performance computing while providing a "knob" to dynamically adjust leakage currents. The challenges in design methodologies and tools for these technologies will be discussed. In many applications, there is significant energy advantage in using an embedded power supply scheme where the voltage can be adapted based on computational demand. Rather than designing a system with a static supply to meet a specific timing constraint under worst case conditions, it is more energy efficient to allow the voltage to vary such that the timing constraints are just met at any given operating condition. The key challenges will be discussed including regulator design, circuit styles and scheduling. Trends in low-voltage library design will also be discussed and will cover logic, memory and low-swing interconnect drivers.

In the second part, we will deal with issues of power estimation and modeling. Estimation and modeling are central to any low power design methodology. After an introduction to fundamentals of power estimation, we will discuss power modeling at the gate/cell level. These models allow power analysis to be done at higher than the transistor level. Modeling and estimation at even higher levels (e.g., RTL) are key to doing early design exploration. These will be discussed next, covering both bottom-up and top-down techniques.

Finally, we will cover power/ground bus analysis and design, power optimization, and leakage power estimation and optimization. An overview of the performance, signal integrity, and electromigration reliability issues related to power distribution problems will be given. Common design styles for power distribution, and a unified methodology to design, analyze, and verify large power/ground grids will be presented with case studies. Modeling of package inductance, decoupling capacitors, and circuit parasitics to study their effect on power grid design will be discussed. Techniques to reduce power grid simulation effort, such as vector compression and static determination of worst case power demand scenario will also be considered. Combinational/sequential logic restructuring, encoding and several special design techniques for power reduction will be reviewed. Some recent transistor level and gate level optimization techniques to reduce leakage power in dual-Vt circuits will also be presented.