TUTORIAL 2

INTERCONNECT-CENTRIC DESIGN AND ANALYSIS
FOR ELECTRICAL INTEGRITY IN SYSTEMS-ON-A-CHIP

Speakers:

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Background: With rising clock rates and scaling technology, it is becoming increasingly necessary to design and model a very complex on-chip electrical environment dominated by wires. In this tutorial, we describe the latest design and analysis approaches to ensuring the electrical integrity of today's systems-on-a-chip, tackling emerging problems such as inductance, substrate coupling, and power-supply integrity. This tutorial is designed for a target audience consisting of VLSI designers, managers, CAD tool developers, R&D engineers, and academic researchers. The goal is to enable attendees to address key interconnect-centric issues including all aspects of signal integrity, inductive effects, and high-performance clock and power distribution.

Description: We begin by describing the design and analysis techniques for signal integrity in deep submicron designs. We introduce the overall design flow and fundamental theories and concepts of RC/RLC interconnect analysis. We discuss the effects of capacitive and inductive coupling on line delay and noise. Design techniques to minimize capacitance and inductance effects are explored. In terms of analysis, we describe interconnect macromodeling in a static noise analysis framework. We also focus on inductance estimation, extraction, and analysis.

The impact of environmental factors including variations in power supply voltage, temperature, and physical factors due to process variations also affect the cycle time and design robustness. Large die sizes and higher operating frequencies, coupled with large on-die variations at reduced device geometries, call for special consideration of this type of “noise”.

We then consider power supply integrity analysis for systems-on-a-chip, including IR and Ldi/dt analysis with full consideration of decoupling capacitance, switching activity, and package models. Power distribution methodologies will be discussed. Substrate coupling is also becoming an important new design and analysis concern for mixed-signal designs. Substrate effects will be considered in the context of substrate noise analysis, latch-up and ESD analysis, RF device modeling, and high-frequency interconnect analysis (current returns through the substrate). In addition to analysis, we will also consider design techniques for limiting all of these coupling interactions.

We will survey various clock distribution approaches and the applicability for large SoC designs. We will compare approaches such as H-tree, mesh, grid for a typical design in terms of requirements including local/global skew, jitter, slew rates, power, buffer area, clock wiring resources, and shielding area. We will review the latest approaches for clock distribution networks including usage of de-skew units to reduce the clock skew.

Throughout the tutorial we will consider measurement techniques and structures for calibrating and characterizing the on-chip electrical environment with an emphasis on interconnect and substrate effects. This is important for technology characterization, yield analysis, and modeling validation.