Simulation and Optimization of the Power Distribution Network in VLSI Circuits

G. Bai, S. Bobba and I. N. Hajj
Coordinated Science Lab & ECE Dept.
University of Illinois at Urbana-Champaign
Urbana, Illinois 61801
E-mail: {gengbai,bobba, i-hajj}@uiuc.edu

Abstract

In this paper, we present simulation techniques to estimate the worst-case voltage variation using a RC model for the power distribution network. Pattern independent maximum envelope currents are used as a periodic input for performing the frequency-domain steady-state simulation of the linear RC circuit to evaluate the worst-case instantaneous voltage drop for the RC power distribution networks. The proposed technique unlike existing techniques, is guaranteed to give the maximum voltage drop at nodes in the RC power distribution network. We present experimental results to compare the frequency-domain and time-domain simulation techniques for estimating the maximum instantaneous voltage drop. We also present frequency domain sensitivity analysis based decoupling capacitance placement for reducing the voltage variation in the power distribution network. Experimental results on circuits extracted from layout are presented to validate the simulation and optimization techniques.

1 Introduction

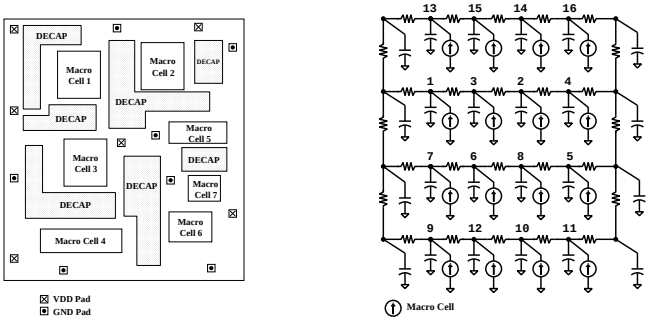
With the increasing levels of integration and the associated increase in the current demand, power delivery is becoming a critical design concern. The parasitics associated with the power distribution network and the time-varying circuit current demand result in a time-varying voltage drop/ surge at nodes in the power distribution network. This voltage variation in the power distribution network can have an adverse impact on the performance and the reliability of a circuit. The delay of the logic gate increases with a drop in the effective supply voltage to the logic gate. This can occur due to a voltage drop at the power bus contact and/ or a voltage surge at the ground bus contact of the logic gate to the power distribution network. With the increasing clock frequency, the time period and the timing margins are reduced. Therefore, any uncertainty in the gate delay has to be modeled and accounted for in the design process. With the reduced supply voltages in scaled technologies, the gate delay becomes sensitive to the supply voltage variations. For a fixed percentage of allowable voltage variation, the absolute magnitude of the allowable voltage variation decreases with the scaled supply voltages. In addition, the rapid current transients and increasing dominance of the interconnect parasitics in scaled technologies further complicate the design of a reliable power delivery network. Also, excessive voltage variations degrade the noise margins and in extreme cases can cause logic failures. Hence, techniques that can accurately estimate the worst-case voltage variations and optimize the power distribution network to reduce the voltage variations are required. This is the focus of the paper.

The number of nodes in the power distribution network can be extremely large because the power distribution network connects to every transistor in an integrated circuit. But a power-bus is typically designed as a hierarchical structure in which the top-level power-grid connects to the macro-blocks and the power distribution network inside the macro-block connects to the logic gates. Power-bus analysis techniques exploit this hierarchical structure by splitting the problem into evaluation of the current signature of each macro-block (non-linear devices) and the use of these currents to analyze the linear top-cell power distribution network to estimate the voltage variation waveforms. These waveforms are then propagated back to compute the voltage drop at nodes inside the macro-blocks by using a current signature for each logic-gate (non-linear device). Hence the power-bus analysis can be treated as a problem in which there are reference nodes with voltage waveforms, current sources that inject/ draw current and the parasitics associated with the power distribution network. All existing techniques [1, 2, 3, 4, 5, 6] and the proposed technique use the hierarchical abstraction with minor variations.

The power-bus analysis techniques [1, 2, 3, 4], compute the IR drop at nodes in the power distribution network by using the macro-block currents as a DC current obtained heuristically, or a DC current obtained by logic simulations for a few vectors or a transient current waveform obtained by simulations for a few vectors. The power-bus analysis techniques [5, 6] use the peak/ average current or the current waveform obtained by simulations for a few vectors to approximate a heuristically constructed triangular or trapezoidal macro-block current waveform. This macro-block current waveform is then used to estimate the voltage drop at nodes in the power distribution network with RLC models by simulation or by a heuristic algorithm that performs a lookup of a pre-characterized waveform library. All the above techniques simulate the power distribution network with R/ RC/ RLC models using macro-block current waveforms obtained heuristically or by simulation for a few vectors and are not guaranteed to generate the worst-case or even the best-case voltage variation at nodes in the power distribution network. The reason for this and other limitations of the existing techniques are described in Section 2.

In our proposed technique, we use a pattern-independent

upper-bound estimate of the macro-block current waveform to simulate for the worst-case voltage drop of the R/ RC power distribution network. This is described in Section 2. In Section 3, we present the frequency-domain steady-state simulation techniques to estimate the worst-case voltage drop of the RC power distribution network. Unlike the existing techniques, the proposed method is guaranteed to generate the worst-case voltage drop at nodes in the RC power distribution network. In addition, we present a frequency-domain sensitivity analysis for the optimal placement of decoupling capacitors to minimize the voltage drop at nodes in the power distribution network. This is described in Section 4. In Section 5, we present the experimental results for the simulation and the optimization techniques described in the paper. Finally, in Section 6 we present the conclusions.



(a) (b)

Figure 1: (a) Macro-blocks with on-chip decoupling capacitances and power pads (b) Equivalent circuit model for the top-cell

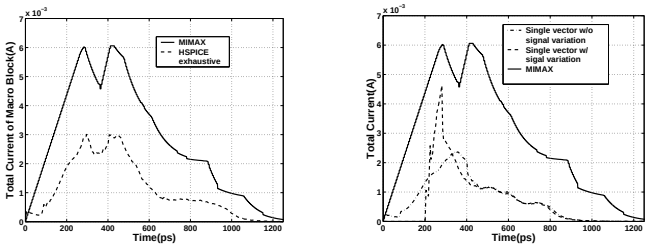
2 Problem Formulation

The voltage variation at nodes in the power distribution network is the response to the time-varying current drawn/ injected by the logic gates in the circuit. Since the logic gate delay is a function of instantaneous supply voltage, estimates of the worst-case instantaneous voltage variation are required at nodes in the power distribution network. In this section, we describe the electrical models of the power distribution network and the input current excitation required to capture the worst-case voltage variations. The hierarchical power-bus analysis divides the problem into the analysis of the top-cell and the analysis of the power distribution network within each macro-block. Accurate electrical models for the top-cell and macro-block power distribution networks are required to capture the worst-case instantaneous voltage drop.

The simplest electrical model for the power distribution network is the resistive power-bus model. Although it simplifies the power-bus analysis, the results are accurate only if the resistance effect dominates the capacitive and inductive effects. A resistive model for the top-cell power distribution network does not take into account the presence of significant on-chip decoupling capacitance that helps to reduce the voltage drops. IR drop analysis with a resistive model has very limited applicability in the optimization of the decoupling capacitors for reducing the supply voltage variations. In our analysis, the RC models are used for the top-cell power distribution network. Fig. 1a shows the top level view of the macro-blocks with on-chip decoupling capacitances and the power pads. Fig. 1b shows the equivalent circuit model of the top-cell power distribution network. Using the Vdd pads as the reference nodes and reversing the direction of the current yields the equivalent circuit that can be used to estimate the voltage variation (drop) at nodes in the power bus. This transformation results in identical formulations for both the analysis of the power and ground buses. For simplicity, in the remainder of this paper the analysis of the power-bus (Vdd) is assumed and we refer to the voltage variation as voltage drop. Note that Fig. 1b does not contain the package inductances and other package parasitics. This is because in a well designed power distribution network, the high-frequency components of the current demand or the cycle-cycle changes in the current demand are predominantly met by the on-chip decoupling capacitance. Since, our goal is to analyze and design the on-chip power distribution network such that the voltage variations are within bounds, we use only a RC model. Note that this analysis can only capture the voltage variations due to the high-frequency components of the current demand and does not include the variations due to the low-frequency components of the current demand. An RC model for the on-chip power distribution network is sufficient because the high-frequency components of the current excitation find a low impedance path through the on-chip capacitances when compared with the impedance of the package inductances for a well designed power bus. If the high-frequency current components with significant magnitude pass through the package inductance, there will be significant undesirable Ldi/dt drop and electromagnetic interference (EMI). We also assume that the top-cell power and the ground grids are designed to enhance the mutual inductance which mitigates the effect of on-chip inductance. We assume that all nodes in the power distribution network have a capacitance to the reference node. In addition, the capacitance at the contact point of each macro-block to the top-cell power distribution network consists of effective intrinsic decoupling capacitance of the macro-block [5] and any additional decoupling capacitance placed at the macro-block.

The IR drop analysis can be used to estimate the voltage drop at nodes inside the macro-block. This is justified by the following reasons. The power delivery network inside a macro-block would most likely be routed on the more resistive lower metal layers. In addition, the effect of the intrinsic decoupling capacitance of a macro-block has already been accounted for in the top-cell simulation. Hence, in this paper we assume that the IR drop analysis for nodes in each macro-block is performed after the voltage waveforms at the contact point(s) of a macro-block to the top-cell power distribution network are computed. The worst case voltage drops at nodes in the macro-blocks are obtained using VMAX [7].

The time-varying current drawn by a macro-block is dependent on the switching activity of the logic gates in the macro-block and hence on the input vectors applied to the macro-block. This implies that the voltage variations at nodes in the power distribution network are also input pattern dependent. The input pattern dependence makes the problem of estimating the worst-case voltage variation a hard problem. Simulation of the macro-blocks with a sub-set of the exponential input patterns is not guaranteed to give the maximum current for the macro-blocks or the worst-case



(a) (b)

Figure 2: Macro-block maximum current envelope (a) Comparison with exhaustive SPICE simulation (b) Simulation with input signal variation

voltage variations at nodes in the power distribution network. In this work, we use the maximum current envelope for the macro-blocks which is an upper-bound over the current drawn by the macro-block. This is described in the next sub-section.

2.1 Maximum current envelope for macro-blocks

The maximum current envelope for a macro-block is defined as the instant-wise upper bound over all possible current waveforms drawn by a macro-block in a clock-cycle. The significance of the maximum current envelope lies in its use to estimate the worst-case voltage drop and it will be described in subsequent sections. Simulation based methods that are used to estimate the macro-block current waveforms [1, 2, 3, 4, 5, 6] and techniques that implicitly search the exponential search space for maximum current [8, 9] can only generate a lower bound estimate of the maximum current envelope given finite computational resources. Pattern independent techniques [10, 11] can be used to estimate a tight upper-bound on the maximum current waveform. In this paper, the maximum current envelopes are obtained using MIMAX [11] for static multi-level circuits. The MIMAX technique accounts for some of the spatio-temporal dependencies to generate a tight upper-bound on the maximum current envelope and it does not possess the complexity of input enumeration [10].

The advantage of using MIMAX is that the variation in gate delay due to supply voltage variations, process variations and uncertainty in simulation parameters such as slew-rate or signal arrival time can be included to obtain an upper-bound current waveform. This is hard to include in a simulation based methods. But the use of excessive uncertainty in the gate delay values can result in pessimistic current envelope waveforms. Fig. 2(a) shows the comparison of the current envelope waveform of a macro cell using MIMAX and SPICE exhaustive simulation. The peak current from the hspice exhaustive simulation is 3mA. But the maximum instantaneous current increases to 4.5mA after considering the signal statistical variation effects as shown in Fig. 2(b). Hence, it can be seen that the MIMAX technique can be made to account for parameter variations.

2.2 Maximum voltage drop waveform with RC models

In [10], it was shown that simulation of the R/ RC power distribution network starting from the initial condition of zero voltage drop with a current excitation that is an instant-wise upper-bound on the current waveform for all input vectors yields the maximum voltage drop waveform. Use of average currents or current values obtained by simulation [1, 2, 3, 4, 5, 6] for a small number of input vectors is not guaranteed to give the worst-case voltage drop. Since the maximum envelope currents are an upper-bound over the current drawn by the macro-blocks for all possible vectors, simulation of the top-cell RC power distribution network with the maximum envelope currents would give the worst-case voltage drop. If the voltages at all nodes in the top-cell are restored to zero voltage drop by the end of a clock cycle, then simulation of the RC power distribution network for one cycle is sufficient to capture the worst-case voltage drop. In case all the nodes voltages are not restored to zero voltage drop, then simulation of the RC power distribution network for one or more cycles would be required to estimate the worst-case voltage drop. This is because the maximum voltage drop in the next cycle can be greater than or equal to the maximum voltage drop in the previous cycle. Therefore, simulation has to be performed till the initial and the final voltage drop values at all nodes are equal. This problem is precisely the problem of finding the steady-state response of a linear circuit with a periodic input excitation. The maximum current envelope waveform of the macro-blocks is duplicated in each cycle resulting in a periodic input. In the next section, steady state simulation techniques are described.

3 Steady-state Simulation Techniques

A complete description of several steady-state simulation techniques can be found in [12]. Note that the steady-state simulation is performed to obtain the worst-case instantaneous voltage drop at nodes in the top-cell power distribution network. With a RC power bus model, simulation of the network for one cycle to obtain the worst-case voltage variations requires the knowledge of the initial conditions that is also a boundary condition. With no apriori knowledge of the initial condition, the steady state solution can be obtained by simulating the circuit with arbitrary initial conditions for a large number of cycles till the initial and the final conditions for a time-period are identical. One approach is to assume an initial condition of zero voltage drop at all nodes, duplicate the envelope currents for N cycles and simulate the network for N cycles. At the end of N cycles the transient effect of the initial condition dies down and the circuit reaches steady state. Since we applied a current waveform (for N cycles) that is a instant-wise upper-bound over the current drawn by the circuit, we are guaranteed to get the worst-case voltage drop. The computation time for this approach can be significant for large power distribution networks. An alternate approach is the frequency-domain technique in which the periodic current waveform is transformed to the frequency domain to compute the voltages in the frequency domain. These voltages can then be transformed to the time domain to get the steady-state solutions.

When the current waveforms and the node voltage waveforms can be accurately approximated by a Fourier series, the frequency-domain steady-state simulation techniques [12] can be used. Fig. 3 shows the frequency spectrum of the periodic maximum current envelope waveform of a macro-block. From the plot, it can be seen that the frequency components consist of the fundamental frequency corresponding to the

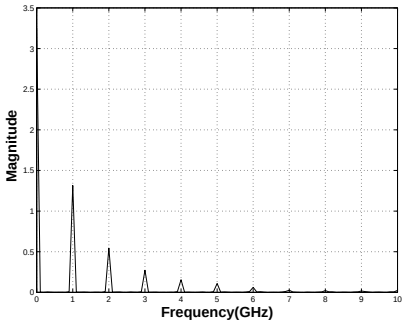


Figure 3: Frequency spectrum of macro-block current waveform

time-period and the higher-order harmonics. At each frequency point in the spectrum for the macro-block current waveforms, the complex admittance matrix is formulated and the node voltages are evaluated. After the node voltages in the frequency domain are computed, they are transformed to the time domain. Since a RC network is a low-pass filter structure, the node waveforms can be approximated closely by sinusoids. Hence, the frequency-domain simulation techniques can be used without a significant loss in accuracy. In section 5, we present experimental results to compare the accuracy and run-time of time-domain techniques and the frequency-domain techniques.

4 Sensitivity Analysis based Power Grid Optimization

One of the techniques to reduce the maximum voltage drop is the judicious placement of on-chip decoupling capacitances. In [5], a decoupling capacitance optimization procedure that iterates between circuit simulation and floor-planning is presented. But techniques for finding the optimal location for the placement of decoupling capacitances are not described. In this section, we present computational techniques for determining power bus sensitivities in the frequency domain [13], which are then used to determine the optimal locations for placement of decoupling capacitances. The physical design issues of the availability of area for decoupling capacitance are not explicitly considered here. If due to some constraints the decoupling capacitance cannot be placed or increased in value, then that node is not used in the sensitivity analysis as a possible candidate. We refer to a violation node as a node with voltage drop beyond a certain threshold.

There are two scenarios in which the sensitivity analysis can be applied:

- Find the sensitivity vector of the voltage drop on one node with respect to a small change in decoupling capacitances at all nodes in the power bus.
- Obtain voltage drop variation of all the violation nodes if one or more decoupling capacitances are changed arbitrarily.

Small change sensitivity analysis is applied in the first case and the large change sensitivity analysis is applied in the second case.

4.1 Small Change Sensitivity Analysis

The goal of small change sensitivity analysis is to find the sensitivity vector of one node voltage to all the capacitance on the power bus. Consider the linear equations of power bus in the form,

$$\mathbf{A}\mathbf{v} = \mathbf{i} \tag{1}$$

where $\mathbf{A}$ is conductance and capacitance matrix of power bus network, $\mathbf{v}$ is the vector of bus node voltages, $\mathbf{i}$ is the vector of current sources connected to the nodes on the power bus. In the frequency domain, $\mathbf{A}$ is complex for the RC power bus model.

Let the voltage drop of the interested node V_j expressed as:

$$V_j = \mathbf{e_j}^{\mathbf{T}}\mathbf{v} \tag{2}$$

where $\mathbf{e_j}^{\mathbf{T}}$ is a unit vector. Our objective is to compute the sensitivity of V_j with respect to all decoupling capacitances $\mathbf{p}$,

$$\frac{\partial V_j}{\partial \mathbf{p}} = \mathbf{e_j}^{\mathbf{T}}\frac{\partial \mathbf{v}}{\partial \mathbf{p}} \tag{3}$$

We differentiate Equation (1) with respect to $\mathbf{p}$ and substitute $\partial\mathbf{v}/\partial\mathbf{p}$ in Equation (3):

$$\frac{\partial V_j}{\partial \mathbf{p}} = -\mathbf{e_j}^{\mathbf{T}}\mathbf{A}^{-1}(\frac{\partial \mathbf{A}}{\partial \mathbf{p}}\mathbf{v} - \frac{\partial \mathbf{i}}{\partial \mathbf{p}}) = -\mathbf{U}(\frac{\partial \mathbf{A}}{\partial \mathbf{p}}\mathbf{v} - \frac{\partial \mathbf{i}}{\partial \mathbf{p}}) \tag{4}$$

Adjoint vector $\mathbf{U}$ is defined through the relation:

$$\mathbf{A}^{\mathbf{T}}\mathbf{U} = \mathbf{e_j} \tag{5}$$

$\partial\mathbf{i}/\partial\mathbf{p}$ is 0 since $\mathbf{i}$ is independent of decoupling capacitances in the frequency domain. From the final solution $\partial V_j/\partial\mathbf{p}$, we can find the locations for decoupling capacitance which are most effective in decreasing the voltage drop on node j.

4.2 Large Change Sensitivity Analysis

In general, there can be many different locations available for the placement of decoupling capacitances. The goal of large change sensitivity is to find the voltage drop variation of all the violation nodes with respect to one or more of the decoupling capacitance perturbances. Using this result, we can determine which location would be the best choice for the placement of the first decoupling capacitance. To simplify the explanation, we use only one decoupling capacitance variation. Similar techniques can be applied to consider the effect of several decoupling capacitances at the same time.

Assume that the decoupling capacitance at node j has Δc_j perturbance. The new matrix $\mathbf{A_{new}}$ can be expressed as:

$$\mathbf{A_{new}} = \mathbf{A} + \mathbf{e_j}\Delta c_j \mathbf{e_j}^{\mathbf{T}} \tag{6}$$

The new linear system $\mathbf{A_{new}}\mathbf{v} = \mathbf{i}$ can be expressed in matrix form:

$$\begin{bmatrix} \mathbf{A} & \mathbf{e_j} \\ \mathbf{e_j}^{\mathbf{T}} & -(j\omega\Delta c_j)^{-1} \end{bmatrix} \begin{bmatrix} \mathbf{v_{new}} \\ \mathbf{z} \end{bmatrix} = \begin{bmatrix} \mathbf{i} \\ 0 \end{bmatrix} \tag{7}$$

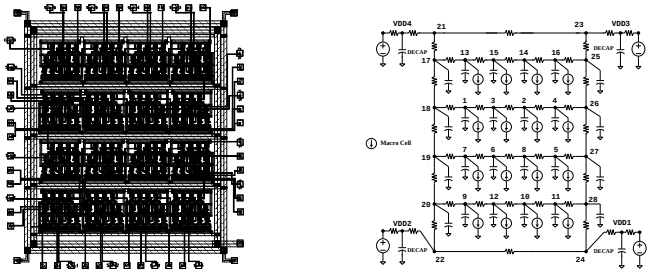
Assume $\mathbf{v_0}$ is the unperturbed solution and adjoint vector $\tilde{\mathbf{P}} = \mathbf{A}^{-1}\mathbf{e_j}$. The perturbed solution is:

$$\mathbf{v_{new}} = \mathbf{v^0} - \tilde{\mathbf{P}} * \mathbf{z} \tag{8}$$

where

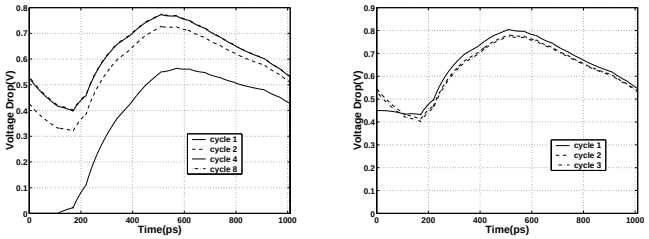
$$\mathbf{z} = \frac{\mathbf{e_j^T}\mathbf{v^0}}{\mathbf{e_j^T}\tilde{\mathbf{P}} + (j\omega\Delta c_j)^{-1}} \tag{9}$$

After large change sensitivity analysis, the voltage drop variation of violation nodes in frequency domain is transformed back to time domain. We can find the total voltage drop decrease of all the violation nodes due to Δc_j perturbance. The



(a) (b)

Figure 4: (a) Layout and (b) Extracted top-cell power bus schematic of the adder circuit



(a) (b)

Figure 5: (a) Time-domain simulation with zero initial condition (b) Time-domain simulation with an improved initial condition

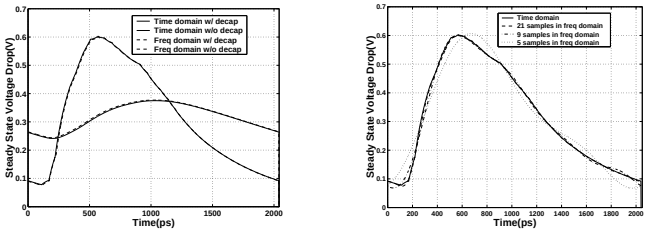
location which causes the maximum voltage decrease at the violation nodes is the first choice for decoupling capacitance placement.

The small change and large change sensitivity analysis can be used iteratively for finding the optimal decoupling capacitance placement locations. When the number of violations are small, one can start with small change sensitivity analysis to fix a voltage drop violation. But after adding certain amount of decoupling capacitance, the system behavior can be different and the effectiveness of the decoupling capacitance should be verified by large change sensitivity analysis. When the number of possible locations for the placement of the decoupling capacitance are small, the large change sensitivity analysis can be used effectively to find the most optimal location for adding the decoupling capacitance.

5 Experimental Results

Experimental results are presented for a 16-bit pipelined static CMOS adder using 0.35μM, 3V technology. The RC interconnect parasitics of the power-bus are extracted from the layout. The simplified top level power bus schematic is shown in Fig. 4. The effective intrinsic decoupling capacitance of each macro-block is included at the contact point of the macro-block to the top-cell power distribution network. The maximum current envelope for the macro-blocks is obtained using MIMAX [11]. We present the simulation results using the time-domain and frequency-domain steady-state simulation techniques and the sensitivity based decoupling capacitance optimization for this circuit.

Fig. 5a shows the voltage drop waveform at a node by time-domain simulation of the top-cell for different number of cycles using the periodic maximum current envelope waveforms starting with an initial condition of zero voltage drop. From the plot, it can be seen that after 4 cycles, the initial voltage drop value is the same as the final voltage drop



(a) (b)

Figure 6: Time and frequency domain simulation comparison

value. Hence, the voltage drop becomes periodic after 4 cycles. Observe that the voltage drop is maximum in the steady state and is much higher than the voltage drop obtained by simulating for one cycle. Fig. 5b shows the voltage drop waveform at the same node by time-domain simulation of the top-cell for different number of cycles using the periodic maximum current envelope waveforms starting with a better initial voltage drop. From the plot, it can be seen that after 3 cycles the voltage drop becomes periodic. Hence, the convergence time can be improved by using better initial conditions. In general, the number of cycles required to reach steady-state is dependent on the power distribution network and the initial conditions.

In order to perform simulation and sensitivity analysis in the frequency domain, the periodic time domain maximum current envelope waveforms are transformed into frequency domain. As shown in Fig. 3, the frequency spectrum of MCE of the macro-blocks has a very strong DC and low frequency components. The amplitude of high frequency components dies down very quickly. Solving the complex admittance matrix only for DC and few low frequency components will be sufficient to determine voltage drop frequency spectrum for all the nodes. An iterative solution technique that solves for additional frequency components till the corresponding time-domain waveforms do not change significantly can be used to determine the number of frequency components required for an accurate solution. Using this approach for a power-bus in which the resistance effect dominates may require the solution for the DC component alone. Since we use the MCE, the IR drop solution would be an upper-bound and is an improvement over the techniques proposed in [1, 2, 3, 4].

Fig. 6(a) shows the comparison of time and frequency domain analysis with and without adding extra decoupling capacitances. It can be seen that adding the extra decoupling capacitance makes the power-bus stiffer and lowers the voltage variation in the power bus. The waveforms obtained by time and frequency-domain techniques closely follow the other. Fig. 6(b) shows the frequency domain simulation results only considering low frequency components of macro-block MCE. In this figure, the curve using 9 frequency components closely follows the time domain solution. Hence, frequency-domain analysis can be used to obtain accurate results at a considerably less computational cost when compared with time-domain analysis. Table 1 shows a comparison of the worst-case voltage drop at various nodes using time-domain and frequency-domain simulation techniques. It can be seen that the frequency and time-domain techniques generate almost identical results. The simulation time on a SunUltra5 workstation to find steady state maximum voltage drop in the time-domain and the frequency domain

Table 1: Comparison of worst-case voltage drops using time-domain and frequency domain techniques

Node	Time Domain (V)	Freq. Domain (V)
12	0.8095	0.7973
9	0.6707	0.6830
13	0.7610	0.7584
15	0.8155	0.8040
14	0.7728	0.7713
16	0.6412	0.6603
4	0.8057	0.7989
2	0.8620	0.8427
3	0.8202	0.8080
1	0.6882	0.6966
7	0.8150	0.8040
6	0.8685	0.8478
8	0.8246	0.8139
5	0.6875	0.7021
11	0.7749	0.7720
10	0.8455	0.8269

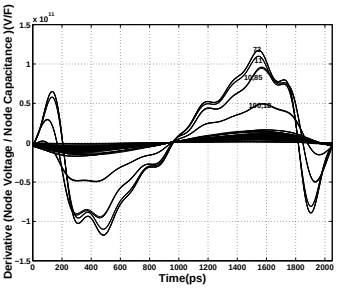


Figure 7: Small change sensitivity curves of one specified node

are 31.53 CPU seconds and 2.16 CPU seconds respectively.

Small change sensitivity analysis is performed to identify locations for adding the decoupling capacitances which are most effective in decreasing the voltage drop at a specified node. As a example, node 72 which is the contact point of the macro-block connecting to the power distribution network at node 11 is chosen. Its sensitivity curves to other nodes are plotted in Fig. 7. From the figure, it can be seen that the location of the additional decoupling capacitance with respect to the violated nodes plays an important role in decreasing the voltage drop. The small signal sensitivity results would be more useful when the number of nodes with violations is small.

Large signal sensitivity analysis is performed to determine the voltage drop decrease at all other nodes for an increase in the decoupling capacitance by Δc at a node. The summation of the voltage drop decrease of all the violation nodes is used as a metric to identify the optimal node to add the decoupling capacitance. Fig. 8 shows this information for several nodes in Fig. 4. From the plot, it can be seen that node 2 is the best location to put the decoupling capacitance. The optimal node is dependent on the topology, RC parameters and the maximum current envelope of the macro-blocks. If there are any violation nodes after one iteration, the sensitivity analysis can be repeated to find the next optimal node.

6 Conclusions

In this paper, we presented techniques to estimate the worst-case voltage variation using a RC model for the power distribution network. This was accomplished by using the maximum envelope current of the macro-blocks as a periodic input and performing steady-state simulation to evaluate the worst-case instantaneous voltage drop. We presented a comparison of time-domain and frequency-domain steady-state simulation techniques for estimating the voltage drop for RC power distribution networks. We also presented frequency domain sensitivity analysis based decoupling capacitance placement for reducing the voltage variation in the power distribution network.

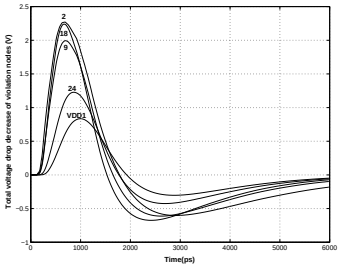


Figure 8: Total voltage drop decrease of violation node due to one decoupling capacitance on nodes 2, 18, 9, 24 or VDD1

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