ABSTRACT

In this paper, we propose a novel twisted-bundle layout structure for minimizing inductive coupling noise. In this structure, we create several routing regions and re-order the routing of nets in each of these routing regions. The purpose is to create complementary and opposite current loops in the twisted-bundle layout structure, such that the magnetic fluxes arising from any signal net within a twisted group cancel each other in the current loop of a net of interest. The effectiveness of the twisted-bundle structure in minimizing coupling inductance has been verified by the application of FastHenry extraction on a 16-bit bus structure. We achieve about two orders of magnitude reduction in inductive coupling. SPICE simulations also show that the 16-bit twisted-bundle bus structure is able to maintain high signal integrity at high frequency of operation.

1. INTRODUCTION

Continued scaling of semiconductor technology has brought the issues of interconnect-limit designs to the forefront. The International Technology Roadmap for Semiconductor (ITRS) [1] forecasts that as the VLSI technology advances towards giga-Hertz on-chip frequency and system-level integration on larger die size, self- and coupling-inductances are becoming dominant factors in determining signal delay and signal integrity.

Ref. [16] gave an extensive survey of various noise sources in circuit design. Predominantly, existing studies focused on crosstalk noise due to capacitive coupling. Due to the short range effect of capacitive coupling, techniques such as shielding, net ordering or track permutation have proved to be effective in minimizing capacitive cross-talk noise [6; 17].

On the other hand, inductive effects have a long range effect because they arise from the electromagnetic phenomenon of magnetic flux linking current loops. As a result, inductive noise has a much wider spatial effect than that of a capacitive noise. For this reason, it makes the worst case situation in a circuit much harder to predict. Many of the existing studies that dealt with on-chip inductive effects focused primarily on the modeling and extraction of on-chip interconnect inductance. In [15], loop inductance was calculated in terms of partial inductances defined for wire segments. The Partial Element Equivalent Circuit (PEEC) model was widely used to analyze on-chip inductance [7; 14; 4]. In [9], frequency dependent inductance and resistance were computed based on the magnetoquasistatic assumption, and in [10], a simple layout rule-based method was used to speed up the computation.

A few recent studies have reported success in minimizing the undesirable inductive effects. In recent Alpha chip designs [2], on-chip inductance was limited by sandwiching lines with high current density between isolating metal planes. In [11], the wiring overhead was reduced by using a interdigitated layout structure, in which a wide wire was split into many lines, interspersed with ground lines. These techniques, however, considered only self-inductance. In [8], inductive coupling noise was reduced by shield insertion and net ordering.

In this paper, we propose a novel twisted-bundle layout structure for minimizing inductive coupling noise. By creating complementary and opposite current loops in the layout structure, we achieve two orders of magnitude reduction in inductive coupling. The abilities of the twisted-bundle structure in minimizing coupling inductance and maintaining high signal integrity have been verified by the applications of FastHenry extraction and SPICE simulations on a 16-bit bus structure.

The rest of the paper is organized as follows. In Section 2, preliminaries regarding inductive coupling are explained. In Section 3, we introduce a twisted-pair layout structure, upon which the twisted-bundle structure is based. In Section 4, we present the novel twisted-bundle structure and a systematic approach for synthesizing such a structure. In Section 5, we apply this structure to a 16-bit bus design and compare it with the “traditional” design based on the parasitic parameters extracted by FastHenry and the simulation results by SPICE. Finally, we conclude in Section 6.

2. PRELIMINARIES

Mutual inductances, as well as self-inductance, are electromagnetic phenomena that arises from current loops [12; 13]. The inductances for a system of N loops are defined as:

$$L_{ij} = \frac{\psi_{ij}}{I_j}, \quad (1)$$

where $\psi_{ij}$ is the magnetic flux in loop $i$ due to a current $I_j$ in loop $j$. $L_{ij}$ represents the self inductance of loop $i$, whereas $L_{ij}(i \neq j)$ represents the mutual inductance between loops $i$ and $j$.

According to the Faraday’s law, the mutual inductance can be calculated by finding the magnetic flux linking one loop related to per unit of current in the other loop:

$$M = L_{ij} = \int_{S_i} \mathbf{B} \cdot d\mathbf{S}_i / I_j, \quad (2)$$

where $\mathbf{B}$ is the density of the magnetic flux arising from current $I_j$ in loop $i$ and the integration is over the surface of loop $i$.

On-chip signal nets form loops with their current return paths; these loops determine the inductances as shown in Eqns. (1) and (2). Therefore, in order to accurately calculate the inductances of...
on-chip interconnections, it is of critical importance to determine the current return paths of on-chip signal nets. However, it is extremely difficult to find accurate return paths for signal nets, because in the complex interconnection structures that we deal with today, there are several paths through which a current returns [3].

In this work, we assume that all signals use the nearest power/ground line as their return paths [5]. Although quiet or opposite-switching neighboring nets may also serve as return paths, they are not ideal because currents returning from signal wires have to go through devices, which typically have a resistance of several hundred Ohms.

3. TWISTED-PAIR LAYOUT STRUCTURE

From the Faraday’s law, there are two possible ways of eliminating the coupling inductance: (i) by creating a magnetic flux that is of an opposite direction; (ii) by eliminating or minimizing the coupling inductance: (i) by creating a magnetic flux that is continuous everywhere along a signal line. Therefore, the two integrations over $S_{21}$ and $S_{22}$ cancel each other:

$$\int \int \bar{B} \cdot d\mathbf{S}_{22} = -\int \int \bar{B} \cdot d\mathbf{S}_{21};$$

Hence, the mutual inductance between signals 1 and 2 is zero:

$$M = (\int \int \bar{B} \cdot d\mathbf{S}_{21} - \int \int \bar{B} \cdot d\mathbf{S}_{21}) / I_1 = 0. \quad (6)$$

In fact, loop$_{12}$ also contributes to the magnetic flux linkage in $S_{21}$. So does loop$_{11}$ to $S_{22}$. However, their contributions are quite insignificant, as these two components of magnetic flux also cancel each other in the integration. We can similarly argue that $L_{12}$ is zero because the surfaces of the two loops loop$_{11}$ and loop$_{12}$ actually “sum” to zero.

All the preceding discussions are based on the assumption that the current in a signal line is continuous everywhere. However, this assumption is not valid when the wire length is sufficient long for the transmission line effect to kick in. If parallel termination is adopted at the receiving ends of signal lines, there are no or minimal reflections at the receiving ends. Consequently, noises gathered at the victim nets cancel each other when they reach the receiving ends. Hence, the mutual inductance is still zero.

We use FastHenry [9] to verify the effectiveness of the proposed twisted-pair layout structure in minimizing coupling inductance. The wire width, height, length, and spacing are 1$\mu$m, 2$\mu$m, 200$\mu$m, and 1$\mu$m, respectively.

We extract the inductance matrix under two frequencies: a high frequency of $f_H = 10^6$Hz and a low frequency of $f_L = 10^6$Hz. The inductance matrices for a normal or un-twisted structure are given below:

$$f_H = 10^6$Hz

$$\begin{pmatrix}
7.4e-11 & 6.2e-12 \\
6.2e-12 & 7.4e-11
\end{pmatrix}$$

$$f_L = 10^6$Hz

$$\begin{pmatrix}
9.1e-11 & 1.0e-11 \\
1.0e-11 & 9.1e-11
\end{pmatrix}$$

The diagonal elements are the self-inductances, and off-diagonal entries in the matrix are mutual inductances. The inductance matrices for a twisted-pair structure are given below:

$$f_H = 10^6$Hz

$$\begin{pmatrix}
7.3e-11 & 7.6e-17 \\
7.8e-17 & 7.4e-11
\end{pmatrix}$$

$$f_L = 10^6$Hz

$$\begin{pmatrix}
8.9e-11 & 1.0e-16 \\
1.1e-16 & 9.1e-11
\end{pmatrix}$$

The mutual inductances for the twisted-pair structure are about 5 orders of magnitude smaller than the corresponding mutual inductances of the normal un-twisted structure. For all practical purposes, the mutual inductance between signals 1 and 2 is negligible. We also observe that the matrix is not symmetric, i.e., there is a slight discrepancy between $L_{12}$ and $L_{21}$. The difference may have arisen from numerical errors.

4. TWISTED-BUNDLE STRUCTURE

In this section, we generalize the simple twisted-pair structure such that we can minimize the coupling inductances within a multiplesignal bus that has more than two signal lines. As in the twisted-pair structure, we want to create for each current loop, a complementary and opposite current loop such that the resultant magnetic flux linkage in the current loop of a net of interest is zero.

Figure 2 shows a multiple-bit bus with six signal lines and two ground lines. Here, we assume that the top three signal lines of the 6-bit bus share the ground line labeled 0 as their current return from loop$_{11}$, and the magnetic flux linkage in $S_{22}$ is primarily due to loop$_{12}$. As the current directions in loop$_{11}$ and loop$_{12}$ are opposite, the directions of the magnetic fluxes in $S_{21}$ and $S_{22}$ are opposite. Therefore, the two integrations over $S_{21}$ and $S_{22}$ cancel each other:

$$\int \int \bar{B} \cdot d\mathbf{S}_{22} = -\int \int \bar{B} \cdot d\mathbf{S}_{21};$$

Hence, the mutual inductance between signals 1 and 2 is zero:

$$M = (\int \int \bar{B} \cdot d\mathbf{S}_{21} - \int \int \bar{B} \cdot d\mathbf{S}_{21}) / I_1 = 0. \quad (6)$$

In fact, loop$_{12}$ also contributes to the magnetic flux linkage in $S_{21}$. So does loop$_{11}$ to $S_{22}$. However, their contributions are quite insignificant, as these two components of magnetic flux also cancel each other in the integration. We can similarly argue that $L_{12}$ is zero because the surfaces of the two loops loop$_{11}$ and loop$_{12}$ actually “sum” to zero.

All the preceding discussions are based on the assumption that the current in a signal line is continuous everywhere. However, this assumption is not valid when the wire length is sufficient long for the transmission line effect to kick in. If parallel termination is adopted at the receiving ends of signal lines, there are no or minimal reflections at the receiving ends. Consequently, noises gathered at the victim nets cancel each other when they reach the receiving ends. Hence, the mutual inductance is still zero.

We use FastHenry [9] to verify the effectiveness of the proposed twisted-pair layout structure in minimizing coupling inductance. The wire width, height, length, and spacing are 1$\mu$m, 2$\mu$m, 200$\mu$m, and 1$\mu$m, respectively.

We extract the inductance matrix under two frequencies: a high frequency of $f_H = 10^6$Hz and a low frequency of $f_L = 10^6$Hz. The inductance matrices for a normal or un-twisted structure are given below:

$$f_H = 10^6$Hz

$$\begin{pmatrix}
7.4e-11 & 6.2e-12 \\
6.2e-12 & 7.4e-11
\end{pmatrix}$$

$$f_L = 10^6$Hz

$$\begin{pmatrix}
9.1e-11 & 1.0e-11 \\
1.0e-11 & 9.1e-11
\end{pmatrix}$$

The diagonal elements are the self-inductances, and off-diagonal entries in the matrix are mutual inductances. The inductance matrices for a twisted-pair structure are given below:

$$f_H = 10^6$Hz

$$\begin{pmatrix}
7.3e-11 & 7.6e-17 \\
7.8e-17 & 7.4e-11
\end{pmatrix}$$

$$f_L = 10^6$Hz

$$\begin{pmatrix}
8.9e-11 & 1.0e-16 \\
1.1e-16 & 9.1e-11
\end{pmatrix}$$

The mutual inductances for the twisted-pair structure are about 5 orders of magnitude smaller than the corresponding mutual inductances of the normal un-twisted structure. For all practical purposes, the mutual inductance between signals 1 and 2 is negligible. We also observe that the matrix is not symmetric, i.e., there is a slight discrepancy between $L_{12}$ and $L_{21}$. The difference may have arisen from numerical errors.

4. TWISTED-BUNDLE STRUCTURE

In this section, we generalize the simple twisted-pair structure such that we can minimize the coupling inductances within a multiple-signal bus that has more than two signal lines. As in the twisted-pair structure, we want to create for each current loop, a complementary and opposite current loop such that the resultant magnetic flux linkage in the current loop of a net of interest is zero.

Figure 2 shows a multiple-bit bus with six signal lines and two ground lines. Here, we assume that the top three signal lines of the 6-bit bus share the ground line labeled 0 as their current return

![Figure 1: Twisted-pair structure.](image-url)
4.1 Synthesis of Twisted-Bundle

In the twisted-pair structure, the top signal line and the top ground line are twisted to produce the complementary and opposite current loops. In Figure 2, we twist a bundle of the top three signal lines 1, 2, and 3 with the ground line 0, while keeping the bottom three signal lines normal or un-twisted. Hence, we call such a layout structure a twisted-bundle, and refer to the group of nets (signal lines and the ground line) that are twisted the twisted group. The other group of nets that are not twisted is called the normal group.

In the twisted-bundle structure shown in Figure 2, there are four routing regions of equal length in the twisted group. Every signal net in the twisted group goes through the four regions and forms four different loops with the ground line 0. In order to eliminate the mutual inductance, two of the four current loops must form a pair of complementary but opposite loops that are of the same size and of the same distance to the normal group. So do the remaining two current loops. To generate pairs of complementary but opposite loops such that each pair is of the same distance to the normal group, we have to re-order the nets in different routing regions.

Figure 3 illustrates the loops formed by signal 2 and the return path in the four regions. In this example, loop_{23} and loop_{23} cancel each other in the flux linkage of any loop in the normal group, because they are complementary and opposite current loops of the same size, and of the same distance from any loop in the normal group. So do loop_{22} and loop_{24}. Hence, the total flux linkage caused by signal 2 (and its return path 0) to any loop in the normal group is equal to zero. Therefore, the mutual inductance between signal 2 and any signal line in the normal group is zero. We can draw similar conclusions for signals 1 and 3.

4.1 Synthesis of Twisted-Bundle

The basic idea of the twisted-bundle structure is to eliminate the mutual inductances, through intelligent net reordering in different routing regions such that the magnetic flux linkages related to one signal-ground pair in different regions cancel each other in the current loop of a net of interest. As the number of the nets in the normal group does not affect the results, the key issue here is the synthesis of the routing pattern in a twisted group.

The order in which the signal nets appear in the twisted bundle defines a routing matrix. In a routing matrix, a column represents a routing region in which the net order remains unchanged. For example, the twisted group in Figure 2 corresponds to the following routing matrix:

\[
\begin{pmatrix}
0 & 1 & 2 & 3 \\
1 & 0 & 3 & 2 \\
2 & 3 & 0 & 1 \\
3 & 2 & 1 & 0
\end{pmatrix}
\]

In the remainder of this section, we assume that the ground line is labeled 0. We further assume that there are N signal nets labeled 1 through N in the twisted group to be routed. Before we present a systematic approach for synthesizing the routing matrix, we state two observations. First, for the signal nets to be completely routable, each column should be a permutation. Second, in order to generate complementary and opposite current loops, for every signal-ground pair at column i with the signal net, say i, at row y and the ground line 0 at row z, there must exist a column in the matrix such that i is at row z, and 0 at row y. The second observation has two implications:

- There must be at least \((N + 1)\) columns in the routing matrix.
- The ground net 0 must appear in all rows in the routing matrix.

We shall now consider the synthesis of a twisted-bundle structure with a odd number of signal nets (i.e., \(N\) is odd) and a shared, common ground line. We shall use \(N = 7\) to illustrate the idea before presenting the construction of the routing matrix for \(N = 2n - 1\). A twisted-bundle routing matrix for \(N = 7\) is given below:

\[
\begin{pmatrix}
0 & 1 & 2 & 3 & 4 & 5 & 6 \\
1 & 0 & 3 & 4 & 5 & 6 & 7 \\
2 & 3 & 0 & 5 & 6 & 7 & 1 \\
3 & 4 & 5 & 0 & 7 & 1 & 2 \\
4 & 5 & 6 & 7 & 0 & 2 & 3 \\
5 & 6 & 7 & 1 & 2 & 0 & 4 \\
6 & 7 & 1 & 2 & 3 & 4 & 0 \\
7 & 2 & 4 & 6 & 1 & 3 & 5
\end{pmatrix}
\]

For simplicity, we construct the matrix such that the diagonal entries are 0. As a result, the second observation that we stated earlier implies that we should construct a symmetric routing matrix with \((7 + 1) = 8\) columns if at all possible. To fill in the remaining entries of the matrix, we perform the following tasks:

1. Fill in the first column with \(C_1 = [7\ 1\ 2\ 3\ 4\ 5\ 6]^T\) except for the first entry, which is already filled with 0. Displace 7 to the last entry in the column.

2. Perform on \(C_1 = [7\ 1\ 2\ 3\ 4\ 5\ 6]^T\) a cyclic shift-up-by-one to obtain \(C_2 = [1\ 2\ 3\ 4\ 5\ 6\ 7]^T\).

3. Fill in the second column with \(C_2\) except for the second entry, which is already filled with 0. Displace 2 to the last entry in the column.

In general, we perform on \(C_i\) a cyclic shift-up-by-one to obtain \(C_{i+1}\); fill in column \(i + 1\); and displace the \((i + 1)\)-th entry in \(C_{i+1}\) to the last entry in column \(i + 1\). We iterate that process until we reach the 8-th column. By symmetry, we can simply transpose the 8-th row to form the routing matrix given above. Following such a construction, we can synthesize the routing matrix for any odd number \(N = 2n - 1\) of nets (see Figure 4).

Can we apply such construction rules for even number \((N = 2n)\) of signal nets? Observe that in the last row of the routing matrix,
4.2 Caveats

This can be achieved easily by taking \( C_1 \) in the left routing matrix, and swapping 1 with 2, 3 with 4, and in general 2\( i - 1 \) with 2\( i \). \( C'_1 = [2 \ 1 \ 4 \ 3 ... \ 2n - 1 \ 2n - 3] \) is the resultant vector. We can apply the same construction as before to obtain the right routing matrix.

Note that the routing matrix is not unique. An alternative routing matrix can be obtained by simply permuting the columns in the original one.

4.2 Caveats

The twisted-bundle structure can significantly eliminate the coupling inductances between signal nets in the twisted group and the normal group if the assumptions that every signal net in a group share a common return path, and there is a return path for each group hold. If these assumptions are not valid, then the structure may fail to eliminate the mutual inductances between two groups, or can only eliminate a portion of the mutual inductance. For the top few signal nets in the normal group, for example, they are equally close to the ground lines above and below them. In this case, the mutual inductances cannot be eliminated.

The mutual inductances between two groups are significantly reduced. It is natural for one to ask the following question: within a group (be it the twisted group or the normal group), is it possible to reduce the mutual inductances for signal nets within one group as we do between two groups? The answer is no. As long as two signal nets share one common return path, the mutual inductance cannot be reduced by net reordering. We prove this in the following.

There are four relative positions for two signal lines and the common ground line as illustrated in Figure 5. We examine the inductive noise induced by signal 1 on signal line 2. We assume that the current in signal 1 flows from the left to right, and that it is increasing. The inductive noise (emf) on signal 2 will try to counteract the change of magnetic flux in the loop formed by signal 2 and the ground. Therefore, in each of the four cases, the direction of this induced voltage drop on signal 2 is from the right to left, as shown in Figure 5. Hence, the mutual inductance cannot be eliminated.

5. EXPERIMENTAL RESULTS

Based on the twisted-bundle structure, a 16-bit bus is designed, as shown in Figure 6. The 16 signals are divided into four groups, with 4 signals in each group. Twisted groups and normal groups are alternated. To join the adjacent routing regions in the twisted groups, another metal layer is used. Figure 7 shows part of the stick diagram of the twisted group. In a normal group, the ground line is in the middle, sandwiched between two signal lines above it and two below it.

To show the advantage of the twisted-bundle structure, a traditional 16-bit bus, which consists of 4 normal groups, is constructed for comparison. We refer to it as the normal structure. The inductance matrix for the two kinds of buses are shown below. Only the first four columns of the 16x16 matrix are shown. Rows 1 through 4 are for nets within the first group; the rest are the coupling inductance between nets in the first group and the remaining groups. We assume that the buses are \( 2nm \) long. For all the metal wires, the thickness is \( 1\mu m \), and the width and spacing are both assumed
to be 1µm. The spacing between the two metal layers is 1µm. The inductance matrix of the twisted-bundle structure is given below:

\[
\begin{pmatrix}
1.5e-09 & 5.9e-10 & 8.2e-10 & 8.4e-10 \\
5.9e-10 & 1.5e-09 & 8.4e-10 & 8.2e-10 \\
8.2e-10 & 8.4e-10 & 1.8e-09 & 1.1e-09 \\
8.4e-10 & 1.1e-09 & 1.8e-09 & 1.1e-09 \\
3.6e-13 & 5.2e-13 & 5.4e-13 & 1.0e-12 \\
3.6e-13 & 5.2e-13 & 5.4e-13 & 1.0e-12 \\
8.2e-13 & 2.5e-13 & 1.1e-13 & 2.4e-13 \\
8.2e-13 & 2.5e-13 & 1.1e-13 & 2.4e-13 \\
3.6e-13 & 4.4e-13 & 1.9e-13 & 4.1e-13 \\
3.6e-13 & 4.4e-13 & 1.9e-13 & 4.1e-13 \\
3.6e-13 & 4.4e-13 & 1.9e-13 & 4.1e-13 \\
3.6e-13 & 4.4e-13 & 1.9e-13 & 4.1e-13 \\
8.2e-13 & 1.2e-11 & 9.8e-12 & 9.8e-12 \\
8.2e-13 & 1.2e-11 & 9.8e-12 & 9.8e-12 \\
1.1e-11 & 8.7e-12 & 2.7e-11 & 2.1e-11 \\
1.1e-11 & 8.7e-12 & 2.7e-11 & 2.1e-11 \\
5.8e-14 & 1.2e-11 & 2.1e-11 & 2.7e-11 \\
5.8e-14 & 1.2e-11 & 2.1e-11 & 2.7e-11 \\
7.2e-14 & 9.3e-14 & 4.0e-14 & 8.0e-14 \\
7.2e-14 & 9.3e-14 & 4.0e-14 & 8.0e-14 \\
3.3e-14 & 4.3e-14 & 1.9e-14 & 3.7e-14 \\
3.3e-14 & 4.3e-14 & 1.9e-14 & 3.7e-14 \\
2.9e-14 & 3.8e-14 & 1.6e-14 & 3.3e-14 \\
2.9e-14 & 3.8e-14 & 1.6e-14 & 3.3e-14 \\
5.5e-14 & 7.2e-14 & 3.1e-14 & 6.2e-14 \\
5.5e-14 & 7.2e-14 & 3.1e-14 & 6.2e-14
\end{pmatrix}
\]

As we can see, the mutual inductances between signal nets within the first group are similar in both matrices. The mutual inductances between signal nets in the first twisted group and the two normal groups are about two orders of magnitude smaller than those between corresponding nets in the normal structure. The mutual inductances between the two twisted groups are not zero. As the two groups are separated by a normal group, the distance between them makes the mutual inductances smaller than those in the first group.

We also extract the capacitance and inductance values for different wire lengths, and simulate the resulting RLC networks in SPICE using different input patterns at 1GHz and 2GHz signal frequencies. Wire lengths are 1mm, 2mm and 4mm, representing typical top-level global wires between repeaters or gates in high-speed circuits [5]. For all traces, the drivers are 160X of the minimum inverter in a representative 0.18um CMOS technology with 1.5V Vdd, and the receivers are 40X of the minimum inverter.

Table 1 describes the input patterns used in the simulations. We index the signals in a 16-bit bus from 0 to F. Note that wire 0 here is not the ground wire. In this table, ‘r’, ‘f’, and ‘q’ stand for ‘rising’, ‘falling’, and ‘quiet’, respectively. The rise and fall times of the signals are assumed to be one-tenth of the clock period. All

![Figure 5: Two signals sharing a common return path.](image)

![Figure 6: A 16-bit signal bus in a twisted-bundle structure.](image)

![Figure 7: Stick diagram of the layout for a twisted group (not drawn to scale).](image)

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Wire Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pattern 1</td>
<td>0123456789BCDEF</td>
</tr>
<tr>
<td>Pattern 2</td>
<td>0000000000000000</td>
</tr>
<tr>
<td>Pattern 3</td>
<td>0000fffffffff</td>
</tr>
<tr>
<td>Pattern 4</td>
<td>ffffffff0fffffff</td>
</tr>
<tr>
<td>Pattern 5</td>
<td>ffffffff0ffffff</td>
</tr>
</tbody>
</table>

The inductance matrix of the normal structure is given below:

\[
\begin{pmatrix}
1.8e-09 & 8.8e-10 & 4.4e-10 & 6.0e-10 \\
8.8e-10 & 1.2e-09 & 3.2e-10 & 4.4e-10 \\
4.4e-10 & 3.2e-10 & 1.2e-09 & 8.8e-10 \\
6.0e-10 & 4.4e-10 & 8.8e-10 & 1.8e-09 \\
7.0e-11 & 4.2e-11 & 7.3e-11 & 2.3e-10 \\
2.8e-11 & 1.6e-11 & 2.6e-11 & 7.3e-11 \\
2.0e-11 & 1.1e-11 & 1.6e-11 & 4.2e-11 \\
3.4e-11 & 2.0e-11 & 2.8e-11 & 7.0e-11 \\
1.6e-11 & 9.0e-12 & 1.1e-11 & 2.6e-11 \\
7.3e-12 & 4.0e-12 & 5.0e-12 & 1.1e-11 \\
6.1e-12 & 3.3e-12 & 4.0e-12 & 9.0e-12 \\
1.1e-11 & 6.1e-12 & 7.3e-12 & 1.6e-11 \\
7.2e-12 & 3.8e-12 & 4.4e-12 & 9.6e-12 \\
3.3e-12 & 1.8e-12 & 2.0e-12 & 4.4e-12 \\
2.9e-12 & 1.6e-12 & 1.8e-12 & 3.8e-12 \\
5.6e-12 & 2.9e-12 & 3.3e-12 & 7.2e-12
\end{pmatrix}
\]
switching signals switch at the same time. Table 2 shows the noise levels measured at the far end of the victim signal B. From the simulation results, we observe that the twisted-bundle structure can effectively reduce the coupling noise. For 1mm wire, we achieve 4% to 72% noise reduction; for 2mm wire, 18% to 76%; and for 4mm wire, 20% to 75%. Similar results are obtained when we use input patterns obtained by substituting ‘f’ for ‘t’ and ‘t’ for ‘f’ in the five input patterns listed in Table 1.

The impact of the twisted-bundle structure on signal delay is also investigated. The input patterns are similar to those in Table 1 except that signal B is also switching (both high and low) instead of being quiet. Table 3 summarizes the maximum delays found for the twisted-bundle and normal structures. The second and third columns in Table 3 list the maximum delays of nets in the twisted groups and normal groups of the twisted-bundle structure, respectively; the fourth column lists the maximum delays of nets in the normal structure. Although every wire in a twisted group has a longer wire length, a higher resistance, and a higher capacitance than wires in a normal group, the simulation results show that wire twisting has minimal impact on the maximum delays. The maximum delays for twisted wires and normal wires in the twisted-bundle structure do not differ by more than 10%. The differences between the maximum delays of the twisted structure and normal structure are even smaller.

6. CONCLUSION

In this paper, we present the twisted-bundle layout structure. Inductance extraction with FastHenry shows the effectiveness of this structure in minimizing mutual inductance. SPICE simulation results also show that it can considerably reduce the coupling noise.

7. REFERENCES


Acknowledgment

We thank Mr. Haoran Wang of Purdue University for his help in preparing this manuscript.

Table 2: Comparison of noise levels between the twisted-bundle and normal structures.

<table>
<thead>
<tr>
<th>Length (mm)</th>
<th>Input Pattern</th>
<th>Noise (V) freq=1GHz</th>
<th>Normal</th>
<th>Twisted</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Twisted</td>
<td>Normal</td>
<td>Twisted</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0.05</td>
<td>0.17</td>
<td>0.07</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>0.23</td>
<td>0.25</td>
<td>0.32</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>0.13</td>
<td>0.16</td>
<td>0.18</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>0.23</td>
<td>0.26</td>
<td>0.38</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>0.12</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0.09</td>
<td>0.36</td>
<td>0.11</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>0.38</td>
<td>0.46</td>
<td>0.44</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>0.18</td>
<td>0.35</td>
<td>0.23</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>0.37</td>
<td>0.47</td>
<td>0.44</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>0.18</td>
<td>0.34</td>
<td>0.23</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0.14</td>
<td>0.55</td>
<td>0.15</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>0.51</td>
<td>0.66</td>
<td>0.53</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>0.21</td>
<td>0.66</td>
<td>0.54</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>0.53</td>
<td>0.66</td>
<td>0.54</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>0.23</td>
<td>0.49</td>
<td>0.24</td>
</tr>
</tbody>
</table>

Table 3: Comparison of maximum delays between the twisted-bundle and normal structures.

<table>
<thead>
<tr>
<th>Length,freq</th>
<th>Maximum delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Twisted Structure</td>
<td>Normal Structure</td>
</tr>
<tr>
<td>twisted</td>
<td>normal</td>
</tr>
<tr>
<td>1mm,1GHz</td>
<td>0.040</td>
</tr>
<tr>
<td>1mm,2GHz</td>
<td>0.033</td>
</tr>
<tr>
<td>2mm,1GHz</td>
<td>0.069</td>
</tr>
<tr>
<td>2mm,2GHz</td>
<td>0.061</td>
</tr>
<tr>
<td>4mm,1GHz</td>
<td>0.140</td>
</tr>
<tr>
<td>4mm,2GHz</td>
<td>0.129</td>
</tr>
</tbody>
</table>