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ICCAD-2000

A Conference for the EE CAD Professional

IEEE/ACM DIGEST OF TECHNICAL PAPERS

NOVEMBER 5-9, 2000

DOUBLETREE HOTEL

SAN JOSE, CA

Sponsored by:

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FOREWORD

On behalf of the ICCAD-2000 Executive and Technical Program Committees, I would like to welcome you to the International Conference on Computer-Aided Design, which will take place between November 5-9 at the San Jose DoubleTree Hotel.

The technical program for ICCAD-2000 was assembled by a program committee which includes experts from industry and academia around the world. The committee was organized and directed by Rolf Ernst. Its members devoted several days to reviewing the papers, and then participated in the full-day meeting to select papers from the many excellent submissions. Each paper was reviewed by at least 5 experts in the field. 86 papers were accepted from 265 papers submitted.

A new part of the technical program this year is the IEEE/CAS William J. McCalla ICCAD Best Paper Award. This award is given in memory of William McCalla, for his contributions to ICCAD and his CAD technical work throughout his career. The award will be given to the authors of a best paper selected through a rigorous and multi-stage review process. It will be given during the opening session on Monday morning, November 6.

Also new this year is the keynote address, which will be given by William J. Dally and is entitled "Lets Get Physical: ASIC/SOC Design in the Era of Wire-Limited Technology".

This year we have increased the number of 90-minute tutorials to seven, as they have been a highly appreciated part of the technical program. The tutorials will cover the topics of communications systems, challenges in physical design, incremental CAD, verification, testing future systems-on-a-chip, low-power processors, and manufacturability.

On Tuesday afternoon, there will be a technical panel organized by Lawrence Pileggi. The panel will be led by Richard Newton, entitled "Why Doesn't EDA Get Enough Respect", and the members will discuss the status of the CAD domain within the larger technology and business worlds.

Complementing the technical program is the 2000 tutorial program, on November 9th, organized by Andreas Kuehlmann. This year's tutorials include the following topics: 1) Algorithms for physical design, 2) Interconnect design and analysis for electrical integrity, 3) Principles and advanced techniques for symbolic model checking, and 4) Gain-based logic synthesis. The first three tutorials address the corner areas of a modern integrated synthesis flow covering logic synthesis, layout design, and signal integrity analysis. The fourth tutorial presents recent advances in verification algorithms based on model checking.

The rapid pace of advance at both ends — deep submicron and mixed signal technology at the physical end as well as systems-on-a-chip and platform-based design at the systems end — continues to make CAD research and tool development an exciting domain. ICCAD-2000 offers a place for CAD researchers, CAD developers, and VLSI designers to meet and exchange ideas about the problems and solutions for next-generation electronic systems.

Ellen M. Sentovich
Conference/Finance Chair

Rolf Ernst
Technical Program Chair

Table of Contents

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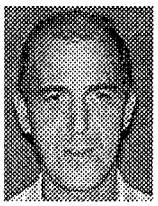

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IEEE/CAS William J. McCalla ICCAD Best Paper Award

The "Best Paper Award", selected by the ICCAD Program Committee, was selected through a rigorous and multi-stage review process. The Award is given in memory of William J. McCalla, for his contributions to ICCAD and his CAD technical work throughout his career.

"EXPLORING PERFORMANCE TRADEOFFS FOR CLUSTERED VLIW ASIPs"

Paper: 10B.2
Authors: Margarida Jacome, Gustavo de Veciana, Victor Lapinskii
Affiliation: Univ. of Texas, Austin, TX

ICCAD-2000 Keynote

William J. Dally
Professor, Stanford Univ.
Chief Technical Officer, Chip2Chip, Inc

Lets Get Physical: ASIC/SOC Design in the Era of Wire-Limited Technology

Description: As semiconductor technology scales, wires, not devices, dominate the delay, power, and area of integrated circuits. To realize the potential of wire-limited technology requires design flows and supporting tools that explicitly manage key wires early in the design process. Such a wires-first flow gives the designer early visibility of power and delay issues and the control over wiring needed to resolve these issues. Such an approach offers increased performance and reduced design time compared to wires-last ASIC flows. This talk will present a system designer's perspective on the challenges of emerging semiconductor technology and how design flows and tools should adapt to meet these challenges.

Biography: William Dally received the B.S. degree in Electrical Engineering from Virginia Polytechnic Institute, the M.S. degree in Electrical Engineering from Stanford University, and the Ph.D. degree in Computer Science from Caltech.

Bill is currently a Professor of Electrical Engineering and Computer Science at Stanford University where his group has developed the Imagine processor, which introduced the concepts of stream processing and partitioned register organizations, and low-power high-speed signaling technology. Bill has worked with Cray Research and Intel to incorporate many of these innovations in commercial parallel computers, with Avici Systems to incorporate this technology into Internet routers, and with Chip2Chip, Inc. to commercialize high-speed signaling technology. He has received numerous honors including the ACM Maurice Wilkes award. He currently leads projects on high-speed signaling, computer architecture, and network architecture. He has published over 110 papers in these areas and is an author of the textbook, Digital Systems Engineering.

TUTORIAL 1

MODERN PHYSICAL DESIGN: ALGORITHM TECHNOLOGY AND METHODOLOGY

Speakers:

Andrew B. Kahng - Univ. of California, Los Angeles, CA

Majid Sarrafzadeh - Univ. of California, Los Angeles, CA

Stan Chow - AmmoCore Technology, Inc., San Jose, CA

Background: This tutorial covers "the latest word" in physical chip implementation methodology and PD algorithm technology, going into more "detail" than the previous edition of the tutorial. The target audience consists of system and circuit designers who would benefit from understanding tool capabilities in this arena, CAD engineers (both R&D and support), design project managers, and academic researchers. Familiarity with basic PD methodology is assumed.

Description: The first section reviews PD implications of the process technology and system design roadmaps. A generic chip planning and implementation methodology will help set context. A review of fundamental PD problem formulations and algorithms will concentrate on latest developments in RTL and gate-level partitioning, block and coarse placement, top-level interconnect planning and optimization, and cell-based place-and-route. We motivate needs for incremental optimization techniques, handling incomplete design data, and new tool interactions and concurrent optimizations.

The second section focuses on "upstream interactions", between traditional PD and floorplanning and logic synthesis. Approaches to achieving a convergent, predictable implementation flow will be reviewed. These center on alternate methodologies for prediction/predictability and estimation, e.g., budgeting-based planning, small blocks + wireplanning, layout-driven logic synthesis, constant-delay methodology, etc. Attention will be given to performance and signal integrity optimizations.

The third section focuses on interactions with parasitic estimation, delay calculation, timing/power/SI validations, and static timing/noise analyses and characterizations. We discuss requirements for tight analysis loops, reconciliation of data models, and speed/accuracy of delay and noise estimates.

The fourth section describes new links between traditional PD and polygon-level optimizations (layout enhancements for manufacturability, layout-on-the-fly or liquid layout, etc.). Such linkages are becoming dominant in high-end ASIC methodologies due to manufacturing yield and die cost considerations.

Last, we compare the half-dozen leading variants in convergent RTL-down methodology, and how they respectively make demands on PD. This taxonomy includes recent methodologies that exploit distributed or parallel computational platforms, or that creatively invoke commodity SP&R to achieve greater design productivity.

TUTORIAL 2

INTERCONNECT-CENTRIC DESIGN AND ANALYSIS FOR ELECTRICAL INTEGRITY IN SYSTEMS-ON-A-CHIP

Speakers:

Dennis Sylvester - Synopsys, Inc., Mountain View, CA
Kenneth Shepard - Columbia Univ., New York, NY
Sudhakar Muddu - Silicon Graphics Inc., Mountain View, CA

Background: With rising clock rates and scaling technology, it is becoming increasingly necessary to design and model a very complex on chip electrical environment dominated by wires. In this tutorial, we describe the latest design and analysis approaches to ensuring the electrical integrity of today's systems-on-a-chip, tackling emerging problems such as inductance, substrate coupling, and power-supply integrity. This tutorial is designed for a target audience consisting of VLSI designers, managers, CAD tool developers, R&D engineers, and academic researchers. The goal is to enable attendees to address key interconnect-centric issues including all aspects of signal integrity, inductive effects, and high-performance clock and power distribution.

Description: We begin by describing the design and analysis techniques for signal integrity in deep submicron designs. We introduce the overall design flow and fundamental theories and concepts of RC/RLC interconnect analysis. We discuss the effects of capacitive and inductive coupling on line delay and noise. Design techniques to minimize capacitance and inductance effects are explored. In terms of analysis, we describe interconnect macromodeling in a static noise analysis framework. We also focus on inductance estimation, extraction, and analysis.

The impact of environmental factors including variations in power supply voltage, temperature, and physical factors due to process variations also affect the cycle time and design robustness. Large die sizes and higher operating frequencies, coupled with large on-die variations at reduced device geometries, call for special consideration of this type of "noise".

We then consider power supply integrity analysis for systems-on-a-chip, including IR and Ldi/dt analysis with full consideration of decoupling capacitance, switching activity, and package models. Power distribution methodologies will be discussed. Substrate coupling is also becoming an important new design and analysis concern for mixed-signal designs. Substrate effects will be considered in the context of substrate noise analysis, latch-up and ESD analysis, RF device modeling, and high-frequency interconnect analysis (current returns through the substrate). In additional to analysis, we will also consider design techniques for limiting all of these coupling interactions.

We will survey various clock distribution approaches and the applicability for large SoC designs. We will compare approaches such as H-tree, mesh, grid for a typical design in terms of requirements including local/global skew, jitter, slew rates, power, buffer area, clock wiring resources, and shielding area. We will review the latest approaches for clock distribution networks including usage of de-skew units to reduce the clock skew.

Throughout the tutorial we will consider measurement techniques and structures for calibrating and characterizing the on-chip electrical environment with an emphasis on interconnect and substrate effects. This is important for technology characterization, yield analysis, and modeling validation.

TUTORIAL 3

SYMBOLIC MODEL CHECKING: PRINCIPLES AND ADVANCED TECHNIQUES

Speakers:

Kenneth L. McMillan - Cadence Berkeley, Labs., Berkeley, CA
Kavita Ravi - Cadence Design Systems, Inc., New Providence, NJ
Fabio Somenzi - Univ. of Colorado, Boulder, CO

Background: By way of introduction, we will first briefly review the low power/low voltage problems and provide an outline of the rest of the tutorial, which will be in three parts.

Description: The first part is focused on design techniques. Several emerging technologies such as Multiple and Variable threshold CMOS enable low voltage/low power high performance computing while providing a "knob" to dynamically adjust leakage currents. The challenges in design methodologies and tools for these technologies will be discussed. In many applications, there is significant energy advantage in using an embedded power supply scheme where the voltage can be adapted based on computational demand. Rather than designing a system with a static supply to meet a specific timing constraint under worst case conditions, it is more energy efficient to allow the voltage to vary such that the timing constraints are just met at any given operating condition. The key challenges will be discussed including regulator design, circuit styles and scheduling. Trends in low-voltage library design will also be discussed and will cover logic, memory and low-swing interconnect drivers.

In the second part, we will deal with issues of power estimation and modeling. Estimation and modeling are central to any low power design methodology. After an introduction to fundamentals of power estimation, we will discuss power modeling at the gate/cell level. These models allow power analysis to be done at higher than the transistor level. Modeling and estimation at even higher levels (e.g., RTL) are key to doing early design exploration. These will be discussed next, covering both bottom-up and top-down techniques.

Finally, we will cover power/ground bus analysis and design, power optimization, and leakage power estimation and optimization. An overview of the performance, signal integrity, and electromigration reliability issues related to power distribution problems will be given. Common design styles for power distribution, and a unified methodology to design, analyze, and verify large power/ground grids will be presented with case studies. Modeling of package inductance, decoupling capacitors, and circuit parasitics to study their effect on power grid design will be discussed. Techniques to reduce power grid simulation effort, such as vector compression and static determination of worst case power demand scenario will also be considered. Combinational/sequential logic restructuring, encoding and several special design techniques for power reduction will be reviewed. Some recent transistor level and gate level optimization techniques to reduce leakage power in dual-Vt circuits will also be presented.

TUTORIAL 4

GAIN-BASED LOGIC SYNTHESIS

Speakers:

Prabhakar Kudva - IBM T.J. Watson Research Ctr., Yorktown Heights, NY
David Kung - IBM T.J. Watson Research Ctr., Yorktown Heights, NY
Ruchir Puri - IBM T.J. Watson Research Ctr.,Yorktown Heights, NY
Leon Stok - IBM T.J. Watson Research Ctr., Yorktown Heights, NY

Background: There exists a large gap between full-custom design and standard ASIC design. Gigaherz micro-processors have been announced while most ASIC parts run at maximum speeds of around 200 Mhz. However, a significant part of this gap can be closed by using the appropriate libraries and synthesis techniques. The same techniques that allow us to synthesize all control logic for gigahertz micro-processors, also helps the time consuming design closure of large complex ASICs. This is especially the case, when decisions early in the process are mistargeted due to the use of misleading wireload models. Delay models parameterized by gain allow predictable pre-placement synthesis without wire-load models and a more rapid evaluation of the effect of changes on the timing, thereby speeding up the combined synthesis and placement process.

Description: Delay models parameterized by gain significantly enhance the design and timing closure problems we are seeing in today's complex standard cell design methodologies. To use these techniques most effectively the libraries, algorithms and methodology need to be adapted. We will address all three of these and tie them together in a coherent methodology that enhances the predictability of the timing closure process.

We will revisit the circuit basics of standard cells and the creation of static delay models with emphasis on the construction of gain-based delay models. Guidelines for designing practical libraries and their implications will be discussed as well as efficient algorithms for timing analysis, and area and load calculation.

Gain-based delay models open the opportunities to the construction of a different class of synthesis algorithms. Technology mapping in particular can benefit from the load-independence property of these models. Recent algorithms from the literature will be discussed. Buffering and fanout tree construction are other examples of algorithms that can be made much more predictable. Wire and gate sizing will be revisited and shown how they can be done in this environment.

Gain-based synthesis opens the opportunity to synthesize predictably without wire-load models. The actual sizing can be postponed until deep in the physical design phases, resulting in a more reliable timing information and better identification of timing critical regions. A methodology will be described that ties these together.

This tutorial is intended for designers to get an insight in circuits and libraries for which very efficient algorithms exist to synthesize them, for CAD-tool developers to understand state-of-the art algorithms for rapid design closure on large designs and for their managers to get an insight in the applicability of gain-based synthesis techniques to their specific design problems.

Author Index

NOVEMBER 4-8, 2001

I•C•C•A•D•2001

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CALL FOR PAPERS

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AREAS OF INTEREST

ORIGINAL TECHNICAL PAPERS ON (BUT NOT LIMITED TO) THE FOLLOWING TOPICS ARE INVITED:

1) PHYSICAL DESIGN AND TEST

1.1 Placement and floorplanning techniques. RTL area estimation. Partitioning for layout. Module generation and layout synthesis.

1.2 Timing-driven and noise avoidance routing. Automatic special net routing. Layout for manufacturability.

1.3 Complete layout systems. Layout migration. Symbolic design & compaction. Physical design planning. DRC, ERC, and layout verification.

1.4 Analog, RF, and mixed signal circuit synthesis, optimization and layout. Analog, RF and mixed signal simulation techniques. Mixed technology design simulation (thermal, packaging, micromechanical).

1.5 Fault modeling, delay test, analog and mixed signal test. Fault simulation. ATPG. Reliability. Yield and manufacturability analysis.

1.6 BIST and DFT. Partial and boundary scan. Memory and core test. System Test. On-line testing.

2)SYNTHESIS AND SYSTEM DESIGN

2.1 Combinational logic optimization for area, timing, power. FPGA optimization. Interaction between layout and combinational logic synthesis. Technology mapping.

2.2 Sequential synthesis and optimization for area, timing, power. Interaction between layout and sequential synthesis. Asynchronous circuit design.

2.3 High-Level Synthesis (scheduling, allocation, binding). Datapath and control synthesis. Synthesis with IP libraries and reuse. Estimation and analysis in high-level synthesis. Memory system synthesis and optimization. HW interface synthesis.

2.4 HW/SW co-synthesis. System synthesis. Hardware platform synthesis and optimization (e.g. SOC). ASIP synthesis. Core based design. Embedded software synthesis (code generation). HW and SW estimation and analysis in embedded system design (area, timing, power). HW/SW interface synthesis.

2.5 Specification, modeling and validation of embedded systems. Languages. Multi-language design. Real-time software and RTOS. System level reuse techniques (e. g. object oriented design, design migration). Embedded systems engineering (e.g. workflow management, systems integration, design methodologies, design metrics, middle ware). Rapid system prototyping.

AREAS OF INTEREST CONT.

3)VERIFICATION, MODELING AND SIMULATION

3.1 Interconnect parameter extraction and circuit model generation. Interconnect level analysis.

3.2 Gate, switch and circuit level timing and power analysis.

3.3 Formal Verification techniques. Switch, logic and high-level simulation. HW/SW co-simulation. High-level design validation.

Proposals for Panel Sessions and Tutorials are also invited.

AUTHOR INFORMATION AND FORMAT

AGAIN THIS YEAR: ICCAD submissions must be made electronically, in PDF format through the ICCAD website. Reference the ICCAD WEB page for instructions on electronic submissions: http://www.iccad.com.

Please submit the following in PDF format:

- 1 page abstract should state clearly and precisely what is new and point out the significant results. The IMPACT, or potential impact, of the contribution will play a major role in the evaluation.
- **1 paper of no more than 8 pages using proceedings format**, double columned, 9pt or 10pt fonts including figures, tables and references. (In the proceedings, four pages are free of charge and each page beyond four pages is charged $100.00 per page).
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  - Previously published papers will not be considered: this includes papers appearing in published workshop proceedings. Papers presented only orally, or only available through informal distribution, will be considered.
  - Authors should clearly address the significance of their contribution as part of the paper.

AUTHOR'S SCHEDULE

Deadline for submissions:	**April 2, 2001**
Notification of acceptance:	**June 29, 2001**
Deadline for final version:	**August 10, 2001**

Papers will not be accepted for submission after 5:00 PM Mountain Standard Time, April 2, 2001 . This deadline is firm and inflexible. No exceptions will be made.

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Session Index