A LOW-POWER CORRELATOR

Bibhudatta Sahoo, Martin Kuhlmann and Keshab K. Parhi

Department of Electrical and Computer Engineering
University of Minnesota, Minneapolis, MN 55455 USA
email: {sahoo, kuhlmann, parhi}@ece.umn.edu

ABSTRACT

The complex valued matched filter correlators consume maximum power in the DS/SS CDMA receivers. These correlators accumulate 1024 samples lying in the range -7 to +7. This accumulation needs 3 data bits, 1 sign bit and 10 extra bits for overflow. Hence, the correlator can be implemented as a cascade of 4-bit full adder and a 10-bit incrementer. As a ripple carry adder (RCA) consumes the least power among all the existing adder architectures, we have implemented the 4-bit adder as a RCA. Previous incrementers were implemented as ripple counters. In this paper we propose a novel incrementer which is faster than a ripple counter based incrementer. Hence, it can be operated at a reduced voltage resulting in considerable power reduction. The incrementer is implemented using multiplexers, AND gates and TSPC registers. The ripple-counter correlator and the proposed incrementer correlator were laid out in MAGIC using 0.5μ CMOS technology followed by power estimation using HSPICE. It is shown that the proposed architecture requires 50% less power than a ripple counter based design.

1.. INTRODUCTION

The viability of portable applications of all-digital spread-spectrum receivers hinges upon the development of low-power matched filter correlators. In DS/SS CDMA [1] [2] [3] receivers maximum power is consumed in the complex valued matched filter correlators while determining the phase of the received PN code [4] [5] [6]. A total of 7 correlators are required to operate at the highest frequency in these receivers, approximately twice the chip frequency with its output being decimated at the data frequency. Hence, they consume a large fraction of the overall receiver power.

Correlators in DS/SS receivers accumulate 1024 samples at $64MHz$ lying in the range -7 to +7. Hence, accumulation for 1024 samples requires 3 data bits, 1 sign bit and 10 extra bits for overflow, leading to a total dynamic range of 14 bits. The correlator can be implemented with a full adder and an incrementer in cascade. The full adder is implemented as RCA which is known to consume the least power among all the existing adder architectures [5]. Hence, the whole problem of designing a low-power correlator boils down to the design of a low-power incrementer. In [7] the incrementer was implemented as a ripple counter (see Fig. 2) and the overall correlator was proved to have less power consumption compared to the correlator discussed in [8].

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This paper discusses an implementation of a 10-bit incrementer (see Fig. 3) which is faster than the 10-bit ripple counter. Hence, it can be run at a reduced voltage resulting in a considerable reduction in the power consumption. The incrementer is implemented using multiplexers, AND gates and TSPC [9] [10] registers. For comparison purposes, the ripple counter and the incrementer are laid out in MAGIC using 0.5μ CMOS technology followed by power estimation using HSPICE.

This paper is organized as follows. Section 2 describes the principle behind the new proposed incrementer. Power consumed in the incrementer and in the ripple counter is presented in section 3. Section 4 presents the power consumption of the ripple counter based correlator and the proposed correlator architecture.

2.. CORRELATOR DESIGN

The design has the following features :

1. The design uses biased representation of the incoming data bits as discussed in [7]. This representation converts the 4-bit signed data to a 4-bit positive value. The biased representation leads to the implementation of the correlator as a 4-bit RCA and a 10-bit incrementer which is gated by the carry output of the 4-bit RCA. The actual output in two's complement representation can be obtained by complementing the MSB of the 14-bit biased sum.

The incoming 4-bit two's complement data to the correlator has a range from -7 to $+7$. We obtain the biased representation by adding 8 to the data so that the data now lies in the range from 1 to 15. This addition of 8 is done by complementing the MSB of the 4-bit incoming two's complement data as shown here with two examples.

If $x = (-6)_{10} = (1\ 0\ 1\ 0)_2$ then the biased value of x is $x + 8 = (2)_{10} = (\overline{1}\ 0\ 1\ 0)_2 = (0\ 0\ 1\ 0)_2$. Similarly, if $x = (2)_{10} = (0\ 0\ 1\ 0)_2$ then the biased value of x is $x + 8 = (10)_{10} = (\overline{0}\ 0\ 1\ 0)_2 = (1\ 0\ 1\ 0)_2$.

2. In order to increment an N-bit number by 1 we can complement the LSB and the other bits till we encounter the first 0 after which the rest of the bits are left unchanged. This principle can be used to design an incrementer.For example,

$$for \qquad x = 1\,0\,0\,1\,0\,1\,1\,1 \tag{1}$$

$$x + 1 = 1\,0\,0\,1\,\overline{0}\,\overline{1}\,\overline{1}\,\overline{1} = 1\,0\,0\,1\,1\,0\,0\,0. \tag{2}$$

3.. POWER CONSUMPTION OF THE INCREMENTER

The AND gates in the circuit are implemented as a cascade of a NAND gate and an inverter. The inputs to the NAND gates have been reordered to optimize the power consumption. The clock period of the correlator was set to the sum of the delay of the incrementer plus the full-adder delay. As RCA is supposed to have

the least power consumption, the 4-bit adder is implemented as a carry-ripple adder. The delay of a static CMOS 24 transistor full-adder is $0.5ns$ and that of a half-adder is $0.4ns$ at $3.3V$. Hence, the total delay for a 4-bit adder is $2ns$ approximately.

Proposed Incrementer: The transistors in the NAND gates are sized for an unit inverter delay. True Single Phase Clock (TSPC) (see Fig. 1) registers are used. The transistors in the multiplexers are sized to give equal rise and fall time. For the proposed incrementer,

$$Delay_{incrementer} = 3.0ns \quad P_{incrementer} = 700\mu W$$
$$T_{clk} = 6ns.$$

Ripple Counter : The ripple counter is implemented using TSPC registers. For the ripple counter,

$$Delay_{ripplecounter} = 10ns \quad P_{ripplecounter} = 200\mu W$$
$$T_{clk} = 13ns.$$

The input to the matched filter correlator, in a DS/SS CDMA receiver, is 4-bits and is clocked at $64MHz$. This implies that the correlation must be complete in $15.6ns(64MHz)$ minus the register setup time. The register setup time is $1ns$. Hence, the maximum speed at which the correlator can be clocked is $13ns$. Since the proposed incrementer is clocked at $6ns$, we can reduce its power consumption if we increase the clock period to $13ns$ and run it at a reduced supply voltage [8].The ripple counter does not have any scope of power reduction since it is already clocked at $13ns$. T_{clk} and the power dissipation can be given by the following equations:

$$T_{clk} = C_{charge}V_0/k(V_0 - V_t)^2 \quad (3)$$
$$P = \alpha C_{total}V_0^2 f. \quad (4)$$

We obtain a β of 0.6 which means a supply voltage of approximately 2Volts. The delay of the full-adder at this reduced voltage is $1.4ns$ and that of a half-adder is $0.9ns$. Hence, the total delay of the 4-bit adder is $5.1ns$. The register setup time has increased to $2.3ns$. In order to maintain our previous clock of $13ns$ we need to pipeline the 4-bit adder at 2-bit level. Hence, the total delay of the 4-bit adder reduces to $2.8ns$. The new figures for the proposed incrementer are given by,

$$Delay_{incrementer} = 7.0ns \quad P_{incrementer} = 155\mu W$$
$$T_{clk} = 13ns.$$

Thus, we obtain a reduction of 22.5% in the power consumption of the proposed incrementer as compared to the ripple counter, both clocked at $13ns$ but at two different supply voltages.

4.. POWER CONSUMPTION OF THE CORRELATOR CHIP

The total power of the correlator chip is the sum of the power consumed in the 4-bit adder and the incrementer/ripple counter. The power consumed in the incrementer/ripple counter has to be reduced to half as the probability of getting a carry out from the 4-bit adder is approximately 0.5. The power consumed in the 4-bit adder takes into account the power consumed in one half-adder, three full adders and the registers.

For the proposed incrementer based correlator the power consumption at supply voltage of $2V$ is given by:

$$P_{TSPC} = 17\mu W \quad P_{half-adder} = 25\mu W$$
$$P_{full-adder} = 29\mu W$$

$$P_{total} = 0.5 * P_{incrementer} + 13 * P_{TSPC} + P_{half-adder} + 3 * P_{full-adder} = 410\mu.W$$

For the ripple counter based correlator the power consumption at supply voltage of $3.3V$ is given by:

$$P_{TSPC} = 49\mu W \quad P_{half-adder} = 70\mu W$$
$$P_{full-adder} = 85\mu W$$

$$P_{total} = 0.5 * P_{ripple-counter} + 8 * P_{TSPC} + P_{half-adder} + 3 * P_{full-adder} = 817\mu.W$$

For both approaches, the delay and power consumption results were obtained by HSPICE simulation. The capacitance values were extracted from the layout and included in the simulation.

Hence, we obtain a power savings of approximately 49.8% in the entire correlator chip after using the proposed incrementer as compared to the ripple counter.

5.. CONCLUSION

The results presented above show that the proposed incrementer leads to a reduction of approximately 22.5% in power compared to the ripple counter. However, the net savings in the correlator is approximately 49.8%. The proposed incrementer can be clocked asynchronously since the circuit in cascade is combinational rather than sequential as in the ripple-counter. This will further increase the speed and consequently, reduce the power consumed due to reduction in supply voltage.

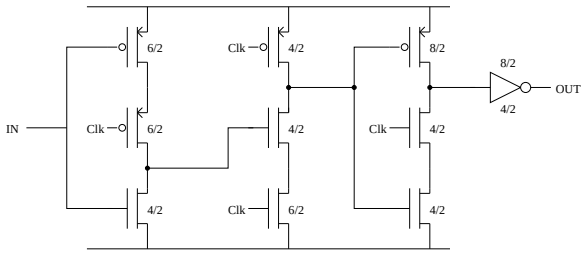

Figure 1. TSPC Register

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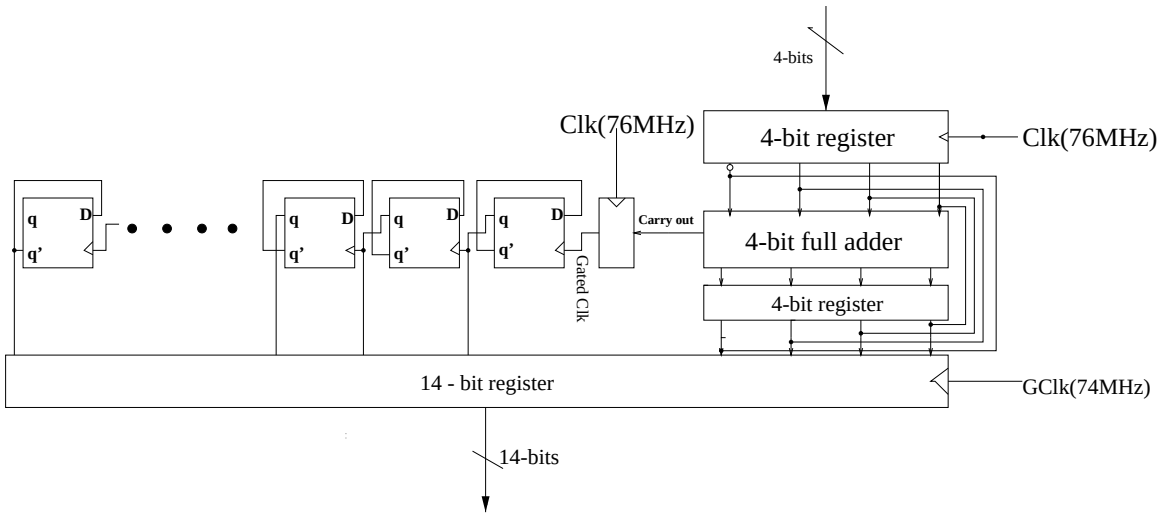

Figure 2. Ripple Counter Based Correlator

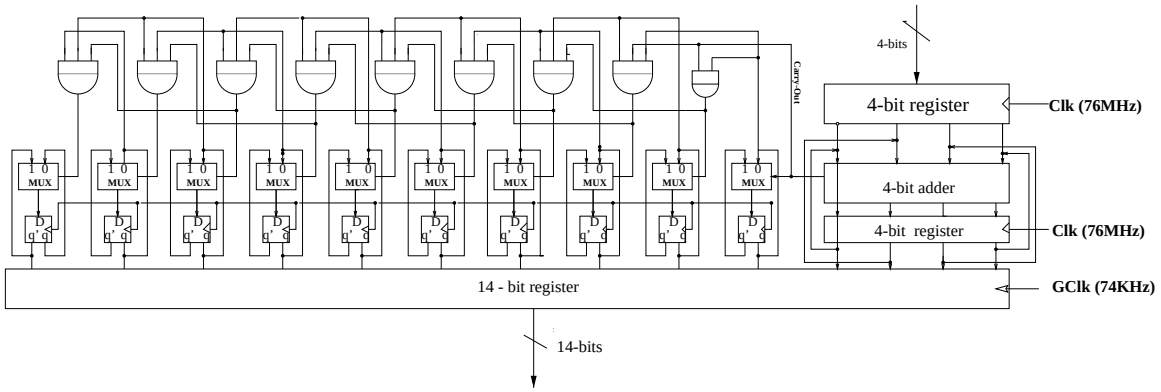

Figure 3. Proposed Correlator Architecture

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