Low Power High Speed Analog-to-Digital Converter for Wireless Communications

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Abstract

A new ADC architecture is devised. This architecture is memory based, in which the last sample is used to predict the current one, resulting in both power dissipation and energy reduction. The low power dissipation is a vital factor when we consider the chip reliability and integrity. The low energy consumption is a critical factor when we deal with battery operated devices like PCSs. This technique may also be used to extend the attainable flash converter resolution by pre-calculating the most significant bits.

1 Introduction

Digital signal processing (DSP) has been proven over the past decade to be a robust and cost effective way of signal processing. However, the nature of our real world is analog. Analog-to-digital converters (ADCs) are the bridge between this analog world and the DSP function block. As a result, data converters pose interesting and challenging tradeoffs relative to integration, process technology and performance parameters.

When a system requires a data converter, the first two specifications that define the performance are speed and resolution. With these two parameters, the data converter market can be defined concisely. While it is true that further specifications will be needed to determine compatibility to system requirements, speed and resolution are the most important. The speed of a data converter refers to the sampling rate or number of samples per second that can be converted. Resolution is the number of bits of accuracy – or the precision – to which the converter can replicate the analog/digital values. Although converter technology continues to improve, speed and resolution have historically had an inverse relationship to one another. Figure 1 shows a broad range of applications arrayed by their need for speed versus resolution. This segments the data converter specifications versus application.

Looking at the chart we can see that the high speed includes products from 6 to 14 bits. This region is dominated by communications and imaging applications. High speeds are necessary for sampling NTSC/PAL video or graphics outputs to produce high-quality video images. Communications systems require the high speed for sampling modulated signals at baseband or IF. The lower speed applications include converters from 8 to 24 bits. The demand for higher resolution is driven by the need for higher-speed modems and higher-quality digital audio systems. As new multimedia systems are developed – such as DVD – consumers are expecting higher-quality audio in their homes.

In between the limits of high speed and high resolution, there are moderate- and low-performance converters. This segment contains the widest variety of applications and customer base. Large markets exist in the fields of industrial process control, various automotive controls, mass-storage drives, low-end modems, scanners and so on. Some of the data converters in these segments have been

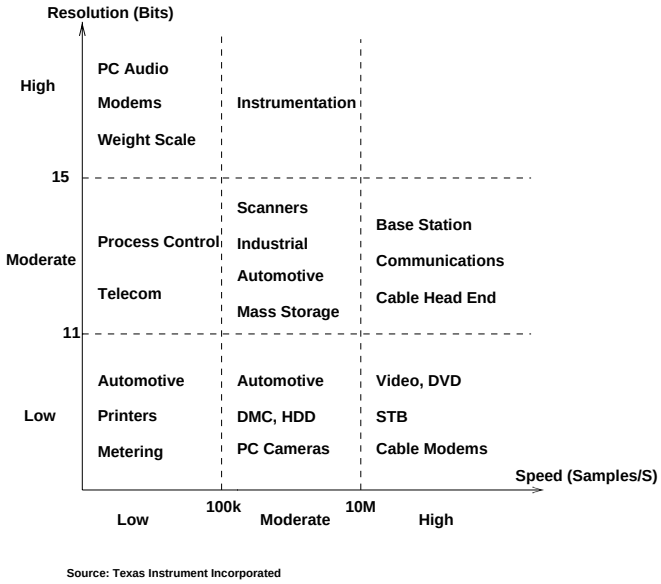

Figure 1: ADC applications vs. specification space

around for years and are still in strong demand. Integration of low-performance converters is now common in DSPs, micro-controllers and ASICs. But performance requirements are not the only factor in integration. Market demand and market maturity often determine whether the data converter is stand-alone or integrated into either an application specific standard product (ASSP) or system-on-a-chip. In section 2 an overview of the current ADCs architectures will be presented. In section 3 the proposed architecture is defined. Section 4 presents the simulation results.

2 Different A/D Converter Architectures

Several A/D architectures have been devised over the past years. Among these architectures the flash A/D [1] [2] [3] is considered the fastest available one. However, flash A/D is a large power consumer and isn't practical for resolutions higher than 8 bits. Pipelined A/D [1] [4] [5] is a wise choice when the latency isn't a critical parameter. It has the same throughput as the flash with considerable lower power dissipation and higher attainable resolution. Oversampling A/D [6] [7] is the best choice for low frequency signals like audio signals, for its power and hardware efficiency as well as its high dynamic range. However, for high frequency signal, oversampling A/D isn't the appropriate choice.

Since we deal with real signals we may not expect sharp variations in the signal amplitude most of the time. For such type of signals, if they have high frequency components, while The the signal value variation between any two consecutive samples are lim-

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ited to a small portion of the full scale. We may reduce the power dissipation by avoiding the recalculation of the most significant bits and using the history of the signal. The next section describes the proposed architecture.

3 Proposed Architecture

Figure 2 presents the proposed architecture, which uses the Most Significant Bits (MSBs) of the previous sample to predict the current sample MSBs.

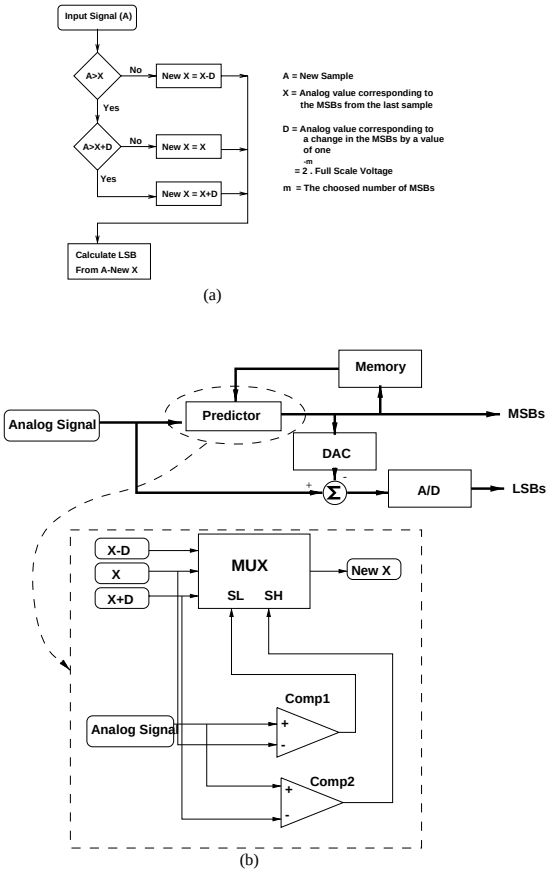


Figure 2: Proposed A/D Architecture (a) The Algorithm Flow Chart (b) The Proposed Architecture

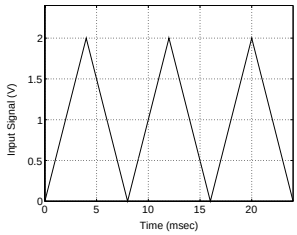
As explained in the algorithm flow chart we carry two comparisons one with ”X” and the other with ”X+D”. The results of these comparisons predict the current MSBs. Table 1 is the truth table for the MUX which has two controls SL and SH. SL is high when the input signal level is greater than ”X”, and SH is high when the input signal level is greater than ”X+D”. That means the maximum allowable change between two successive samples is ”D”, this may be used to determine the ratio between the predicted number of bits to the total resolution (M/N).

Table 1: Choosing Current MSB

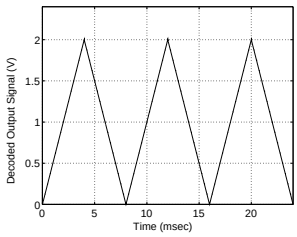
SH	SL	New X
0	0	X-D
0	1	X
1	1	X+D

4 Simulation Results

The validity of this algorithm is examined on the architectural level using MATLAB and SIMULINK. Figure 3 represent, the result of this simulation. The input signal, output signal after decoding, and the predictor stored value are shown in Figure 3 (a), (b), & (c) respectively.



(a)



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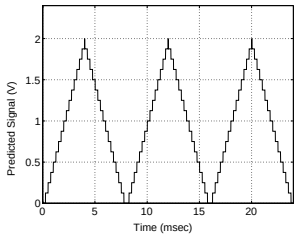


(c)

Figure 3: SIMULINK simulation results (a) Input signal; (b) Decoded output signal; and (c) Predicted signal.

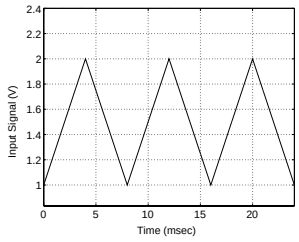
To check the stability of this algorithm we use input signal with a nonzero start while the simulation is carried with zero value in the predictor memory. The input signal, output signal after decoding, and the predictor stored value are shown in Figure 4 (a), (b), & (c) respectively. From this figure it is clear that the predictor value increase linearly until it captures the correct signal value, adaptive

Table 2: Hardware requirements for different A/D architectures

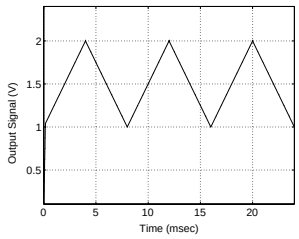
Architecture	Hardware Complexity
Flash	$2^N - 1$ [6]
Modified Flash	$2 + 2^{N-M}$
Pipelined	$\frac{N}{K}(2^K + a)$ [8]
Modified Pipelined	$2 + \frac{N-M}{K}(2^K + a)$

N is the number of bits of overall resolution
K is the number of bits per stage
M is the number of predicted MSBs
a is the ratio of stage hardware to per-comparator hardware.

methods may be used to decrease the time required for the predictor to capture the signal MSB.



(a)



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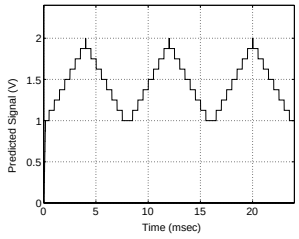

(c)

Figure 4: Algorithm stability results (a) Input signal; (b) Decoded output signal; and (c) Predicted signal.

The major concern when dealing with portable communication systems is power and energy dissipation. To find out the power saving using the proposed architecture in section 3 the hardware complexity of the proposed architecture is compared with the currently used architectures like flash and pipelined. Table 2 compares the hardware complexity in the flash and pipelined architectures with their modified versions. Taking into account the fact that the comparator is the most power consuming block in the design, the total number of comparators required in each design is taken to reflect the hardware complexity.

To compare the power efficiency for different architecture, the required number of comparators in each architecture has been calculated using table 2, this number is directly proportional to the power dissipation in the architecture. To find out the power efficiency we calculate the reciprocal of the hardware complexity number and normalize it. The higher value for this factor means less power dissipation and higher efficiency factor. The power efficiency factor for the different architectures in table 2 has been plotted in figures 5, 6 . The factor "a" in the pipelined architecture is taken equal to 0.5 [8].

From these results it is clear that, a better performance is obtained from the new architecture when the ratio (M/N) increases. This depends on the nature of the signal itself (i.e how fast its variation).

5 Conclusion

The efficient use of previous signal samples may reduce the power dissipation in the A/D converter. A new architecture is devised. This architecture is a memory based in which the current sample is predicted from the previous sample value. The high level simulations prove the functionality of the proposed architecture and the power dissipation reduction has been demonstrated.

References

[1] B. Razavi, *Data Conversion System Design*, IEEE Press Marketing, 1995.

[2] A. Dingwall, "Monolithic Expandable 6 Bit 20 MHz CMOS/SOS A/D Converter," *IEEE Journal of Solid State Circuits*, vol. 14, pp. 926–932, Dec. 1979.

[3] C. Mangelsdrof, "A 400 MHz Input Flash Converter with Error Correction," *IEEE Journal of Solid State Circuits*, vol. 26, pp. 184–191, Feb. 1990.

[4] E. Greeneich S. Park, "Fast Pipelined A/D Converter in CMOS Technology," *International Symposium on Circuits and Systems*, pp. 1–4, May 1998.

[5] T. Cho, "Low-Power Low-Voltage ADC Techniques using Pipelined Architectures," *Ph.D. Thesis, University of California, Berkeley*, 1995.

[6] Kevin M. Daugherty, *Analog-To-Digital Conversion, A Practical Approach*, McGraw-Hill, 1995.

[7] A. Eshraghi T. Fiez, "Delta-Sigma A/D Converters: The Next Generation," *Midwest Symposium on Circuits and Systems*, pp. 181–184, Aug. 1997.

[8] P. Gray, "High speed CMOS A/D converters," *Presentation Slides, University of California, Berkeley*, 1995.

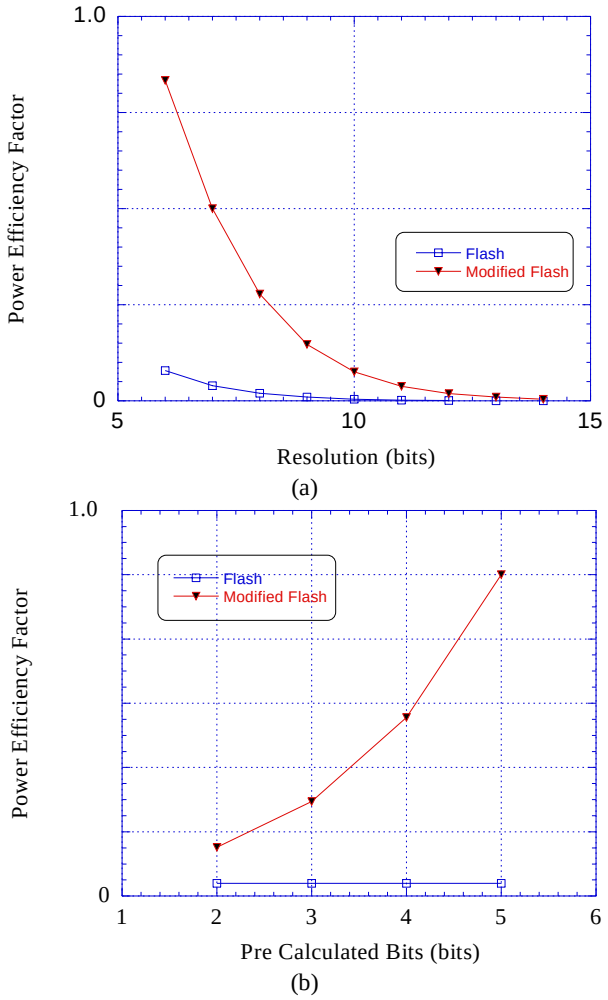

Figure 5: Power efficiency comparison between flash and modified flash architectures (a) Different resolutions(M=4) ; and (b) Different pre-calculated bits (N=8).

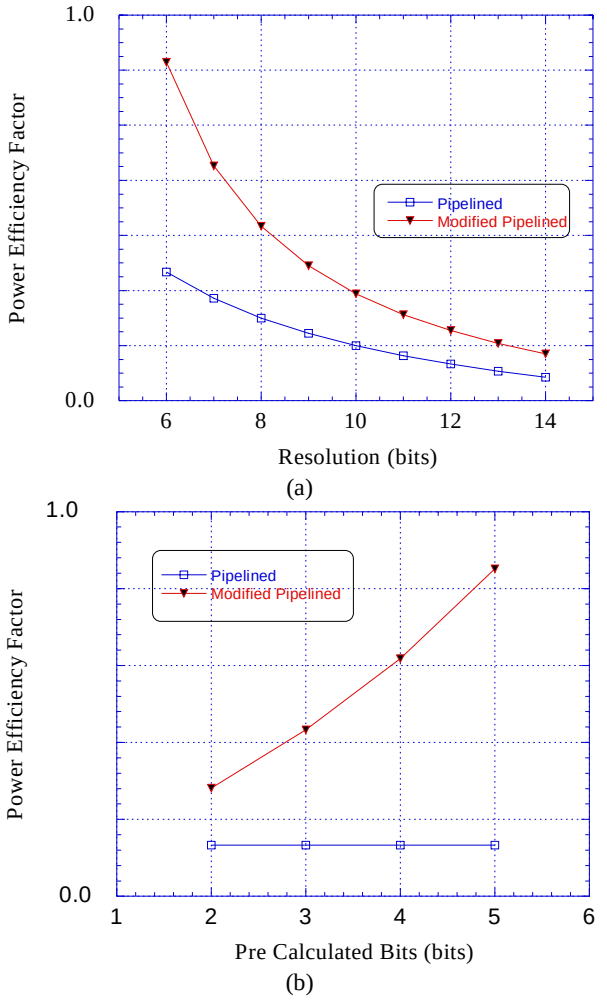

Figure 6: Power efficiency comparison between pipelined and modified pipelined architectures (a) Different resolutions(M=4) ; and (b) Different pre-calculated Bits (N=8).