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WELCOME

Welcome to the 2000 Great Lakes Symposium on VLSI (GLSVLSI). The symposium provides a forum for the presentation of advances in high-performance, low-power systems and components, design validation and testing, interconnects, and physical design. Aspects of designing low-power and high-performance products, including power-conscious design, design validation, routing and repeaters, placement algorithms, low-power circuits, behavioral and high level synthesis, power estimation and partitioning for low power, and simulation and estimation will be covered in detail in this year's GLSVLSI. As in previous years, this year's GLSVLSI contains a mix of invited talks and contributed papers.

Many thanks to all the authors who submitted papers. A total of 64 contributed papers were received. We were able to accept only 26 regular papers and 10 short papers. Short and regular papers authors are given 10 and 20 minutes presentation time, respectively.

The keynote speaker, featuring Dr. N. Sherwani from Intel Corporation, will address the impact of Internet on EDA research and development. The invited talks will feature Dr. V. De from Intel Corporation, and Dr. D. Blauuw from Motorola on the first and second day, respectively. Dr. De will address the technology and design challenges for low power and high performance microprocessors, while Dr. Blauuw will address on-chip inductance modeling and effects. A special luncheon talk on Moore's Law and MOSFETs at the End of the Roadmap will be given by Professor Mark Lundstrom of Purdue University.

Many thanks to the technical program committee for all the hard work in reviewing papers, paper selection, and session organization. Additional reviewers have also contributed to the review process, and we acknowledge their contribution. Thanks also to the invited speakers for graciously donating their time. Finally, we want to thank the ACM SIGDA for their support and cooperation, and Northwestern University, Monterey Design Systems, Motorola, Microsoft, and Intel Corporation for their sponsorship.

We hope you will find the symposium both stimulating and helpful. Please give us your comments and suggestions on any aspects of the conference.

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K. Roy, Program Chair (Purdue University)
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EDA is a mature business with over 30 years of history and stable market place. We have come along way from simple layout editors to complex formal verification engines of today. EDA industry (like all other industries) is now facing its greatest challenge yet! Internet is fundamentally redefining the EDA business. It impacts not only the target R&D areas but also sales, marketing and distribution of EDA software.

As hundreds of fabless companies learn to move in internet time, ASIC EDA tools and methodologies must also embrace the quick turn-around, first silicon goes to market approach. This requires integrated EDA solutions from architecture, RTL, layout, extraction and verification. The other impact is due to change in product focus areas. Wireless internet appliances requires small size, and low power. While size has been a traditional focus for the EDA industry, low power is a new challenge. Low power requires EDA tools for architecture power based tradeoffs, power estimation at different levels of design, and power optimization throughout the design process.

Dr. Naveed Sherwani received Ph.D in computer science from University of Nebraska at Lincoln in 1988. His research concentrated on graph theoretic algorithms for routing in printed circuit boards. He joined the Department of Computer Science at Western Michigan University. Dr. Sherwani's research concentrated on combinatorics, graph algorithms and algorithms for VLSI Physical Design Automation. In particular, Dr. Sherwani concentrated on efficient algorithms for over-the-cell routing to reduce channel routing area. In 1994, Dr. Sherwani joined Intel Corporation and currently leads the Strategic CAD Labs for Physical Design. His initial work in Intel concentrated on physical design tools and methodologies for layout of microprocessor chips with very high frequency goals. His current responsibilities include leading strategic EDA ventures and programs.

He has published over seventy five refereed papers in various journal and conferences on these topics. His paper on three layer over-the-cell routing received ‘distinguished paper’ award at ICCAD-91. He has chaired seven conferences and served on technical committees of several others. He is founder of Great Lakes Symposium on VLSI held regularly for the last eight years in the midwest. He is member of the technical committee for ICCAD'97, ICCAD'98 and ICCAD'99 and program chair for International Conference

SPECIAL ADDRESS

Moore's Law and MOSFETs at the End of the Roadmap

Forty years after its birth, identifying the limits of silicon microelectronics has become a critical issue. This talk will review the performance limits of silicon MOSFETs, the technological challenges that may limit future device scaling, and some new device approaches that are being explored. Issues that VLSI designers will have to deal with when designing chips with nanoscale transistors will also be identified.

Dr. Lundstrom received B.E.E. and M.S.E.E. degrees from the University of Minnesota in 1973 and 1974 and a Ph.D. from Purdue University in 1980. From 1974-1977 he was employed by Hewlett-Packard where he worked on the development of a second-generation NMOS integrated circuit process. He is currently Professor of Electrical and Computer Engineering at Purdue where he has also served as Assistant Dean and Director of the Optoelectronics Research Center. Dr. Lundstrom's research interests center on the physics of semiconductor devices, especially carrier transport and the limits of devices. He is an IEEE Fellow and the recipient of the ASEE Frederick Emmons Terman Award, and of two teaching awards from Purdue University.
PANEL DISCUSSION

VLSI Design Challenges in the Next Five Years

Chair: Majid Sarrafzadeh

Panel Members:

Eric Collins, Motorola
Khuram Mohammad, TI
Naveed Sherwani, Intel
Tak Young, Monterey Design Systems
Tom Ryan, Tellabs

In this panel, industrial experts speculate fundamental challenges of VLSI Design in the next five years. Major problems facing the industry will be formulated and possible solutions will be outlined. Panelists will provide their input on possible show-stoppers.
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