On-Line Testing and Diagnosis of Bus Lines with respect to Intermediate Voltage Values

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Abstract

This paper presents a self-checking, on-line testing and diagnosis scheme for bus lines affected by intermediate voltage values possibly due to bridging faults, or to different kinds of faults affecting the bus connected units.

1 The proposed scheme

Buses are very critical components of integrated systems. They may be protected with respect to faults resulting in logical errors using bus data encoding, and a bus connected checker. However this may not be the case for faults resulting in *intermediate voltage values* (IVVs), that is in voltage values different from those expected for the fault-free case, which may occur because of bridging faults involving the bus lines or different kinds of faults affecting the bus connected units.

The scheme that we propose for the on-line testing and diagnosis of IVVs is shown in Fig. 1, where TRC denotes a two-rail code checker, and CK is the system clock.

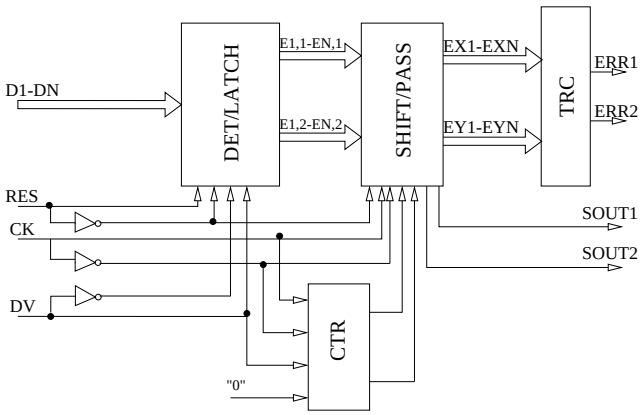

Figure 1. Internal organization of the proposed scheme.

DET/LATCH consists of N cells, each monitoring a bus line, and capable of revealing on-line the presence of an IVV affecting the monitored bus line in the time interval during which it should be stable in the fault-free case (e.g., when DV=1).

If the bus signals $(D_1, ..., D_N)$ are fault-free, $E_{i,1} = E'_{i,2}, \forall i$ (i = 1, ..., N), where E'_i is the complement of signal E_i. Therefore, a codeword of the two-rail code is produced at the output of DET/LATCH. Instead, in case of bus IVVs possibly compromising the system correct operation, $E_{i,1} = E_{i,2}$ for a number of is equal to the number of affected lines, so that a non-codeword is given to the output of DET/LATCH, which remains latched until RES = 1.

SHIFT/PASS receives the 2N signals $E_{i,1}$ and $E_{i,2}$, and gives to its output signals EX_i and EY_i (i = 1, ..., N), and (SOUT1, SOUT2). SHIFT/PASS can be in one of the following states: 1) the pass state; 2) the shift state. On-line testing is performed while in the pass state. Diagnosis is performed while in the shift state. Faults possibly affecting our scheme are revealed while in the pass or shift state. When in the pass state, SHIFT/PASS directly connects $E_{i,1}$ and $E_{i,2}$ to EX_i and EY_i, respectively. Therefore, in the fault-free case, TRC receives an input codeword, and produces an indication of correct operation on (ERR1, ERR2). Instead, in case of bus IVVs possibly compromising the system correct operation, a non-codeword is given to the TRC input and an error message is produced on (ERR1, ERR2). In case of internal faults affecting our scheme, an error indication is also provided on these outputs. When in the shift state, SHIFT/PASS provides two serial words on (SOUT1, SOUT2) which, in case of IVVs, allow to identify the faulty bus lines.

2 Verification and self-checking ability

As an example, we have implemented our scheme considering a standard 0.8μm CMOS technology, and we have performed conventional and Monte Carlo electrical simulations to verify the behavior of our scheme, considering statistical variations of electrical parameters up to the 15%.

As for the self-checking ability of our scheme, we have considered a set of faults ($\mathcal{F}$) composed of all possible stuck-ats, transistor stuck-ons, stuck-opens, resistive bridgings, crosstalks, delays and transients. We have verified that the functional part of our scheme is Strongly Fault Secure with respect to all faults $\in \mathcal{F}$, but few stuck-opens.