Panel:
Survival Strategies for Mixed-Signal Systems-On-Chip

Chair: Stephan Ohr, EE Times
Organizers: Rob A. Rutenbar, Georges Gielen

Abstract

More and more large ASICs require analog subsystems to interface to the real world—to wireless and wired networks, to sensors and transducers in embedded applications, to electrically complex high-speed interconnect. This is a major problem, since these analog subsystems break almost every assumption we know and love about digital systems. Analog circuits interact tightly with the technology, exploit rather than hide the physics of the fab, and manipulate precise electrical quantities rather than friendly binary abstractions. With respect to today’s logic-centric CAD flows, analog blocks fit poorly and abstract badly. The digital side of SoC designs is addressed via a mix of cell-based logical and physical synthesis, commercially available soft and hard IP, and company-specific reuse methodologies for migrating complex functional blocks. On the analog side, “reuse” usually means hoping you still employ the person who designed the legacy analog block you are desperately trying to update.

What is happening to help mixed-signal SoC designers in this difficult area? Analog synthesis tools that have been simmering in academia for the last decade are suddenly being commercialized. Mixed-signal IP companies have appeared, proffering a variety of commonly used core functions. Foundries themselves are augmenting their libraries to include portfolios of analog blocks. EDA methodology czars have started returning phone calls from annoyed analog designers. What can we hope for here? Analog synthesis? Mixed-signal IP? Practical reuse methodologies? Or will we continue to design analog the old-fashioned way— one transistor, one polygon at a time? Our panelists offer a mix of widely differing viewpoints on this important question.

Position Statements

Henry Chang
Cadence Design Systems, USA

We believe that it is absolutely true that more and more ASICs will require analog subsystems and that designing these chips will be difficult. We also believe that addressing these difficulties will require a combination of all the potential solutions listed above (and more), and we cannot continue in the old-fashioned way. The challenge will be to find the correct combination. The key to putting us on the right path will be to follow both a “Platform Based Design” approach and to engineer complete design methodologies around specific “field-of-uses.”

Georges Gielen
Katholieke Universiteit Leuven, Belgium

Analog synthesis is the avenue to follow to increase analog design productivity for time-to-market constrained complex mixed-signal ICs and SoCs. This includes both circuit synthesis where the optimal device sizes are determined, as well as automatic performance- and constraint-driven layout synthesis. Maturing research results and emerging commercial initiatives allow the automatic customized generation of frequently used analog cells from specification to layout in any target technology, and also alleviate the burden posed by the rapid pace of process migrations. In addition, the advent of standardized analog and mixed-signal behavioral modeling languages provides the technology to extend analog synthesis to more complex analog blocks and even entire front-ends, and to link it to a system design methodology.

Rudolf Koch
Infineon Technologies AG, Germany

For systems-on-a-chip IP-based design and re-use of blocks is at the core of most design strategies. For a (real) system-on-a-chip comprising also analog, mixed-signal and radio frequency blocks together with the digital cores, IP-based design does not really work today. Even the transfer of existing MS-blocks into a new technology requires roughly 50% of the effort of the first design for simulation, sizing, layout all done by hand, and even worse, a redesign of the transferred block may become necessary due to the impossibility to simulate or control all parasitic effects. Therefore the MS- and RF blocks slow down the design cycles and hinder the usage of the latest available technologies in SoCs.

The first challenge is to speed up the MS IP-reuse by increased design automation to catch up with digital. The next challenge is to design and verify the MS blocks including parasitic effects as crosstalk with improved or new tools. Finally the co-integration of software, digital hardware and MS blocks makes up systems with a virtually unlimited number of tradeoffs possible all along the signal processing chain. The last challenge is how to optimally partition such a system. Beside improvements in CAD tools and design flows, shrink-friendly technologies are essential for MS-SoCs.

Roy McGuffin
Antrim Design Systems, USA

Antrim licenses portable mixed-signal intellectual property (IP), design software, and expert design services for telecom, consumer and multimedia products. By fully supporting top-down design flows, higher levels of design representation, integration and automation of design processes, and reusability of existing IP are possible. Antrim’s customers have demonstrated significantly reduced design cycle times and improvements in overall design quality. With the introduction of mixed-signal synthesis, Antrim has automated many mixed-signal design processes, often reducing them from days to minutes. Mixed-signal synthesis also addresses
investment protection by automating process and foundry migration of mixed-signal IP.

K.C. Murphy  
*Pivotal Technologies Corp., USA*

The amount of functionality that can be packed onto a single silicon chip at deep-sub-micron (DSM) densities requires both new technical and new business approaches. The concept of system-on-a-chip (SOC) has been talked about for quite some time. But as the silicon foundries begin to use 0.25u technology as their mainstream technology, the SOC approach to design is now required.

The central concept that allows SOC designs to succeed is the separation of the “authoring” of functional blocks from their integration and manufacture. The SOC process is similar to the mature process upon which systems manufacturers have relied throughout the last four decades: functional blocks separately authored (by merchant semiconductor companies) and integrated onto printed circuit boards. The difference is that, with the incredible number of transistors that can be packed onto a chip, there is now only one manufacturing step instead of many.

There are four major blocks in a system-chip: memory, processors, custom digital logic and mixed/signal communications sub-systems. Embedded memory is typically supplied through the manufacturing process, digital logic is essentially supplied by EDA tools flows and companies like ARM, MIPS and others supply processors. Only one of these four blocks - the analog/mixed signal sub-system - has yet to be coherently addressed, and it is the essential enabler of integrated communications products.

Complete system-on-chip designs are the only path to successful products at the 0.25u and 0.18u feature sizes available today. Dataquest predicts that SOC designs will account for $16 billion in silicon by 2000, up from $2.2 billion in 1996.

Pivotal Technologies develops communications solutions that enable highly integrated silicon for data transmission. Using proprietary architectures and advanced methodologies, Pivotal combines key analog/mixed-signal/RF circuits with dedicated digital-signal-processing (DSP) to meet the significant market demands of broadband communications. Such markets include high-speed networking (10/100 and Gigabit Ethernet), digital subscriber line (DSL), cable Modems, Home Phone Networking (HPNA), Digital Video Interfaces (DVI) and wireless LAN (Bluetooth and 802.11).

Rob A. Rutenbar  
*Carnegie Mellon University, USA*

Very few companies can afford to design complex ICs one device and one rectangle at a time, and yet this remains today what dominates as “methodology” in essentially all analog design groups. Our digital colleagues combat the complexities of their designs with synthesis tools; we design by hand. The analog community no longer has the option to hand craft every design; there are just too many designs to do. Unfortunately, most historical analog synthesis approaches (and even some recent ones) have relied on simplifying assumptions intended to limit unpleasant secondary effects, reduce the degrees of freedom, and otherwise make difficult analog design problems easier.

We have a name for circuits that get simplified to make them easier: they’re called digital.

The lifespan of all of these shortcuts to analog synthesis has always been tragically short, as technologies, performance goals, and favored circuit topologies evolve. To be practical, analog synthesis tools need to (1) retarget quickly to *arbitrary* new designs and technologies, (2) support *full* capture, archiving and reuse of the constraints that practicing analog designers insist on, (3) support *both* circuit sizing and geometric layout, and (4) integrate *seamlessly* into the custom design flows in which circuit designers have historically been most comfortable.

At CMU, we have recently developed scalable synthesis techniques for analog circuit sizing that have successfully handled designs ranging from opamps to the frontends of commercial communication systems. Commercial versions of our earlier layout algorithms have demonstrated how automatic analog layout synthesis can be made practical and reliable for complex, commercial analog circuits.

For the coming generation of mixed-signal SoC designs, practical analog synthesis techniques will be essential.