Test Challenges for Deep Sub-Micron Technologies

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Abstract

The use of deep submicron process technologies presents several new challenges in the area of manufacturing test. While a significant body of work has been devoted to identifying and investigating design challenges in nanometer technologies, the impact on test strategies and methodologies is still not well understood. This paper highlights the challenges to current test methodologies arising from technology driven trends, and will present an overview of emerging techniques that address deep submicron test challenges.

1. Introduction

The faster and smaller technologies are challenging test in a number of areas. The fabrication cost of transistors continues to reduce while the cost of testing is not scaling. Geometries shrink year by year while the defect sizes do not shrink in proportion. Also, the increase of wiring levels and the increasing dominance of wire delay demand for new fault models. Furthermore, many of today's signal integrity problems, which are targets of deep-submicron (DSM) design validation, are becoming test problems as well. Examples are distributed delay variations, crosstalk - induced delay and logic errors, excessive voltage drop and/or swing on power nets, and substrate and thermal noise. The effects of these noise sources to the product quality remain unknown while it is becoming clear that process variations are now more likely to cause devices to marginally violate the performance specifications. Testing has to target not only spot defects but also such parametric performance failures. A new class of "noise" faults caused by above mentioned DSM parametric variations needs to be properly modeled to the levels of abstraction higher than the electrical-, circuit-, and transistor-levels for the applications in fault simulation, test generation, design for testability and built-in self-test.

DSM technology poses new challenges to Iddq testing as well. For deeper submicron technology, the background Iddq increases inexorably and the spread of Iddq distribution is also increasing. Iddq testing needs to be adapted to exist in an environment of decreasing signal to noise ratio, or be replaced with a better suited method that maintains its effectiveness in defect screening and reliability prediction.

In this paper, we discuss some of the key test issues in nanometer technologies and survey some emerging techniques that address the DSM test challenges. In Section 2, we give an overview of the test challenges and discuss critical areas for test, DFT tools, and methodologies, and the need for greater integration to the rest of the design processes. Section 3 focuses on the issues, challenges and emerging solutions to testing crosstalk-induced failures. In Section 4, we discuss the impact of power supply noise on reliability and delay testing. The section also gives a brief overview of modeling, test generation and path selection techniques that consider the effects of power supply noise on path delay. Section 5 highlights the challenges of Iddq testing under high intrinsic leakage and discusses leakage reduction techniques for the application of current testing.

2. DSM Test Challenges, Industrial Perspective

We will first examine the macroscopic use of these deep sub-micron transistors, i.e., the end product VLSI device itself that uses the additional and faster transistors predicted by Moore's Law. We will describe business trends and challenges for VLSI and their testing looking forward. Then we'll drill down into the software tooling and specific device design aspects of these challenges as they relate to DFT, ATPG, and test program generation and design integration processes.

The internet is driving an explosion of business to all aspects of our industry, transforming opportunities and presenting significant new challenges for the industry and for test. Only a small fraction of the internet of five years from now is installed. The size of the opportunities are driving tremendous competitive cost pressure on the producers while at the same time accelerating the increase of device core speeds and I/O and bus protocols to Giga-bit/sec plus ranges across platforms to meet the net's exploding data demands. The explosion of e-business is driving much greater quality expectations, i.e. increased test quality requirements. The trends towards increasing levels of integration and faster product cycles are significant challenges to test development and manufacturing

Even without these environmental factors, VLSI testing today is at a crossroads. First, the cost of component test is not scaling. Fig 2.1 shows the capital investments for fab equipment vs. test equipment projected from the SIA roadmap.

The top curve shows the fab capital per transistor cost reduction that's the basis for Moore's law. The bottom curve shows how the tremendous efforts and technologies of test have basically just kept up with device speed and complexity. These

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trends are consistent going back 20 years. Looking forward, we must have new DFT and test paradigms that change the direction of the bottom curve, so that it doesn't become more expensive to test a transistor than to fabricate it.

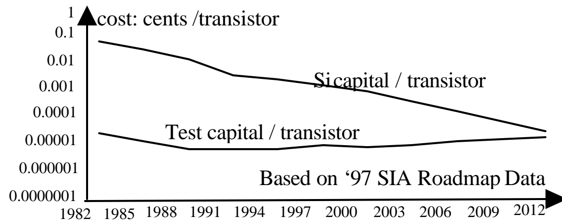

Fig 2.1: Moore's Law for Test: Fab. vs. Test Capital

Device power and power delivery in the end use platform as well as for the applied test face major challenges and redefinition of the critical metrics, where di/dt becomes as important as P_{avg} and P_{max}. A couple of years ago we looked at 500mA/nS as a di/dt test power delivery wall, but we now project devices capable of tens of amps per nS of di/dt (Fig. 2.2). Power delivery in the end use platform is moving to materials and schemes for lowering intrinsic R and L values, increased decoupling C, and local power regulation. For applied component test, the unique constraints of these environments often drive more stringent power requirements than the device "spec" or end use. These boundaries will drive new requirements, methods, and tools into VLSI design, i.e., design-for-power-delivery, design-for-di/dt, and global power management schemes on chip.

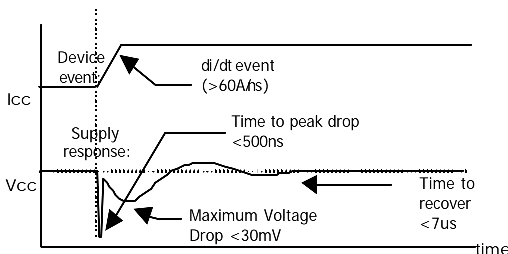

Fig 2.2: Test Power Delivery Challenge (Vcc at die)

We've used power supply scaling over the last few years to manage overall device power, as we broke the 5V barrier and have steadily reduced Vcc lower and lower. However, we will not continue that methodology much below 1.0V as noise and device margins really appear to be a hard boundary at that point and will accelerate the need and drive for overall design-for-power advances and usage. As design-for-power schemes involve chip globals and intrinsic properties from clock distribution to synthesis to standard cell design, it will require us to develop, modify, and integrate our logic DFT solutions to the device design and power solutions at several levels of abstraction. We also have to start to examine issues regarding differences in power distribution for DFT schemes (e.g. scan) verses power distribution for actual device end use.

Just as the external customer quality expectations are increasing, test quality at the transistor, gate, or circuit level faces increasing challenges. We've talked about the limits of the stuck-at fault model for many years, but failed to consistently deliver CAD solutions for fault simulation and ATPG that went much beyond stuck-at and some transition fault coverage, at least that are pragmatically applicable on today's VLSI designs.

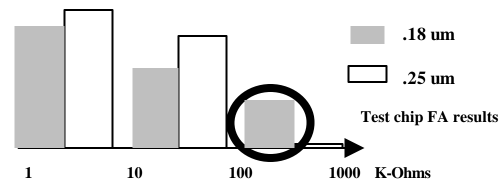

Fig 2.3: Bridge Defect Observed Resistance

Fig 2.3 shows a histogram of observed defect resistances obtained by failure analysis on a test chip fabricated on .25 micron technology vs. the version fabricated on .18 micron technology. On the .18 micron die, we see a marked increase in the quantity of defects that cause device failure in the next decade of resistance (100 K-Ohms) over the .25 micron device. Increasing defect populations and device sensitivities are causing more "soft" defects, i.e. defects that cause device failures increasingly sensitive to frequency, Vcc, and temperature.

Moving forward, our structural test and DFT solutions, i.e. scan schemes, fault simulations, and ATPG technologies must move to more realistic fault types in order to meet the increasing quality expectations, rapid product development cycles, and producer test development and manufacturing cost expectations of the internet age.

The transition from Aluminum to Copper interconnect on die will accelerate the need for fault simulation and ATPG for advanced fault types. The Copper damascene processes are radically different than the Aluminum subtractive lithographies that have been in use for the last 20 years, and will produce substantially new distributions of defect circuit behaviors, especially opens, which don't easily lend themselves to deterministic detection algorithms [1].

Solutions for simulating more complex fault behavior likely do involve more complex algorithms at the local level. However, the integration trend and shear number of transistors available to VLSI designs will require very significant gains in overall fault simulation and ATPG capacities. Breakthroughs are required in the size of the databases we can run on such tools, as well as the raw CPU efficiency and performance of those tools. This could require grounds up re-design of the DFT and ATPG CAD solutions towards a more complex hierarchy, yet one that provides better overall performance.

Increasing use of BIST, not only for arrays, but also for core logic and device I/Os is driven by not just the test capital cost problem. It is also driven by technical challenges of ATE to keep up with rapidly increasing device speed, edge placement accuracy, and stimulus-response data rates. Nanometer device performance coupled with the net's thirst for higher bandwidth will accelerate these test cost and technical challenges. In addition, BIST DFT best enables test content at tapeout, thereby better aligned to shorter product development cycles and reduced engineering resource investment for test content development.

Pseudo-random testing generally takes substantially more vectors (test time) than deterministic vectors to achieve equivalent coverage. However, a substantially longer test time could provide an optimal solution if coupled with significantly reduced tester hardware requirements, e.g., through BIST. Even if the DFT area is included, an optimized BIST solution on a simpler ATE could provide significant ROI. Logic BIST presents additional design integration and CAD challenges,

notably in the areas of automated contention checking as well as for power (under test) predictability.

Nanometer technology will have smaller, faster transistors, more sensitive to a wider variety of subtle process variations and defect types such as Copper voids, lattice dislocations, parasitic leakages, etc. These sensitivities will be further activated by the increasing variance in the types of circuits being used for digital VLSI moving forward. The reasons for this are varied: increased performance, performance per unit power, better performance on a given fab process, etc. Less and less of the digital nanometer VLSI will be basic CMOS and more and more will contain a wider variety of circuits (domino, pass gate logic, etc) and use of what was previously more exotic transistor and process techniques (multiple threshold, SOI technologies, etc).

Each of these techniques or technologies will present a different distribution of circuit and more complex fault types (e.g., SOI history effect, or leakage, timing sensitivities of new more dynamic circuit styles) that must be analyzed and built into the DFT and test solutions and CAD environment ahead of time. Scaling and integration for DFT/ATPG will become even more critical moving forward, both for the integration of DFT methodologies (circuits, cells, test clocks, etc) to the other design methodologies (design for power, standard cells, etc.) as well as for the integration of the DFT CAD tools (fault simulation, coverage analyses) to the rest of the design CAD suite (logic simulation, performance verification, timing analysis, etc.).

3. Testing Crosstalk-Induced Failures

With deep sub-micron technology and clock frequencies in the GHz range, signal integrity problems due to increasing cross-coupling capacitance and mutual inductance will have significant adverse effect on the proper functioning and performance of VLSI systems. Figure 3.1 illustrates a circuit model of the elements influencing the interaction of two adjacent interconnects (Y1, Y2) running in parallel. The model contains distributed values of capacitance (C1, C2), resistance (R1, R2) and inductance (L1, L2) of each line, cross-coupled capacitance (C_C), and mutual inductance (M_{12}). Also included are drivers with a characteristic "ON" resistance (R_{ON}) and capacitive loads (C_{L1}, C_{L2}) for each line.

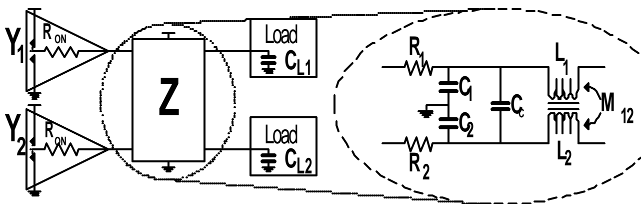

Figure 3.1 Circuit model for adjacent interconnects.

For sub-micron processes, driver resistance (R_{ON}), line resistance (R_1, R_2), line capacitance (C_1, C_2), and load capacitance (C_{L1}, C_{L2}) dominate circuit behavior. However, for deep sub-micron technologies, cross-coupled capacitance (C_C) starts dominating and becomes a considerable contributor to problems with signal integrity [2,3,4,5]. Moreover, line inductance (L_1, L_2) and mutual inductance (M_{12}) may also contribute to the noise mixture [6]. The increase of these parameters can be attributed to the decrease in spacing between conductors, the increase of height to width ratio of each conductor, the increase of length for which conductors may run adjacent to each other, and the increase in density due to the increase in metal layers.

The adverse effects of increased cross-coupling capacitance and inductance on signal integrity can be threefold. When cross-coupled capacitance becomes a first order parameter between two interconnects, two basic signal anomalies can take place as a result to step inputs. When one signal is switched (for example, Y_1 switched high) and the other is driven steady (Y_2 driven low) the energy transfer through C_C results in a voltage glitch on the steady signal (Y_2). This is shown in Figure 3.2(a).

The second anomaly, when the two interconnects are switched to opposite values (for example, Y_1 switched high and Y_2 switched low), the result can be a significant increase in transition time, as shown in Figure 3.2(b). On the other hand, when the two input transitions are in the same direction, both falling or both rising, the resultant transitions can experience significant speed-up.

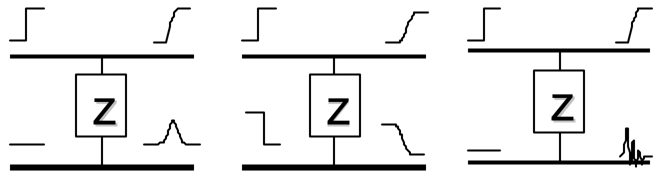

Figure 3.2 (a) Glitch , (b) Delay, and (c) Oscillations

When inductance is combined with other elements of the circuit model, the voltage relationship generally results in a high-order differential equations, producing damped voltage oscillations superimposed on top of a glitch or delay, resulting in overshoots and undershoots until the signal finally settles down, as illustrated in Figure 3.2(c).

Several design [3,7,8] and analysis techniques [9,10,11,12,13,14,15] have been developed to help design for margin and minimize signal integrity problems. However, the amount of over design may be prohibitive. Moreover, it is impossible to anticipate in advance, all the process variations and manufacturing defects that may significantly aggravate the cross-coupling effects. Hence, the need to test for manufacturing defects leading to signal integrity problems.

3.1. Analysis Techniques for Crosstalk Test

To be able to generate quality test vectors which can excite and detect crosstalk defects, it is essential to have available analysis models and tools which can predict the crosstalk effects, without having to perform detailed and time consuming SPICE simulation. At the same time, the analysis models/tools need to consider the dependence of the crosstalk effects on several factors like drive strength (R_{ON}), wire length, clock speed, skew, driver balance, load to load balance, and impedance matching. Most of the crosstalk analysis techniques [9,10,11,12,13,14,15] are not suitable for iterative use in crosstalk test generation for large VLSI circuits, and also do not consider the effects of non-linearity of the source and load networks. In [4], a methodology was developed to characterize cases where inputs to one or both the coupled interconnects have transitions with arbitrary transition times and directions. Expressions were obtained which can be used to characterize the amplitude, width, energy, and timing of a glitch pulse, as well as the speedup or slowdown of transitions, due to cross-coupling capacitance [4].

To enable generation of test vectors to detect errors caused by overshoots and undershoots from inductance induced oscillations, an analytical model has been developed in [16] which can estimate the magnitude of overshoots and undershoots, and the time taken by the signal to settle to a bound close to the final value. As opposed to earlier techniques to estimate inductance induced oscillations [17,18], which assume step inputs, the technique in [16] allows input transitions to have arbitrary fall and rise times.

In order for crosstalk to affect the performance, certain logic and timing conditions must be satisfied. Performance sensitivity analysis can be used to determine the set of crosstalk noise sources that need to be targeted for testing in a given design. To be able to consider the statistical nature of noise sources, a statistical timing analysis framework has been proposed to perform the sensitivity analysis [19]. In statistical timing analysis, the delays of cells/interconnects are modeled as correlated random variables with known probability density functions. Given these delays, the cell-level netlist and the clock period, statistical timing analysis can derive the probability density functions of the signal arrival times, required times and slacks at internal signals and POs. Crosstalk noise can cause perturbations of the delay random variables of the affected cells/interconnects. To derive the sensitivity of the performance to the given source of crosstalk noise, the statistical timing analysis can be run twice: first time without considering delay perturbations caused by crosstalk and the second time with the perturbed delays.

We next discuss the use of crosstalk analysis models to develop test generation techniques for crosstalk defects.

3.2. Gate-level Crosstalk Test Generation

In this section, we describe test generation techniques that can be applied to generate tests for local interconnects in gate-level circuits [21,22,24,25,16]. One of the first test generation techniques developed was [21], based on a logic fault model developed for crosstalk glitch [20]. For each candidate pair of wires, two faults were considered: a positive glitch on the victim wire activated by a signal value '0' on the victim and a rising transition on the affecting wire; and a negative glitch on the victim wire, activated by a signal value '1' on the victim and a falling transition on the affecting wire. The faults were characterized by the duration of the glitch. A test generation technique was developed, based on PODEM [23], to generate the required signal values at the candidate pair of wires from the circuit inputs, and propagate the fault effects to the circuit outputs. Since only glitch faults were considered, the case where both the victim and affecting wire had opposite transitions was avoided. Several enhancements to the basic approach resulted in a more efficient test generation technique for crosstalk glitch faults in [22].

A crosstalk test generation technique was developed in [24] that takes into account several attributes such as noise strengths and signal arrival times while generating test patterns to maximize the crosstalk glitch effect. Also, care is taken to monitor the glitch size at each step, and noise sensitive paths are selected for noise propagation, to ensure the worst case glitch effect is propagated to the circuits primary outputs. An enhanced test generation technique, which can also generate test vectors to detect delay (slowdown) and speed-up effects, has been proposed in [25]. Besides traditional logic values, the test generator also includes computation for signal timings (such as arrival time and rise/fall times). New timing conditions are also proposed so that a crosstalk effect, E, is first generated, and then other constraints employed so as to propagate the maximum effect of E, namely delay for slowdown or speedup, or amplitude and width for pulses, to an output or a flip-flop. Based on the analytical models for inductance induced noise effects described above, a test generation procedure has been developed in [16] to detect functional errors caused by overshoots and undershoots due to inductance induced oscillation.

3.3. Testing Crosstalk Defects in Long Interconnects

The test generation techniques described in Section 3.2 cannot be applied to system-level interconnects, like busses and inter-core interconnects, which dominate today's core-based system-on-chips (SoCs). Empirical data has shown that crosstalk effects are most significant in long interconnects [5,26]. Hence, there is a critical need for developing methods for testing crosstalk defects in SoC interconnects.

For a set of interconnects, the number of possible process variations and defects that need to be considered can be so extensive that testing for all such variations and defects explicitly is prohibitive. At the circuit level, a coarser mesh of lumped circuit elements (R, L, and C parameters) can describe the cumulative effect of process variations behaviorally, but the resulting fault space is still too large. To make testing for crosstalk defects feasible, a new Maximal Aggressor fault model has been developed [26], based on the four possible crosstalk error effects, positive glitch, negative glitch, rising delay, and falling delay, on the victim wire of the set of interconnects under test. All the other interconnects in the set are designated aggressors, and act collectively to generate the glitch or delay error on the victim. Based on the input conditions required to activate the error conditions, a set of Maximum Aggressor (MA) tests, consisting of four input transitions, are proposed for the four crosstalk faults on each victim. The attractiveness of the model is that it can abstract crosstalk defects in interconnects with a linear number of faults, while the corresponding MA tests provide complete coverage for all physical level defects related to cross-coupling capacitance between the interconnects.

A methodology has been developed to simulate physical-level crosstalk defects in interconnects, and measure the fault coverage of crosstalk tests [26]. Since the number of crosstalk defects may be extensive, techniques have been developed to select a small set of representative defects, based on some key crosstalk properties that have been established. Extensive simulation was performed to validate the crosstalk properties, the defect selection procedure, and the MA crosstalk fault model.

To facilitate at-speed testing, which is important for testing high-frequency systems most susceptible to signal integrity problems, a self-testing methodology has been developed for testing crosstalk defects in SoC interconnects [27]. Constraints and requirements for testing system-level interconnects have been established, determining which interconnects need to be tested. The self-test methodology is based on the MA fault model, and consists of on-chip test generators and error detectors embedded in necessary cores; while the test generators generate the MA test sequences for crosstalk faults, the error detectors, analyze the transmission of the test sequences in the interconnects, and detect any transmission errors. A test controller has been designed to initiate and manage test transactions by activating the test generators and error detectors, and having diagnosis capability should an error be reported.

While the use of on-chip self-test structures to test SoC interconnects using MA tests ensure 100% at-speed test of all crosstalk defects, the area and delay overheads can be excessive for some SoCs. Alternative crosstalk test strategies need to be explored, which involve the use of legacy tests, like boundary-scan, delay, and functional tests, in testing for crosstalk in interconnects. To enable the above, fault coverage estimation techniques need to be developed which can evaluate the effectiveness of test sets to detect crosstalk defects in interconnects. Also, alternative techniques need to be developed to generate the MA tests on the embedded SoC interconnects, minimizing the use of on-chip test structures.

4. Delay Testing Considering Voltage Drops

With the increasing complexity of deep-submicron designs, more devices are switching simultaneously, which results in increased power supply noise. One component of this noise, inductive noise (also called ground bounce noise), results from sudden current changes on either the package lead or wire/substrate inductance. The other component, net IR voltage drop, is caused by current flowing through the resistive power and ground lines. The noise can cause a voltage glitch on power supply lines, resulting in timing and/or logic errors. Large voltage drops through the power supply lines can cause electromigration, which in turn can cause short or open circuits. Techniques for modeling and estimating the chip-level power supply noise have been proposed in [35, 33, 30, 32, 28].

Power supply noise can affect both reliability and performance. It reduces the actual voltage level that reaches a device, which in turn can increase cell and interconnection propagation delays. SPICE simulations show that a 10 to 15 percent voltage drop during cell transition can cause a 20 to 30 percent increase in cell propagation delay. If the cell is a clock buffer or is in the timing-critical path, this delay deviation could cause serious clock-skew problems or a nontrivial increase in the critical path delay. The impact of the power supply noise on the performance of deep-submicron designs has been studied in [34]. A statistical modeling technique for power supply noise has been proposed and integrated with a statistical timing analysis framework to estimate the performance degradation.

To provide an accurate estimate of the design performance, the power supply noise effects on the delays need to be considered during timing analysis. However, traditional timing analysis techniques cannot consider these effects. This is because the noise effects are highly input pattern dependent. A possible solution is the use of the dynamic timing analysis technique [29]. It is based on generating and simulating patterns that sensitize the longest paths in the circuit and produce the worst-case noise effects on the signals/cells along these paths. Experiments show that the circuit delay predicted by the dynamic timing analysis method is significantly longer than the delay predicted using traditional timing analysis tools.

Power supply noise can cause logic and timing faults that need to be targeted during manufacturing testing. To activate these faults and propagate them to the primary outputs, test vectors must be carefully selected. A test generation technique for detecting logic errors caused by ground bounce in deep-submicron designs has been proposed in [31]. A cost function derived from the analytic equations for the proposed circuit model for ground bounce in internal logic and from circuit simulations is used to generate patterns that maximize ground bounce. The method can handle fanout-free circuits while for designs with re-convergent fan-outs the computational complexity might be very high.

The effects of power supply noise on the performance can be detected by applying delay tests. However, most of the existing delay techniques are based on simplified, logic-level models and cannot be directly used to model and test timing defects in high-speed designs that use deep submicron technologies. Therefore, new delay testing strategies are needed to close the gap between the logic-level delay fault models and physical defects. The tests must produce the worst case power supply noise along the sensitized paths and therefore, cause the worst case propagation delays on these paths. A delay test generation procedure that can take into account the power supply noise effects on the delay of the circuit has been proposed in [28]. This technique uses a Genetic Algorithm-based approach to generate patterns that maximize the power supply noise for the gates on the target path in addition to sensitizing the path. The test generator needs the netlist as well as the physical design of the circuit as input. The test generation consists of three phases. The first phase is a pre-processing phase and it is performed only once for each design. The second and third phases are repeated for each target path.

In the first phase, the power net RCs are extracted and a current/voltage waveform library is built for different cells [28]. In the second phase, for each selected path, a partially specified test is generated under most stringent sensitization condition under which a test exists without considering timing information. Sensitizing a given path usually requires assignment of only a small number of primary input values. The unspecified values can be assigned such that they activate the worst-case noise effects and produce the worst-case propagation delay on the path. Therefore, in the second phase, delay test is generated for each target path and an attempt is made to leave as many primary inputs unspecified as possible. In the third phase, the unspecified primary inputs are assigned values such that the power supply noise impact on the delays is maximized. A genetic algorithm-based (GA-based) approach is used for this purpose.

In addition to considering power supply noise during test generation, the noise effects need to be considered during path selection as well. It has been shown that the selection of critical paths has a significant impact on detection of timing failures [36]. This is because, usually, only a very small subset of all paths can be selected for delay testing. A common path selection strategy is to select the longest paths reported by timing analysis. However, performance optimized designs tend to have a large number of paths of similar lengths and selecting all longest paths might not be feasible. Selecting an arbitrary subset would not be a meaningful solution because small process variations, capacitive coupling, power supply noise and/ or delay modeling inaccuracy may cause the delays of many non-target paths to be longer than the selected target paths. Therefore, new methods based on accurate gate/interconnect delay information as well as consideration of noise factors such as crosstalk and power supply noise need to be developed for selecting the critical paths for delay testing in deepsubmicron designs.

5. Current Testing for DSM Technologies

5.1. Iddq testing under high intrinsic leakage

The ever-increasing levels of on-chip integration in the recent decade have enabled phenomenal increases in computer system performance. Unfortunately, an increase in performance has also been accompanied by an increase in a chip's stand-by

leakage current – mainly due to the scaling down of transistor threshold voltage (V_T) to maintain high performance. Borkar [39] estimates a factor of 7.5 times increase in leakage current and a five-fold increase in total static power dissipation in every chip generation. The high stand-by leakage threatens well-established quiescent current (I_{DDQ}) based testing techniques.

Off-state leakage (I_{OFF}) varies as a function of transistor device architecture, transistor type (*p* and *n*), dimensions (L_{gate}), and process variation. To combat high intrinsic leakage a differential current testing technique is proposed in [39] where a differential current measurement taken at a given vector (ΔI_{DDQ}) is defined as the I_{DDQ} measurement taken at this vector minus the I_{DDQ} measurement taken at the previous vector. It is shown that ΔI_{DDQ} follows, on a vector to vector basis, a normal distribution with a mean of 0. Since the differential rather than the absolute current measurements are used, the effect of high sub-threshold leakage can be eliminated. However, the ΔI_{DDQ}'s can be small and hence, can affect the fidelity of the technique.

The transistor intrinsic leakage mechanism is a function of bias point, temperature, L_{eff}, well-to-source backbiasing (V_{SUB}), and power supply (V_{DD}). These device properties, however, can be applied to a test application that combines I_{DDQ} and the IC's maximum operating frequency (F_{max}) to establish a multi-parameter test technique for distinguishing intrinsic and extrinsic (defect) leakages in IC's with high background stand-by current. Results show that I_{DDQ} along with F_{max} can be effectively used to screen defects in high performance, low V_T CMOS IC's while achieving higher yield [41].

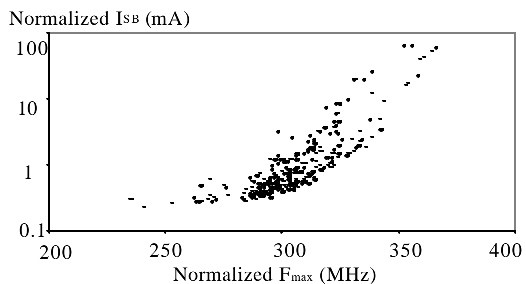

Fig. 5.1. I_{SB} versus F_{MAX} for 32-bit microprocessor.

Fig. 5.1 summarizes how a microprocessor F_{MAX} and I_{SB} (stand-by current) track each other. F_{MAX} and I_{SB} values shown in Fig. 5.1 were normalized by multiplying the numbers by a constant value. I_{SB} and F_{MAX} are fundamentally related as both increase with reducing transistor channel length. We found a clear correlation between I_{DDQ} (I_{SB}) and the maximum operating frequency (F_{MAX}) of a microprocessor as both are functions of L_{eff}. Note that data shown in Fig. 5.1 was obtained by intentionally varying the transistor channel length of our microprocessors. Our data suggests that as one targets for lower transistor channel length, the frequency of the IC along with its static leakage increases. The relationship established in Fig. 5.1 will be fundamental for an IC product manufactured in a given process technology. Thus, this dependency varies from technology to technology, product to product, and company to company and needs to be established for each product on a given process technology. Once we know how I_{SB} vs F_{MAX} varies as a function of fundamental parameters of the technology (L_{eff}, V_T, etc.), we are able to use it for IC testing. A defective IC will be one whose leakage versus frequency violates this behavior. An adjustable I_{SB} limit can be set based upon the parameters I_{SB} and F_{MAX} to establish a 2-parameter test limit that distinguishes fast and slow die from those that are defective. Adjustable limit means that I_{DDQ} (I_{SB}) limit is not set at a fixed constant value. The concept allows for improved signal to noise ratio for defect detection for high performance ICs with high background leakage levels.

Fig. 5.2 further illustrates the test application. To explain the concept, let us assume a linear dependency for simplicity. Intrinsic values of I_{SB} can be distinguished from extrinsic (defect driven) I_{SB} values and a limit set up to reject the defective ICs. The I_{SB} limit moves up as F_{MAX} increases. The defect dots shown in Fig. 5.2 show higher leakage than the proposed adjustable I_{SB} limit shown by the dashed line.

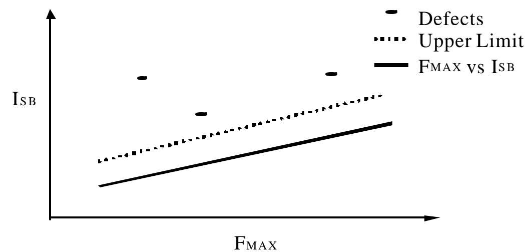

Fig. 5.2. I_{SB} versus F_{MAX} for the 32-bit microprocessor.

Table 5.1 is a decision matrix when I_{SB} and F_{MAX} values are available after regular manufacturing test. I_{SB} is measured to check the static power of the IC against the data sheet and for defect detection while F_{MAX} is measured for speed binning the microprocessors. Consequently, the proposed test is only a data manipulation after the fact and does not add to the cost of testing. The I_{SB} value coupled with the corresponding F_{MAX} value put an IC in one of four categories as shown in Table 5.1. When I_{SB} is high, one expects F_{MAX} to be high representing a fast IC based on the fundamental relationship established by Fig. 5.1. However, if F_{MAX} happens to be low when I_{SB} is high, we are most probably dealing with a defective IC violating the established I_{SB} vs. F_{MAX} relationship. The adjustable upper limit (dashed line in Fig. 5.2) is determined by the user incorporating various components of variation. For example, many dice may be characterized by a Gaussian distribution with limits typically set at 3σ to 4σ or limits may be chosen based on empirical data and acceptable yield loss.

Table 5.1. IC decision matrix for I_{SB} and F_{MAX} testing.

I_{SB}	F_{MAX}	Decision on IC
H	H	Good - Fast
H	L	Defect
L	H	Unlikely
L	L	Good - Slow

The data shown in Fig. 5.1 came from a controlled experiment varying the channel length of hundreds of IC's. Thus, the population was not large enough to encounter defective IC's where their occurrence requires thousands being evaluated.

5.2. Intrinsic Leakage and Stand-by Leakage Reductions

I_{OFF} reduction can be effective in achieving high performance with "leaky transistors" while test engineers will be able to apply more conventional current test techniques. Such I_{OFF} reduction techniques include: (1) temperature reduction, (2) substrate backbiasing, (3) lowered quiescent V_{DD}, (4) multiple

transistor threshold designs, (5) alternative technologies (SOI). These are discussed below.

(1) Temperature: The subthreshold swing S_t predictably decreases with lowered temperature while V_T rises - both factors contribute to a decrease in I_{OFF}. For test practices that use T ≈ -50 °C (military applications), the reduction factor measured was 356; a relatively small fraction, but useful if intrinsic I_{DDQ} is on the order of 1-10 mA.

(2) Substrate (Well) Backbiasing: The V_{SUB} data show that backbiasing during the quiescent portion of a logic cycle offers significant reduction in intrinsic leakage current. Reduction factors between 2500 to 4400 were reported for backbiases between 2-3V. If GIDL (Gate Induced Drain Leakage) can be better controlled for larger substrate backbiases, larger reductions in I_{OFF} can be achieved.

(3) Lowering Quiescent V_{DD}: Leakage currents decrease as V_{DD} is lowered which is uniformly good for quiescent power reduction and reliability. However, lowering quiescent V_{DD} to decrease background I_{DDQ} to detect defects is more complicated.

(4) Multiple Threshold (MT) CMOS: Exponential reduction in I_{OFF} is possible if V_T increases. Leakage can be reduced by four orders of magnitude for a 150 mV change in V_T for a given process technology. This is the essence of the MT technique to reduce I_{OFF} [39, 55, 64].

(5) Alternative Technologies (SOI): SOI devices have small parasitic capacitance (aerial portion of junction capacitance is eliminated) and nearly ideal sub-threshold characteristics (60 mV/dec at room temperature if fully depleted). SOI represents a possible technology having better leakage (approaching ideal S_t of 60 mV/dec at room temperature hence better weak inversion leakage) and capacitive advantages. If we compare the room temperature weak inversion component of I_{OFF} of an SOI transistor (60 mV/dec) with the example in Section IV (80 mV/dec and V_T = 0.35 V), then the I_{OFF} reduction factor for SOI is 28X. Substrate backbiasing and other I_{OFF} reduction techniques can also be applied to SOI. This technology is reviewed in [39,55,56].

Acknowledgments – The authors wish to thank Anand Raghunathan of NEC USA, Angela Krstic of UCSB and Ali Kehavarzi of Intel for their efforts and contribution to this paper.

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