A Benchmark Suite for Substrate Analysis

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Abstract— The paper proposes an initial benchmark set, suitable for substrate analysis and test. The aim is to help accurately represent electrical noise injected into and picked up from substrate in a variety of high performance circuits. Creating an accurate image of such noise is becoming a critical requirement with the expansion of real plug-and-play style designs. Several important methods for the analysis of substrate parasitic coupling are reviewed in light of the effect substrate noise has on the performance of analog and digital ICs over a wide frequency spectrum. The requirements and formats for each benchmark are described in full detail to allow possible algorithmic as well as signal integrity tests.

I. Introduction

The IC industry is currently migrating from one based on stand-alone, individually packaged chips to one where so-called virtual components are its fundamental building blocks. Virtual components implementing various intellectual properties will be integrated onto a common silicon substrate and interconnected, using a Plug-and-Play design style. It is conceivable that seemingly diverse circuits will significantly interfere with each other to various degrees via interconnect lines (power rails, signal, clock), cross-talk, and substrate coupling. When lacking accurate means of predicting interferences, engineers tend to over- or underdesign the circuit, with a resulting excessive silicon area consumption and possibly lower performance. In this perspective, building an extensive description of the electrical interface and of all functionality and performance requirements is essential. The process of properly defining and formatting such information is referred to as *encapsulation*.

A complete electrical interface includes information about internal spurious activity as well as constraints on external parasitics and noise. There are two types of internal spurious activity in ICs: switching and intrinsic noise. Switching noise is the cumulative effect of thousands or even millions of logic gates changing state in a digital circuit at a given instant, while intrinsic noise is the consequence of a collection of physical phenomena associated with electronic circuits. There exist several mechanisms associated with the transport of noise: (a) power, signal and clock rails, (b) substrate, and (c) electromagnetic interferences. This paper focuses on substrate related noise.

Switching noise is injected into substrate through *impact ionization* and *capacitive coupling*. The first phenomenon occurs when electron-hole pairs are generated in the pinch-off region, when the electric field exceeds a given threshold. The excess holes are collected in the region of substrate under the device and from there they are transported throughout the chip. Capacitively coupled noise currents are generated when charges accumulate on one plate due to switching activity, while the other plate consists of low resistivity trenches, e.g. contacts, implanted directly in the substrate. Noise present in the substrate can modulate the threshold voltage of devices in the vicinity, thus impacting performance and possibly preventing correct circuit functioning. Alternatively it can be picked up by high-impedance interconnect through capacitive coupling, thus resulting in signal integrity problems. For a review of substrate noise injection and reception mechanisms, see [1, Chapter 2].

To help designers characterize noise present in the substrate due to capacitive coupling and impact ionization, there exist today a number of efficient algorithms for substrate extraction and macromodeling. In this paper we propose a benchmark suite aimed at testing such algorithms and comparing performance, accuracy and tradeoffs thereof. The paper is organized as follows. Section II gives an overview of state-of-the-art substrate extraction techniques, currently used or researched in academia and industry. Section III presents a minimum set of requirements as well as optional information which should be used to properly characterize every benchmark. Section IV describes the currently available benchmarks and the formats in which they are stored.

II. Substrate Analysis Techniques

The substrate analysis problem has been addressed by a number of authors since the 1970s, however the advent of advanced miniaturization has fundamentally revolutionized the field. Two main approaches have emerged. The first, known as macro-modeling, consists of generating compact analytical representations of substrate induced

parasitics [2, 3, 4]. The second approach is based on a fully numerical [5, 6, 7] or semi-analytical [8, 9, 10, 11] solution of the ordinary differential equations (ODEs) underlying substrate transport.

Characterizing substrate transport mechanisms requires the computation of the electric potential $\Phi(x,y,z,t)$ at any bulk point $\mathbf{r} = (x,y,z)$ in the vicinity of the substrate surface, i.e. $z \approx 0$. From Maxwell's equations one can show that

$$\frac{1}{\rho}\nabla \bullet \nabla\Phi(x,y,z,t) + \epsilon\frac{\partial}{\partial t}(\nabla \bullet \nabla\Phi(x,y,z,t)) = 0, \quad (1)$$

holds. Parameters ϵ and ρ are the local dielectric permittivity and the resistivity of the substrate. Equation (1) reduces to the Laplace equation

$$\nabla^2\Phi = 0, \quad (2)$$

in the electrostatic case. The boundary conditions of (2) set the potential (Dirichlet) and the electric field (Neumann) on some surfaces of the substrate. Generally the backplate is set to 0 Volts, while the substrate walls are have zero electric field in the perpendicular direction.

Equation (2) can be numerically solved using techniques based on some discretization of the (possibly anisotropic) space. An often utilized method, known as *box integration* technique, consists of partitioning the workspace into three-dimensional boxes indexed $\{i,j,k\}$ for dimensions $\{x,y,z\}$. Then, (2) is translated into a finite difference equation replacing the derivatives of Φ in each dimension as

$$\frac{\partial^2\Phi}{\partial^2 x} = \frac{\Phi_{i+1,j,k} - \Phi_{i-1,j,k} - 2\Phi_{i,j,k}}{\triangle_i^2},$$

where $\triangle_i$, $\triangle_j$, $\triangle_k$ are the sizes of the integration box. Similar substitutions are made for y and z-directions.

To find the potential in each node $\{i,j,k\}$ it is sufficient to compute the voltage at the center of an appropriately sized resistive mesh, assuming that the faces in each box are equipotential. By setting all the nodes associated with a given contact to 1 Volt and by measuring the current flowing out of each other contact, one can compute the resistance between each contact pairs. Techniques based on this concept are currently used in LAYIN [5].

The resulting system of simultaneous equations is diagonally dominant and sparse, since only seven elements in each row are non-zero. Hence, standard techniques for the solution of sparse linear systems can be applied [12]. The most commonly used methods in substrate-related literature are (1) *direct methods*, based on Gaussian elimination and LU decomposition; (2) *iterative methods*, based on Conjugate Gradient Algorithms, Jacobi and Gauss-Seidel Relaxation schemes; (3) *hybrid methods*, i.e. combination of (1) and (2); (4) *frequency domain methods*, based on Asymptotic Waveform Evaluation (AWE) and similar algorithms. The literature on the subject is extensive, for a review see [1, Chapter 3].

Due to the size of such systems of linear equations, iterative schemes are possibly the only practical solution. Frequency domain analysis is quite complex for multi-layered substrates, as the different layers of silicon have different time constants. To address this problem efficiently AWE has been used [7]. AWE produces an approximate representation of the frequency response by selecting appropriate low-order transfer functions to model the circuit. In these approaches a mixed RC mesh was originally used, which was more recently replaced by a purely resistive one. The reason for this is that the substrate behaves resistively upto frequencies of 4-5 GHz. At these frequencies however, the emergence of skin-effect modes in high-conductivity substrates complicates the modeling problem, thus making RC modeling inadequate [1, 6].

An alternative way to solve (2) is based on Boundary Element Methods (BEMs) on an approximation of the substrate which ignores horizontal conductivity gradients. The technique is the basis of Cadence Design Systems' and Texas Instruments' substrate extraction tools. The potential at each location $\mathbf{r}$ in the substrate volume V is given by

$$\Phi(\mathbf{r}) = \int_V \rho(\mathbf{r}')\Psi(\mathbf{r},\mathbf{r}')d^3\mathbf{r}' + \epsilon\oint_S (\Psi\frac{\partial\Phi}{\partial n} - \Phi\frac{\partial\Psi}{\partial n})\, ds',$$

where $/\partial n$ symbolizes the derivative with respect to $\hat{\mathbf{n}}$, the unit outward normal vector to surface S enclosing volume V. $\rho(\mathbf{r})$ represents a localized charge density. $\Psi(\mathbf{r},\mathbf{r}')$, called *Green's function*, relates the potential of a point in space to the charge present in a different location. If the location and geometry of each contact is known, a matrix relating the potential in a contact panel to the charge of all the remaining contact panels can be computed. Such matrix, known as the *coefficient of potential matrix*, needs be solved to evaluate the impedances between every contact pairs.

In [8, 9] the Green's function was computed for a finite uniform medium and later for a multi-layer substrate, with zero normal electric field boundary conditions, exploiting the technique of the separation of variables. Image-charge based concepts have been used, in order to avoid the series computation involved in the method. The Green's function for a multi-layer substrate can be approximated by a finite two-dimensional Discrete Cosine Transform (DCT) of a technology-dependent function [10]. The DCT can be computed in $\mathcal{O}(n\ log\ n)$ time, thus the computational bottleneck becomes the inversion of the coefficient of potential matrix, which is dense. In [1] a method was proposed to sparsify the coefficient of potential matrix while solving the underlying system of equations using iterative branch-and-bound methods. The sparsification procedure exploits knowledge of the loading of a subset of contacts. A beneficial byproduct of this procedure is the inherent reduction in size of the resulting impedance matrix, thus greatly improving the effectiveness of simulation.

When substrate analysis must be included in an optimization loop, there exist methods to reduce or eliminate the need for re-inverting the coefficient of potential matrix. Such methods generally use sensitivity analysis applied to the matrix or circuit components to speed-up computation. Such optimization-targeted substrate analysis has been embedded in placement and trend analysis tools as well as custom silicon compilers [13].

The problem of sparsifying the coefficient of potential matrix without requiring additional information has been attacked by almost every author. The most traditional method, proposed for example in [14], consists of ignoring the effects of remote contacts during the extraction, thus in effect forcing the coefficient of potential matrix to have a variable band structure.

A more robust and numerically stable method was proposed in [11]. The method exploits the smoothness of the Green's function of typical substrate-related problems and the fact that contacts in remote clusters have a similar effect over near contacts. This results in quasi-linearly dependent columns in the matrix, hence standard Singular Value Decomposition (SVD) techniques can be used to represent it. If the SVD of the matrix is used, vector matrix multiplications can be performed more efficiently, thus resulting in a overall complexity of $\mathcal{O}(n\ log\ n)$.

In another, more recent approach [15], the space is first discretized using a coarser, uniform set of panels, which is in turn partitioned into smaller panels. Then, a two-grid method (TGM) is applied to these two discretizations, iteratively, until either the finest possible discretization is reached or a certain tolerance on the residual of the local matrix inversion process is obtained. The TGM[1] at any given iteration consists of two steps. First, the preliminary result of the inverted matrix, as computed in the previous iteration, is used as a guess to solve a local problem in with a finer discretization. The result of the finer problem is then averaged and used to recompute the solution of the coarser problem. Complex contact profiles are partitioned into shapes of varying resolution which can be processed hierarchically.

An alternative approach [16] is based on the assumption that a current injected at a great distance is "seen" to have a very similar effect at two or more close-by pick-up points. Similarly, injecting a current in any of the close-by points has nearly the same effect on another distant pick-up point. The DCT can be modified to account for this fact as in [17], thus resulting in an overall smaller coefficient of potential matrix, and hence in higher computational efficiency.

Recently, a sensitivity analysis feature has been added to some substrate extractors. Computing sensitivities of substrate coupling is useful to project the effect of small ECOs or redesigns. It can also be used as a quality factor to select the most cost-effective technology or to evaluate the effects of slight imperfections in the fabrication process on the performance of a circuit and, ultimately, its yield. Finally, sensitivities can be used to build a performance model which accounts for discrete parasitics as well as substrate effects.

[1] The method can be extended to full-blown multi-grid.

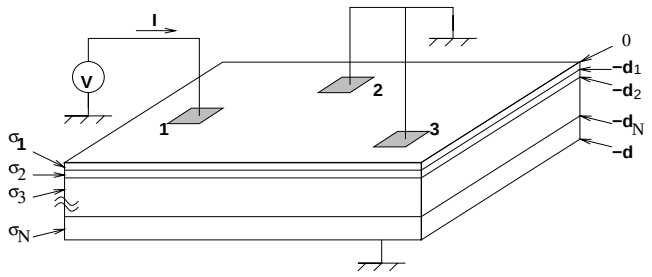

Fig. 1. *Measurement setup*

III. Benchmark Requirements

A. General Setup

In its most general formulation, substrate analysis consists of finding the current absorbed by a contact (e.g. "1" in Figure 1) when a voltage is applied to it and all the other contacts are grounded. Let M be the total number of contacts, each with its own properties (see Section C). Let $\mathbf{V}(t)$ be the vector of all the contact potentials as a function of time and $\mathbf{I}(t)$ the vector of all the currents absorbed by every contact. A parametrized transistor model should also be available to evaluate injected currents and threshold voltage modulation behavior. We use the models proposed in [18].

B. Doping Profile Modeling

Consider a typical substrate cross-section, relative doping levels are represented by continuous distributions. The substrate is fully described by the layers in which its doping profile is discretized. Let N be the number of such layers, $\sigma_i/\epsilon_i, i = 1 \ldots N$ the conductivity / dielectric constant of each layer, and $-d_i, i = 1 \ldots N$ the depth of each layer. Wells should be described in the same fashion, with the addition of their boundaries, defined individually for each well.

C. Contacts

The geometry of each contact is defined in terms of its lower-left and upper-right coordinates, contact depth c, and number of partitions per edge. If the partitions are non uniform, the exact position of each partition or the function used to derive them, e.g. $\log y$ or y^2, should be specified. See Figure 2. Additional parameters for the contact are its frequency-dependent conductivity $\sigma_c(\omega)$ and loading $Z_c = R_c(\omega) + j\ X(\omega)$. Notice that contacts can be multi-layer.

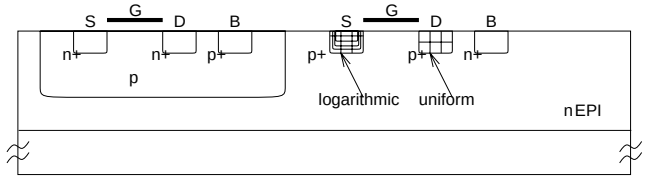

Fig. 2. *Contact partitioning*

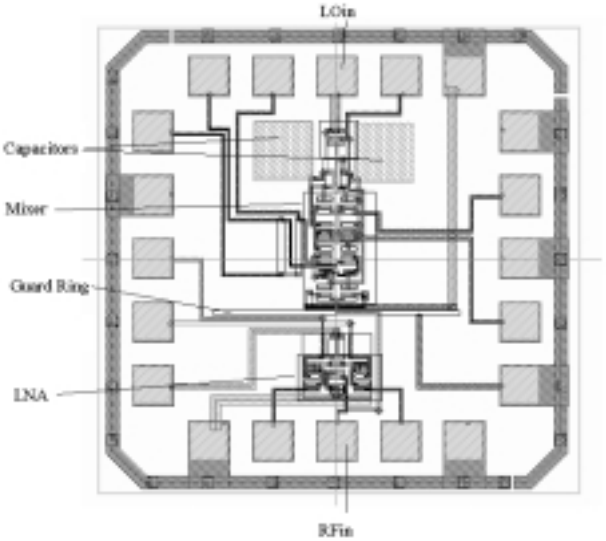

Fig. 3. *Layout of downconversion stage (Courtesy of Raminderpal Singh)*

There exist a variety of noise-sensitive structures: transistors, interconnect, capacitors, etc. The active area of devices subject to body effect [19] may be represented as a contact of dimension $W \times L$. Wells may also be represented as contacts with appropriate dimensions if their conductivity is much higher than that of the layer they are buried in.

D. Guard Rings

Guard Rings are one- or two-dimensional diffusion structures connected at the surface through highly conductive interconnect, generally metal. The goal is to attract substrate currents away from sensitive analog/RF circuitry, thus minimizing signal integrity problems. Guard rings are often used in mixed-signal and ASIC designs to combat substrate noise. Recently, similar structures have been used to insulate sensitive digital circuits, such as domino logic, from other digital circuits. As an illustration, consider the layout in Figure 3, where the guard ring isolates the Low Noise Amplifier circuitry from the Mixer.

Substrate and guard rings should be seen as part of a larger complete RLC parasitic model involving package and interconnects also. Often, it is not practical to change the package due to high costs, but it may be possible for the designer to try variations of bond pad connections and even look at multiple bond wires. This approach adds some effective variables to the guard ring problem which helps alleviate over- and underdesigning. Examples of such techniques include:

1. dedicated bond pads for those guard rings that have been simulated to show high current noise picked up from the substrate.

2. multiple bond wires to create a lower high frequency impedance to the off-chip ground line, through lower bond wire inductance.

Rectilinear guard rings can be viewed as four adjacent rectangular contacts. More complex structures should be represented as an array of rectangular contacts, with possibly variable depth and width. The size, location and materials of guard rings have traditionally been a intuitive guessing game for experience analog-focused designers. It is therefore important that they be precisely modeled using the same partitioning scheme as regular contacts.

E. Non-Determinism

Every measure discussed sofar should be provided along with its related statistical information. Substrate profiles as well as vertical and horizontal geometries should have 3σ spreads and, if available, an explicit distribution function. This information should be given for a given temperature.

IV. Initial Benchmark Set

Table I lists the initial set of benchmark circuits presently available on the WEB. The benchmarks are all implemented in a SCMOS technology specified in the description file, even though such a restriction is not necessary.

All the parameters of Section III are included. The benchmarks are currently available at the site `ftp://ic.eecs.berkeley.edu/pub/benchmarks`. Every benchmark includes the description file, the technology description, and additional information designers might need to successfully simulate the circuit. The format used to describe the benchmarks is a dialect of CIF. However, GDSII can also be used, where all additional information is stored in the text layer.

A general header describes the substrate:

```
(dimension 1e3 1e3 400)  /* x,y,z chip dimensions in um */
(number_of_layers 4 )    /* number of layers */
(layer_z_coord 399 2 1)  /* -d1, -d2, etc. */
(layer_resistivity 200e3 150e3 100e3 1e3)  /* in Ohm m */
(contact_partition linear) /* partitioning mode */
(contact_partition_number (x 50) (y 20))
(temperature 10C)        /* temperature */
(three_sigma .1 .1 .01)  /* dimension variance */
```

and it is followed by a description of all geometries:

```
L CAA; (c= 0.1); (Z= 1000); (r= 0.1); (x=2, y=2);
    B 16 720 -40 -2616; (c= 1); (Z= 10 + j100);
    B 92 528 70 -2540; (Z= 10 + j100);
    B 60 64 86 -2836; (Z= 100); (x=3, y=4);
    B 36 528 174 -2540; (Z= 0); (x=3, y=4);
    B 24 64 168 -2836;
```

where `L` signifies "layer", `B` "box", `c` the depth in μm, `Z` the load impedance in Ω, `r` the contact resistivity in Ωm, and `x/y` the partition number. The values immediately after the tag are the defaults. Note that the file will still be readable by any CIF parser, since the added information is in commented form. A similar comment-based format is available in GDSII.

V. Conclusions

A benchmark suite, designed to test and compare substrate analysis tools, is presented. The minimum set of requirements to satisfactorily represent the benchmarks is given, as well as the formats adopted. This paper presents a review of several currently available tools and the techniques on which their engines are based are also described.

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benchmark	function	poly cnt.	diff cnt.	g.r.
c145	comparator	9	145	-
c433	comparator	14	433	-
c566	OTA	12	566	-
c184	class AB	5	184	-
ardac	D/A	200	502	-
sd	SigmaDelta	230	2800	1
grid10	10×10	-	100	1
grid100	100×100	-	10000	4
pll	PLL	479	2666	3
rfdconv	downconversion	-	27	1

TABLE I
Initial benchmark set

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