A Sigma-Delta Modulation Based BIST Scheme for Mixed-Signal Circuits

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ABSTRACT

In this work, we present the analysis of a built-in self-test (BIST) scheme for mixed-signal circuits that is intended to provide on-chip stimulus generation and response analysis. Based on the sigma-delta modulation principle, the proposed scheme can produce high-quality stimuli and obtain accurate measurements without the need of precise analog circuitry. Numerical simulations are conducted to validate our idea and the results show that the scheme is a promising BIST approach for mixed-signal circuits.

I. INTRODUCTION

Testing of analog circuits has been a costly process because of the limited access to the analog parts and expensive automatic test equipment (ATE) required to perform functional testing. The situation has become worse due to the trend of integrating various digital and analog cores onto a single system-on-chip (SOC), in which testing the analog parts becomes the bottleneck of production testing.

To resolve the problem, various design for testability (DfT) and BIST approaches for mixed signal systems have been proposed. They either increase the controllability and observability of the circuit under test (CUT) [1, 2] or provide the capability of on-chip stimulus generation and signal analysis [3, 4, 5, 6, 7, 8]. In [3], the authors present a BIST scheme for a signal-to-noise ratio (SNR), gain tracking, and frequency response test of a sigma-delta analog-to-digital converter (ADC); however, the on-chip digital-to-analog converter (DAC) for sine-wave generation, and the digital signal processing unit able to perform the desired analysis are not always available. Implicit functional testing [4] uses the random patterns from LFSR (usually appears as part of the digital BIST structure) as the test stimuli; however, the on-chip or external DAC and ADC are needed for D/A and A/D conversions. The oscillation BIST scheme in [5] converts the circuit under test to a circuit that oscillates. However, the BIST circuitry in general cannot be shared among different CUT's. The sigma-delta modulated oscillator in [7] provides a digital solution to high quality on-chip sinusoidal stimuli. The main disadvantage is the area overhead of the oscillator. The on-chip signal measurement approaches in [6, 8] rely on accurate reference voltages and may suffer from process variations. The proposed BIST scheme in this paper employs the oversampling $\Sigma\Delta$ modulation principle for both stimulus generation and response analysis, and, as will be clear latter, can achieve high-quality stimuli and measurements without stringent hardware requirement. The objective of this paper is to provide the theoretical analysis foundation of the BIST scheme and to validate the idea with numerical simulations.

For stimulus generation, there have been some works [3, 7, 9, 10] that utilize the $\Sigma\Delta$ modulation technique. Among the works, the idea of periodic application of *software* generated single or multi-bit $\Sigma\Delta$ modulated digital bit streams [9, 10] to a low-resolution single or multi-bit DAC followed by a high-tolerance analog filter is of particular interest. The advantages of this approach include:

- The required BIST circuitry, i.e., the DAC and the filter, that converts the digital bit streams to analog signals does not have to be very accurate and can use simple and relatively high-tolerance analog components.
- Various band-limited analog signals can be generated by applying different digital streams and thus without hardware modification.

To achieve higher stimulus quality, multi-bit digital streams are preferable to single-bit ones (each additional bit in the DAC increases the SNR by approximately 6 dB); however, the need for measuring the transfer function of the multi-bit DAC to ensure the stimulus quality [11] makes it difficult for BIST application. Our contribution in this work is to provide a calibration method that utilizes on-chip resources to measure the transfer function of the multi-bit DAC. With the transfer function, the software multi-bit $\Sigma\Delta$ encoder can compensate for the DAC imperfection, e.g., the offset voltage error, the differential and integral nonlinearity, and gain error. The resulting digital bit streams, after passing the DAC and the analog filter, will produce high quality analog signal. Thus, high quality test stimuli can be generated without stringent requirement on the on-chip DAC.

For on-chip response analysis, previous works in [6, 8] rely on accurate analog reference voltages, which is either from external sources or on-chip circuitry, to compare against the signal to be analyzed. Although on-chip reference voltages are preferred as a BIST solution, they are vulnerable to process variation, and their inaccuracies have direct impact on the measurement quality. We resolve this problem by first converting the analog signals into one-bit digital streams by a one-bit $\Sigma\Delta$ encoder, and then employs digital signal processing techniques

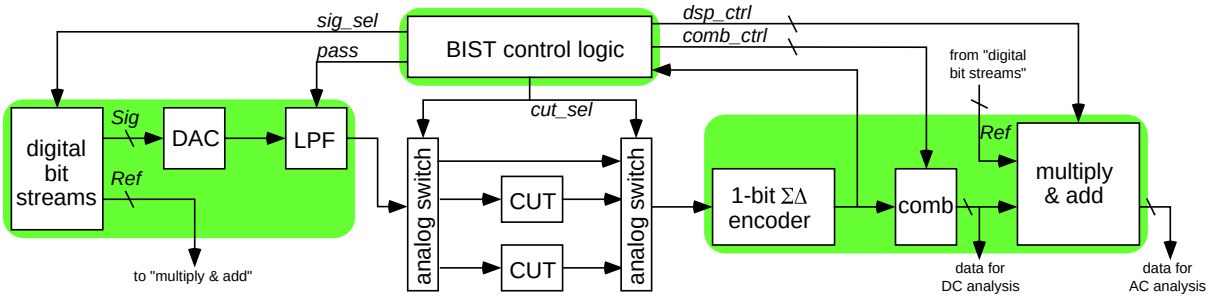

Fig. 1. The BIST architecture

to extract the desired information. The main advantages of this approach include

- The proposed scheme is more immune from analog imperfection because the oversampling one-bit $\Sigma\Delta$ encoder relaxes the need for precise analog circuit by using a much higher sampling frequency than the Nyquist frequency, and, in its simplest form, the encoder can be constructed with an integrator and a comparator.
- Sophisticated digital processing techniques, if allowed, can be used to further increase the measurement quality.

For digital signal processing, we focus on (1) the measurement of DC signal value, and (2) the discrete Fourier transform for AC analysis (the outputs of the discrete Fourier transform allow one to derive AC information like frequency response, SNR, gain, etc.) We use the comb filter, which is simple and widely employed in signal processing, for DC measurements, and analyze the required testing time to arrive at the desired accuracy. We also propose a DfT approach that can further reduce the testing time. For AC measurement, we investigate the trade off among hardware, testing time, and measurement errors for discrete Fourier transform. A series of numerical simulation is conducted to validate our idea—the frequency spectrum of a multi-tone signal is computed and the amplitude errors range from 0.02 to 0.06 dB.

This paper is organized as follows. We will first show the overall BIST architecture in Section II. Then, techniques and issues of stimulus generation and response analysis are discussed in Section III and IV, respectively. Finally, we conclude the work in Section V.

II. The BIST architecture

Fig. 1 depicts the proposed BIST architecture. The required BIST circuitry includes stimulus generator (the left shaded box), the BIST control logic, the signal processing unit (the right shaded box), and the analog switches surrounding the CUT's.

digital bit streams The source that provides digital bit streams for stimulus generation (Sig) and response analysis (Ref). In practice, this can be implemented by on-chip storage, digital signal processing unit, or is simply the interface to external digital stream sources. sig_sel selects the desired bit streams depending on the application and will be discussed latter.

DAC A low-resolution DAC that converts digital bit streams to discrete, continuous analog signals. It can be shared with an on-chip DAC (using only a few of its output levels) or could be dedicated BIST circuitry if no on-chip DAC is available.

LPF An analog low pass filter that removes the modulation noise in the DAC output and thus restores the test stimuli. When testing the BIST structure, $pass$ may be set to active to bypass the filter.

1-bit $\Sigma\Delta$ encoder An A/D converter that encodes its input analog signal into a one-bit digital bit stream. The encoder, often used in modern ADC's, can be from an on-chip ADC or is implemented as dedicated BIST circuitry if not available.

comb A digital comb filter that realizes the *integrate-and-dump* function. When supplied with input sequence x_i at sampling rate f_s, the output sequence y_k of the comb filter occurring at $f_D = f_s/D$ is defined by

$$y_k = \frac{1}{D} \sum_{i=D(k-1)}^{Dk-1} x_i \qquad (1)$$

where D is the decimation factor of the comb filter. Its control signals $comb\_ctrl$ include (1) the decimation factor D, (2) $comb\_reset$ which initializes its internal storage elements to zero, (3) $comb\_neg$ which, when activated, inverts its input bit stream, and (4) the $comb\_enable$ signal.

multiply & add Consisting of digital circuits that realize the multiply-and-add function for discrete Fourier transform. The dsp_ctrl control signal consists of (1) dsp_reset which resets its internal storage, and (2) dsp_enable which enables the unit. The "multiply & add" block can be implemented in software using on-chip processor core.

The necessary area overhead of the proposed scheme is the BIST control logic and the analog switches that select the circuit to be tested. Most of the other BIST resources are commonly found in modern mixed-signal designs.

III. Stimulus generation and testing the BIST structure

A discussion on the generation of $\Sigma\Delta$ modulated single or multi-bit streams for band-limited signals can be found in [10]. The basic idea is as follows: First, the desired analog signal is applied to a software $\Sigma\Delta$ encoder and a selected portion of the encoder's output is stored. Then, to restore the original signal, the stored portion is applied periodically to a DAC followed by a low-pass filter to remove the modulation noise. Depending on the available on-chip DAC, the software encoder generates either single or multi-bit digital streams. Although multi-bit streams are favored for their higher in-band SNR, that the encoder should be configured to use the DAC's *real* (instead of the *ideal*) transfer function to ensure the quality of the restored signal makes it difficult for BIST application because the on-chip response analyzer cannot be validated without a reliable signal source!

Assume that the DAC can generate at least two reliable output levels. The combined procedure for measuring the transfer function of the low-resolution DAC and testing the analog parts of the BIST structure (digital parts can be tested with standard digital testing approaches) consists of the following steps:

Pre-processing The software encoder is configured to use only two output levels of the DAC and generates the required waveforms for testing the on-chip one-bit $\Sigma\Delta$ encoder.

Testing the 1-bit $\Sigma\Delta$ modulator First, $pass$ and cut_sel are set such that the DAC output is directed to the $\Sigma\Delta$ encoder without passing LPF and any CUT. Then, one can apply the desired test stimuli to validate the encoder. Note that LPF can be by-passed here due to the low-pass nature of the encoder.

Testing the LPF The digital bit streams for testing the LPF are selected and bypass the CUT's. The outputs are then analyzed to validate the LPF.

Characterizing the DAC Each time, a fixed digital pattern is applied to the DAC and the corresponding output level is measured.

Stimulus generation The transfer function of the DAC is then incorporated into the software encoder to generate the desired multi-bit $\Sigma\Delta$ encoded streams for testing the CUT's.

IV. Response analysis

In this section, we will discuss how to use a first-order one-bit $\Sigma\Delta$ encoder to convert analog signals into digital single-bit streams and how to extract from these streams various DC and AC characteristics. Higher order encoders in general exhibit better performance at the price of reduced dynamic range. Fig. 2(a) shows the block diagram of a first-order $\Sigma\Delta$ encoder, and Fig. 2(b) is its corresponding discrete-time model. Our analysis is based on the discrete-time model which can be described by the difference equations

$$\begin{aligned} u_i &= e_{i-1} + u_{i-1} \\ e_i &= x_i - Q(u_i) \end{aligned}$$

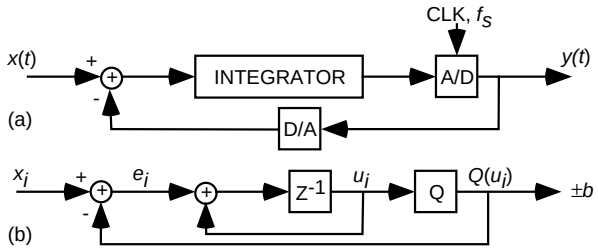

Fig. 2. The single-loop $\Sigma\Delta$ encoder

where x_i is the discrete time sample of the encoder input at sampling rate f_s, u_i is the state of the encoder and the binary quantizer is defined by

$$Q(u_i) = \begin{cases} +b, & u_i \geq 0 \\ -b, & u_i < 0 \end{cases}$$

Note that the quantizer outputs $+b$ and $-b$ correspond to the encoder outputs 1 and 0, respectively.

To extract either DC or AC information of the original signal, a digital comb (or integrate-and-dump) filter is employed to attenuate the modulation noise in the single-bit digital stream from the encoder. The comb filter is described by Eq. 1 and is considered here because of its simplicity (can be implemented with an up/down counter and a register.) Note that the decimation factor D must satisfy the requirement $f_D > f_o$ ($f_D = f_s/D$ and f_o is the Nyquist frequency of the input data.)

A. DC measurements

When the encoder is supplied with an analog DC signal $v \in [-b, +b]$ and the encoder's initial state u_0 lies in $[v-b, v+b]$ (the index 0 corresponds to when the comb filter is enabled,) the DC value decoded by the comb filter is

$$\hat{v} = \frac{1}{D} \sum_{i=0}^{D-1} Q(u_i),$$

and the error is bounded by ([12])

$$|\hat{v} - v| \leq \frac{2b}{D} \tag{2}$$

Since $f_o = 0$ for DC signal, there is no upper limit on D; therefore, the desired measurement accuracy, represented by the maximally allowed error ϵ, can be achieved by choosing D such that

$$D \geq \lceil 2b/\epsilon \rceil \tag{3}$$

Note that Eq. 3 is valid when both $v \in [-b, +b]$ and $u_0 \in [v-b, v+b]$ are satisfied. Although the former can always be achieved by limiting the input range, one in general has no control over the latter. In the following, we show how to determine whether $u_0 \in [v-b, v+b]$ is true by observing the *digital* output sequence of the encoder.

Let's first summarize the operation of the $\Sigma\Delta$ encoder with DC input v:

$$u_i = \begin{cases} u_{i-1} + v - b, & u_{i-1} \geq 0 \\ u_{i-1} + v + b, & u_{i-1} < 0 \end{cases}$$

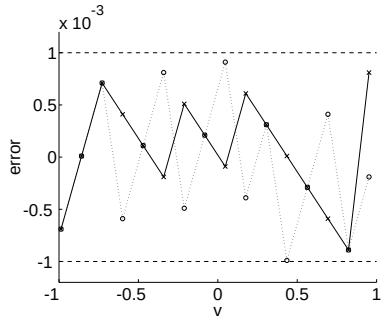

Fig. 3. Numerical results for DC measurements

Once u lies in $[v-b, v+b]$, all the succeeding u_i's will lie in $[v-b, v+b]$, too ([12]). Furthermore, it can be shown that

Lemma 1 *If $Q(u_i)$ and $Q(u_{i+1})$ have different signs, then $u_j \in [v-b, v+b]\ \forall j \geq i+1$.*

proof: When $u_i < 0$ and $u_{i+1} \geq 0$, one has

$$0 \leq u_{i+1} = u_i + (v+b) < v+b$$

and when $u_i \geq 0$ and $u_{i+1} < 0$, one has

$$0 > u_{i+1} = u_i + (v-b) \geq v-b$$

In either case, the claim is true.

Based on Lemma 1, the accuracy shown in Eq. 2 can be achieved if one enables the comb filter after a sign change (from 1 to 0 or 0 to 1) of the encoder output is observed. This can be controlled by the BIST control logic and $comb\_ctrl$ signal (Fig. 1).

The above method assumes no control over the internal state of the 1-bit $\Sigma\Delta$ encoder. In fact, a better performance can be achieved if the encoder has the DfT feature that allows one to set its state to desired values. A more detailed description of the modulation error is ([12])

$$v - \hat{v} = \frac{2b}{D}\left(\langle z + D\beta\rangle - z\right)$$

where $z = (u_0 + b - v)/2b$, $\beta = (b+v)/2b$, and $\langle r\rangle$ denotes r mod 1, that is, the fractional part of r. By choosing $u_0 = v$, one has $z = 1/2$ and

$$|v - \hat{v}| \leq b/D \tag{4}$$

which, compared to Eq. 2, stands for half the error, or equivalently, half the testing time for a given ϵ. The block diagram of the encoder (Fig. 2(a)) indicates that this is equivalent to setting the state of the integrator to be the same as the input value. Note that in this case, one does not have to wait for the encoder's output change to enable the comb filter.

A.1 The DC measurement procedure

The procedure for measuring a DC value v consists of the following steps:

1. Compute D according to Eq. 2 or Eq. 4 depending on if one can control the value of the encoder's internal state.
2. Set sig_sel to select the digital bit stream for the desired test stimulus.
3. Set cut_sel to select the CUT.
4. Reset the comb filter's storage to zero.
5. Enable the comb filter upon the detection of the first sign change of the encoder output or after one sets the internal state of the encoder to v.
6. The estimation of v is at the output of the comb filter after D cycles.

To measure the difference between two DC values, say v_1 and v_2, which is usually used in static tests for DAC's, the above procedure is executed twice. Note that, in the second run when v_2 is applied, we skip the fourth step and set the $comb\_neg$ control signal to invert the filter's input and thus obtain $v_1 - v_2$ after another D cycles.

A.2 Numerical simulation

In Fig. 3, we show the numerical results for DC measurements with the settings $b = 1$ and $\epsilon = 0.001$ for different v's ($|v| < 1$). The horizontal and vertical axes represent the input value v and the measurement error $\hat{v} - v$, respectively, and the two horizontal dashed lines correspond to $\pm\epsilon$. The solid line corresponds to "wait" for the sign change ($D = 2b/\epsilon = 2000$), and the dotted line corresponds to "preset" the state of the integrator to v ($D = b/\epsilon = 1000$). In the "wait" experiment, the encoder's initial state is a random variable between $-2b$ and $+2b$. It can be seen that both methods accomplish the desired accuracy; however, the "preset" technique requires only half the testing time.

B. AC measurements

For AC signal measurements, we focus on the efficient implementation of the discrete Fourier transform. The frequency spectrum of the AC signal can be built with multiple runs of discrete Fourier transform, and one can derive other AC characteristics e.g., gain and SNR, from the knowledge of the frequency spectrum. In the following analysis, we assume that the principle of coherent sampling [13] is followed.

Let v_i, c_i, s_i ($i = 0, 1, \ldots, N-1$) be the signal to be analyzed, the reference sine and cosine signals (at frequency f and unity amplitude), respectively. (v_i, c_i, s_i are sampled at the same rate f_s.) Then the signal amplitude of v at $f = kf_p$ (denoted by $v(f)$), where $f_p = f_s/N$ and $k = 0, 1, \ldots, N/2-1$, can be obtained with two runs of cross correlation:

$$v_{cos} = \frac{2}{N}\sum_{i=0}^{N-1} v_i c_i \tag{5}$$

$$v_{sin} = \frac{2}{N}\sum_{i=0}^{N-1} v_i s_i \tag{6}$$

followed by

$$v(f) = \sqrt{v_{cos}^2 + v_{sin}^2} \tag{7}$$

In our BIST scheme, v_i corresponds to the output of the comb filter, while c_i and s_i are stored in "digital bit streams".

TABLE I
FIND THE BEST DECIMATION FACTOR

f/f_s	1	2	4	8	16	32	64
2^{-12}	-0.0015	-0.0052	-0.0010	-0.0002	-0.0001	-0.0001	-0.0005
2^{-11}	-0.0126	-0.0184	-0.0060	-0.0014	-0.0006	-0.0008	-0.0025
2^{-10}	0.0053	-0.0247	-0.0003	-0.0029	-0.0016	-0.0030	-0.0093
2^{-9}	0.0643	-0.0032	-0.0066	-0.0011	-0.0036	-0.0096	-0.0360
2^{-8}	0.0492	0.0289	0.0115	0.0035	-0.0055	-0.0364	-0.1217
average	0.0266	0.0161	0.0051	0.0018	0.0023	0.0100	0.0340

When D is set to one, the comb filter is not functioning (or bypassed.) Eq. 5–6 can be realized with an adder (the output bit stream of the $\Sigma\Delta$ modulator has only two levels.) However, since the un-filtered bit stream still carries out-of-band modulation noise, the amplitude resolution of c_i and s_i must be high enough, e.g., 12-bit or floating point precision, to ensure high quality measurement (shown later.)

When D is other than one, the comb filter will attenuate the out-of-band modulation noise and thus relaxes the accuracy requirement on c_i and s_i. However, care must be taken when selecting D. The spectral density of the modulation noise of a $\Sigma\Delta$ encoder output may be expressed by

$$N(f) = 2e_{rms}\sqrt{2\tau}sin\left(\pi f\tau\right)$$

where $e_{rms}^2 = b^2/3$ and $\tau = 1/f_s$. The transfer function of a comb filter with decimation factor D is

$$H\left(f\right) = \frac{sinc\left(\pi fD\tau\right)}{sinc\left(\pi f\tau\right)} \tag{8}$$

Thus, the total noise power at the output of the comb filter is then

$$\int_0^{f_s/2} \left|N(f)H(f)\right|^2 df = \frac{4b^2}{3D^2} \tag{9}$$

Eq. 9 states that the noise power decreases with increased D; however, larger D also increases the unwanted side effect of attenuating the in-band signal.

The best decimation factor can be obtained via numerical simulation: For example, let $N = 4096$, $b = 1$, and the signal band be from DC to $f_s/2^r$ ($r = 8$ in this example and f_s is the sampling frequency.) We use Eq. 5–7 to compute the amplitude error of sinusoidal sine waves with amplitude $0.7b$ for different D's ($D = 1$ corresponds to no filtering at all) and the results are shown in Table I. The first row is the decimation factor up to 2^6 (larger D's will attenuate the in-band signal too much to be acceptable.) The first column corresponds to the signal frequencies. Because the comb filter tends to attenuate high-frequency signals more than low-frequency ones, the lowest frequency we use is $f_s/2^{r-4}$. The bottom row is the average of the absolute amplitude error for each D, and we find that in average $D = 8$ is the best choice.

B.1 The AC measurement procedure

The procedure for applying discrete Fourier transform to a sampled sequence v_i ($i = 0, 1, \ldots, N-1$) to obtain its signal amplitude at f is:

1. Set D to one or use the above method to find the best choice of D.
2. Set cut_sel to select the CUT.
3. Set "sig_sel" such that Sig is the desired digital bit stream for the test stimulus, and Ref the digital bit stream of the reference cosine wave at frequency f.
4. Reset the contents of "multiply & add" to zero.
5. Enable "multiply & add" and execute Eq. 5.
6. Same as 3, except that Ref is the reference sine wave.
7. Enable "multiply & add" and execute Eq. 6.
8. Execute Eq. 7.

Since N, the length of the sequence to be analyzed, is known, one can reduce Eq. 5 and 6 to sum of product which can be performed by "multiply & add" (the $2/N$ factor instead appears in the acceptable range.) Also, in most applications where signal power is of interest, the square root operation in Eq. 7 is not needed.

To compute the gain of the CUT, one run of discrete Fourier transform at the signal frequency is sufficient. For gain tracking, the signal power within the signal band of interest is computed with multiple runs of discrete Fourier transform. For SNR calculation, sum of the noise power in the signal band is obtained with multiple runs of discrete Fourier transform (note that the "multiply & add" is reset only at the first run.)

B.2 Numerical simulation

Using the same setup as the previous example, we conduct the following simulations to validate the response analysis scheme. The test signal we use contains three tones—$5f_p$, $11f_p$, and $13f_p$, where $f_p = f_s/4096$.

In Fig. 4, we compare the the spectra corresponding to the "original" signal and $\Sigma\Delta$ modulated signal (denoted by"limit" because this is the best one can obtain.) The horizontal axis is the frequency normalized by f_p, and the vertical axis is the signal amplitude in dB. One can see that after the signal is modulated by the $\Sigma\Delta$ modulator, the noise floor rises. The noise floor can be lowered by increasing the sampling rate f_s.

In Fig. 5, the spectra obtained using different combinations of D and c_i, s_i are shown. The setup "limit" is the same as that in Fig. 4), and is shown here for comparison purpose. For all the other configurations, the setup is as follows:

- The signal to be analyzed is modulated by the $\Sigma\Delta$ modulator into 1-bit stream.
- In the "D=8" experiment, the sine and cosine reference signals are modulated by the software $\Sigma\Delta$ modulator. Comb filters with decimation factor $D = 8$ are employed to remove the out-of-band modulation noise for all three modulated signals.
- In the experiments "8-bit", "12-bit", "16-bit", and "float", the comb filter is bypassed (by setting $D = 1$), and the reference signals are stored as 8, 12, 16 bit integers or as floating point numbers (without being modulated by the $\Sigma\Delta$ modulator.)

For all the configurations, the amplitude errors for the three signal tones (the three spikes in the spectrum) are small with a maximum of 0.062dB. However, the "D=8" configuration results in the highest noise floor.

In terms of the required hardware, the configurations "8-bit"–"float" can be realized with an adder able to perform the addition/subtraction at the speed f_s, and $2N$ samples of the reference signals are required, which corresponds to $16N$ bits for the "8-bit" configuration. On the other hand, the "D=8" configuration needs a 4-bit multiplier and an adder running at a lower speed $f_s/8$. $2N/D$ samples of the reference signals must be stored, which corresponds to $N/4$ bits. The choice of configuration depends on the available hardware resource, the allowed area overhead, and the required test accuracy.

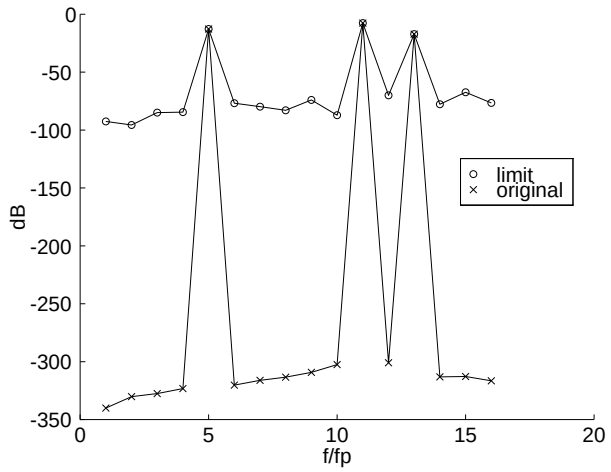

Fig. 4. Frequency spectra of the original and modulated signals.

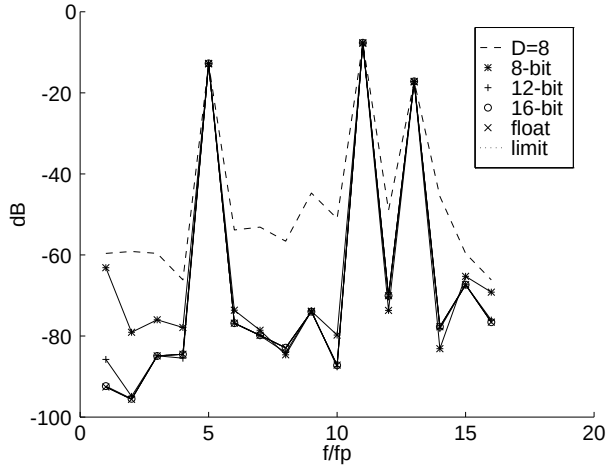

Fig. 5. Numerical results for AC measurements

V. Conclusion

We propose a $\Sigma\Delta$ modulation based BIST scheme for mixed-signal SOC's. For stimulus generation, an on-chip self-calibration method is presented. For DC value measurement, we provide methods to achieve any desired level of measurement accuracy, and for AC analysis, we analyze the accuracy corresponding to different frequencies, and decimation ratios. The results are validated by numerical simulation. We will further investigate on improving the performance of our techniques, and validate our ideas with hardware implementation.

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