Design Challenges for 0.1um and Beyond

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Abstract - If we look into the scaling law carefully, we find that three crises can be stringent in realizing LSI's for 0.1um and beyond: namely power crisis, interconnection crisis, and complexity crisis. This paper describes these crises and possible solutions to cope with the problems.

Summary

If we look into the scaling law carefully, we find that three crises can be stringent in realizing LSI's for 0.1um and beyond: namely power crisis, interconnection crisis, and complexity crisis. As for power crisis, there are activities to lower the power consumption from device level, circuit level to system level. Lowering supply voltage ($V_{DD}$) is very effective in reducing the power but the threshold voltage ($V_{TH}$) should be reduced at the same time for high-speed operation. The low $V_{TH}$, however, increases the leakage current. To overcome this situation, $V_{TH}$ and $V_{DD}$ control through the use of multiple $V_{TH}$ variable $V_{TH}$ and variable $V_{DD}$ are intensively pursued and some have been productized. At the system level, system LSI approach is promising for realizing low power and the new trend is to exploit cooperation of software and hardware. In the sub-1-volt design, watch out for the abnormal temperature dependence of drain current.

The interconnection will be determining cost, delay, power, reliability and turn-around time of the future LSI's rather than MOSFET's. RC delay problem can be solved through LSI architecture realizing "the further, the less communication" with the help of local memories.

It is just impossible to design LSI's with 100 million transistors from scratch. The complexity issue can only be solved by the sharing and re-use of design data. So-called IP-based design will be preferable. The virtual components are put together on a silicon to build billion transistor LSI's, which can be compared to the present system implementation with pre-manufactured LSI components.

References


Fig. 4 VDD, Power and Current Trend (From SIA)

<table>
<thead>
<tr>
<th>Power range</th>
<th>Concerns</th>
<th>Typical applications</th>
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<tr>
<td>&lt; 0.1W</td>
<td>Battery life</td>
<td>Portable, PDA, Communications</td>
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<td>~ 1W</td>
<td>Inexpensive package limit</td>
<td>Consumer, Set-Top-Box, Audio-Visual</td>
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<td>&gt; 10W</td>
<td>Ceramic package limit</td>
<td>Processor, High-end MPU’s, Multimedia DSP’s</td>
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Fig. 5 Necessity for Low-Power Design

- NMOS ➔ CMOS (Cost up)
- Bipolar ➔ CMOS (Speed down)
- Not cost nor speed but power set the technology trend.
- Integration can achieve low cost and high speed as a system.

Fig. 6 What sets the technology trend?

$$P = \alpha V_C \frac{V_{DD}^2}{2} \left[C_L \left(\frac{V_{DD}}{V_T}\right)^\alpha + \frac{V_{DD}}{V_T} + 1\right]$$

- $V_{ON}$: Charging & discharging
- $V_{OFF}$: Crowbar current
- $V_{DC}$: Static current
- $V_{TH}$: Threshold leak current

Fig. 7 Expression for CMOS Power

Fig. 8 Voltage waveform of CMOS inverter

Fig. 9 Short-circuit power dissipation formula

$$P_S = \frac{k(V_{DD})}{V_{DD}^2} \left[C_L \left(\frac{V_{DD}}{V_T}\right)^\alpha + \frac{V_{DD}}{V_T} + 1\right]$$

- $g_T(V_T, \alpha) = \frac{V_T^2 (V_T - V_D)}{2k(V_{DD})}$
- $h(T, \alpha) = 2(V_T - V_D)$

$$\eta = \frac{P_S}{P_0} = \frac{I_{TH}}{I_{TH(m)}}$$

Fig. 10 The change of the short-circuit power dissipation with scaling


Fig. 11 VDD, VTH, Power and Current Trend

$$P = \alpha f C V_{DD} + \text{leakage (sub-Vth, gate, D/S)}$$

- Low-voltage: Variable-Vth, multi-Vth (Super-Cut-off CMOS, dynamic leakage cut-off SRAM, positive temp. coeff. for CMOS, optimum voltages)
- Low-power: multi-Vth (Software control)
- Low-swing: Bus, clock, interconnection (Reduced clock swing FF, bus with sense-amp FF, low-power repeater insertion)
- Easy library generation for early adoption of new tech.

Fig. 12 Solving power issues
Fig. 13 Power and delay

Fig. 14 Standby Power Reduction (SPR) Circuit

Fig. 15 Self-Adjusting Threshold-voltage Scheme

Fig. 16 Measured leakage in SAT+SPR

Fig. 17 Multi-Threshold CMOS Circuit

Fig. 18 Super Cut-off CMOS (SCCMOS). H. Kawaiyachi and K. Nose, 'A CMOS Scheme for 0.5V Supply Voltage with nano-Ampere Standby Current,' ISSCC, pp.192-193, Feb. 1998.

Fig. 19 Super Cut-off CMOS Scheme (SCCMOS)

Fig. 20 Delay characteristics (inverter & NAND)

Fig. 21 Losing information in standby

Fig. 22 Dynamic Leakage Cut-off
**Fig. 23** Power Distribution in CMOS LSI's

**Fig. 24** Reduced Clock Swing Flip-Flop

**Fig. 25** Positive temp. coeff. in low-voltage

**Fig. 26** Cause of positive temp. dependence of transistors (Igs)

**Fig. 27** SOI Processors in ISSCC '99

**Fig. 28** Hi-Speed is Low-Power.

**Fig. 29** Approach to low-power LSI

**Fig. 30** Homogeneous vs. Heterogeneous

**Fig. 31** Software feedback loop for low-power

**Fig. 32** DRAM Embedding
Fig. 33: Compact yet High-Performance (CyHP) Library for Low-Power Technologies

Fig. 34: Interconnect determines cost & perf.

Fig. 35: Interconnect parameters trends

Fig. 36: RC delay and gate delay

Fig. 37: RC delay of global interconnections

Fig. 38: Delay and Power Optimization for Repeaters

Fig. 39: The further, the less

Fig. 40: Locality in space & time

Fig. 41: Capacitive Coupling Noise
Fig. 42 Coupling noise in RC bus

Fig. 43 Coupling among Interconnection

Unscaled / anti-scaled
- Clock
- Long bus
- Power supply

Scaled interconnection

1V 16W > 15A current
6% noise -> 0.05V noise -> 3mΩ sheet R -> 0.1μm thick Al
Area pad + package, or thick layer on board is needed.

Fig. 44 Interconnect Cross-Section and Noise

Fig. 45 Skin Effects for Signal Lines

Fig. 46 Inductive Effects

Fig. 47 System LSI design complexity increases faster than productivity (http://notes.sematech.org/97elec.htm)

Fig. 48 Overcome complexity crisis

Fig. 49 LSI in 2014

Fig. 50 Chip in 2014