An Analytic Calculation Method
for Delay Time of RC-class Interconnects

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Abstract— This paper presents an analytic 3rd order calculation method, without simulations, for delay time of RC-class circuits, which can be conveniently used to model on-chip interconnects. While the proposed method requires comparable evaluation time to the previous 2nd order calculation method, it ensures more accurate results than those of 2nd order method. The proposed analytic delay calculation method guarantees allowable error tolerance when compared to the results obtained from the AWE technique or HSPICE and has better performance in evaluation time as well as numerical stability. The first algorithm of the proposed method requires 7 moments for the 3rd order approximation and yields accurate delay time approximation. The second algorithm requires 5 moments for the 3rd order approximation and results in shorter evaluation time, the accuracy of which may be less than the first algorithm.

I. INTRODUCTION

As the device and process technology are improving, delay times of signal propagation due to on chip interconnects become larger than those due to gates. Interconnects are related, directly or indirectly, to the delay time as well as die size, power dissipation in the form of capacitive load and signal coupling due to dense routing. Hence much efforts and researches have been concentrated on the interconnect parameter extraction, modeling and analysis for the accurate estimation and verification of the performance of on chip interconnects. Since interconnects can be analyzed accurately after physical design stage, it is hard to handle interconnects in such a precharacterized form as used for gates. It is a generally accepted approach to use wire load model for interconnect delay based on statistical techniques before physical design and to analyze the interconnect delay using extracted circuit parameters and circuit models after physical design.

In circuit extractors, the modeling of on chip interconnects generally consists of extracting parasitic parameters for a uniform structure, dividing it into small segments, substituting the T- or Π - RC lumped model for each segment, and finally cascading each segment. In this method, overall interconnection networks become RC tree, RC mesh or the compound form of these. The potential problem of this method is that the resultant circuit may be extremely large. Hence, for the delay analysis of interconnects, model order reduction techniques such as Elmore delay[1] and AWE[2] based on the moment matching is largely used rather than the direct analysis method, owing to its lower time complexity.

Elmore delay, the first moment of the impulse response, has been used as a common metric of the RC interconnect signal delay due to its simplicity. As the signal transition time becomes shorter, however, signal bandwidth and maximum operating frequency become higher [3]. Also the current technology trend, such as the device size reduction for highly integrated circuit and the die size increment for high functionality, lengthen the average length of the on chip interconnects, which result in the resistance shielding effect [4]. Owing to the above-mentioned reasons, Elmore delay becomes inadequate delay metric for the high performance circuits.

Contrary to Elmore delay which approximates the interconnect delay using only one time constant, AWE (Asymptotic Waveform Evaluation), a representative method of the order reduction approximates the interconnect delay using q time constants obtained from $2q$ moments. While AWE requires more evaluation time than Elmore delay, it ensures accurate results comparable to those of the circuit simulator such as SPICE. Generally, for the RC interconnects of the chip whose operating frequency is lower than several GHz, delay times can be calculated within 10% error tolerance when compared to the results obtained from SPICE [5]. Because of the effectiveness in evaluation time, much efforts were concentrated on the calculation of the delay time of on chip interconnects analytically. Recent works presented an analytic second order approximation algorithm for the on chip interconnect delay time using RC-class [6] or RLC-class [7]. However, considering that second order approximation may result in inaccurate result for high-performance chips and

systems, it would be agreed that an analytical algorithm for the third order approximation is necessary.

In this paper, we present two analytical algorithms to calculate the delay time of on chip RC networks, based on stable 3 pole approximation. The first proposed algorithm requires 7 moments of the impulse response, and the second one requires 5 moments. Since these algorithms calculate poles without nonlinear iterative method used in AWE, the proposed method improves the evaluation time extremely and overcomes the defect of AWE which is sensitive to numerical noise.

This paper is organized as follows. Following the introduction, in Section 2, we explain Elmore delay and AWE briefly as a background. We pesent two algorithms to calculate poles and residues analytically in Section 3. Since these algorithms calculate poles and residues analytically without iteration, they have several advantages as follows. (1) Evaluation time can be improved extremely. (2) Numerical errors can be reduced. (3) The stability of the resultant circuit model is ensured. The stability of the resultant circuit model is particularly one of the weakness of the model order reduction algorithms such as AWE, which have to use stabilization methods to obtain stable circuit models by means of moment shifting [8] or implementation of passive networks [9]. In Section 4, the results of the proposed method are compared to those of AWE and SPICE. Section 5 concludes this paper.

II. BACKGROUND

A. Elmore Delay

Elmore delay is used as a common delay metric of the on chip RC interconnects due to its simplicity in calculation process. Elmore delay of the on chip RC interconnects having N nodes has $O(N)$ time complexity. For the on chip RC tree, the Elmore delay at some node i, T_{Di}, can be expressed as [10]:

$$T_{Di} = \sum_k R_{ki} C_k \qquad (1)$$

where R_{ki} is the sum of common resistances of the path between node k to the input node and the path between node i to the input node, and C_k is the capacitance at node k.

Assuming $h(t)$ to be the unit step response at a certain node, Elmore delay is related to the *mean* time (or the first moment, m_1) if we regard the impulse response as a probability density function ($\int_0^\infty h'(t)dt = 1$), which is expressed as:

$$T_D = m_1 = \int_0^\infty t \cdot h(t)dt \qquad (2)$$

It is known that impulse responses of the practical on chip interconnects leans to the left. Hence if we consider the waveform as a probability density function, we can express the following relation:

$$Mode \leq Median \leq Mean \qquad (3)$$

Since the definition of the delay time is the difference in times between 50% points of input and output, it is the *median* rather than *mean*. However, delay time approximation by Elmore delay uses the *mean* value of impulse response as the *median* value and may result in pessimistic estimation, e.g., an upper bound of the real delay time [10].

B. AWE Technique

The transfer function between a pair of terminal for any linear, lumped, passive circuit is expressed as:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1 + b_1 s + b_2 s^2 + \ldots + b_m s^m}{1 + a_1 s + a_2 s^2 + \ldots + a_n s^n} \qquad (4)$$

If we transform Eq.(4) to Eq.(5), we call the coefficient of ith term as the ith moment at the node.

$$H(s) = m_0 + m_1 s + m_2 s^2 + \ldots \qquad (5)$$

Laplace transform of impulse response in time domain, $h(t)$, is expressed as:

$$H(s) = \int_0^\infty h(t)e^{-st}dt \qquad (6)$$

Hence the expansion of e^{-st} about $s = 0$ by *McLaurin Series* is expressed as:

$$
\begin{aligned}
H(s) &= \int_0^\infty h(t)[1 - st + \frac{1}{2!}s^2 t^2 - \frac{1}{3!}s^3 t^3 + \ldots]dt \\
&= \sum_{k=0}^\infty \frac{(-1)^k}{k!}s^k \int_0^\infty t^k h(t)dt \qquad (7)
\end{aligned}
$$

From eq.(7), j^{th} coefficient of eq.(5), m_j, is expressed as:

$$m_j = \frac{(-1)^j}{j!} \int_0^\infty t^j h(t)dt \qquad (8)$$

The procedure to approximate poles in AWE consists of performing $2q$ dc analyses to obtaining $2q$ moments, and building q^{th} transfer function using $2q$ moments. For example, when approximating a complex RC tree circuit to a 3rd order transfer function, 6 moments are required, which can be obtained through 6 successive dc analyses. Using the moment values, eq.(9) is formed, and the 3 roots (e.g. 3 poles) of the characteristic equation, eq.(10), are computed.

$$
\begin{bmatrix} m_0 & m_1 & m_2 \\ m_1 & m_2 & m_3 \\ m_2 & m_3 & m_4 \end{bmatrix}
\begin{bmatrix} a_3 \\ a_2 \\ a_1 \end{bmatrix} =
\begin{bmatrix} m_3 \\ m_4 \\ m_5 \end{bmatrix} \qquad (9)
$$

$$a_3 x^3 + a_2 x^2 + a_1 x + 1 = 0 \qquad (10)$$

LU decomposition is a common method to obtain the vector 'a' values in eq.(9) and $Newton - Raphson$ or $Laguerre$ method is used to obtain the roots of the characteristic equation [11]. Once the reduction of the circuit to a q pole system has been done, j^{th} moment can be expressed in terms of poles and residues as:

$$m_j = \sum_{i=1}^{N} \frac{k_i}{(p_i)^{j+1}} \qquad (11)$$

where k_i is the ith residue, p_i is the ith pole of the corresponding node. Hence we can calculate the residues using eq.(11).

III. ANALYTIC ALGORITHMS FOR 3rd ORDER APPROXIMATION

A. Algorithms for 3 Pole Approximation

Moment matching used in AWE has two main flaws. The first is that the method is very sensitive to the numerical noise produced by computer which has finite precision, due to the divergence characteristic of circuit moments. The second is that it requires non-negligible evaluation time for calculating poles due to embedded iterative procedure such as $Newton-Raphson$. We discuss numerical noise briefly below, the details of which are dealt in [8]. When reducing big RC circuits, which have many poles, to simple RC circuits, the effect of high frequency poles to be removed from the circuit may transform the resultant circuits unstable as it gets combined with numerical noise such as truncation error. To overcome this problem, numerous methods have been presented [9], but most of them have a problem in that they require large evaluation times.

The analytical algorithms presented in this section not only overcome the problem discussed above, but also ensure faster evaluation than AWE for obtaining poles. We present two analytical algorithms. The first one (denoted as '$Method - 1$') generates q^{th} transfer function using 2^q moments, and ensures accurate delay time approximations. The second one (denoted as '$Method - 2$') requires $2q$ moments for approximating q^{th} order transfer function, and ensures faster evaluation than $Method - 1$, but its accuracy may be less than that of $Method - 1$.

A.1 Method-1: Approximation of 3 poles using 7 moments

A.1.1 First pole approximation

As the order increases, the ratio of successive moments converges to the dominant pole, which is expressed as [12]:

$$p_1 = \lim_{i->\infty} \frac{m_i}{m_{i+1}} \quad (i : 0, 1, 2, \ldots) \qquad (12)$$

Eq.(12) can be expressed as Eq.(13) in terms of Eq.(11).

$$\frac{m_i}{m_{i+1}} = p_1[1 + \frac{k_2}{k_1}(\frac{p_1}{p_2})^{i+1}(1 - \frac{p_1}{p_2})$$

$$+ \frac{k_3}{k_1}(\frac{p_1}{p_3})^{i+1}(1 - \frac{p_1}{p_3}) + \ldots]$$

$$(i : 0, 1, 2, \ldots) \qquad (13)$$

Since the definition of poles tells $|p_1| < |p_2| < \ldots < |p_n|$, as i increases, Eq.(13) converges to p_1. Hence the equation for the first pole approximation is expressed as:

$$p_1 = \frac{m_6}{m_7} \qquad (14)$$

A.1.2 Second pole approximation

For the second pole approximation, we define A_i as:

$$A_i = \frac{m_i}{m_{i+1}} - \frac{m_{i+1}}{m_{i+2}} \qquad (15)$$

From eq.(13), we obtain eq.(16),

$$A_i = p_1[\frac{k_2}{k_1}(\frac{p_1}{p_2})^{i+1}(1 - \frac{p_1}{p_2})^2 + \frac{k_3}{k_1}(\frac{p_1}{p_3})^{i+1}(1 - \frac{p_1}{p_3})^2 + \ldots] \qquad (16)$$

and we can derive eq.(17) in terms of eq.(16).

$$\left| \frac{A_i}{A_{i+1}} \right| = \frac{p_2}{p_1}[1 + \frac{k_3}{k_2}(\frac{p_2}{p_3})^{i+1}(1 - \frac{p_2}{p_3})\frac{(1 - \frac{p_1}{p_2})^2}{(1 - \frac{p_1}{p_3})^2} + \ldots] \quad (17)$$

As i increases, eq.(17) converges to $\frac{p2}{p1}$. Hence the equation for the second pole approximation is expressed as:

$$p_2 = p_1 \cdot \left| \frac{A_4}{A_5} \right| \qquad (18)$$

A.1.3 Third pole approximation

For the third pole approximation, we define B_i as:

$$B_i = \frac{A_i}{A_{i+1}} - \frac{A_{i+2}}{A_{i+3}} \qquad (19)$$

From eq.(17), we obtain eq.(20),

$$B_i = (\frac{p_2}{p_1})[(\frac{k_3}{k_2})(\frac{p_2}{p_3})^{i+1}(1 - (\frac{p_2}{p_3})^2)(1 - \frac{p_2}{p_3})^2 \frac{(1 - \frac{p_1}{p_3})^2}{(1 - \frac{p_1}{p_2})^2}$$

$$+ (\frac{k_4}{k_2})(\frac{p_2}{p_4})^{i+1}(1 - (\frac{p_2}{p_4})^2)(1 - \frac{p_2}{p_4})^2 \frac{(1 - \frac{p_1}{p_4})^2}{(1 - \frac{p_1}{p_2})^2} + \ldots] \quad (20)$$

and we can derive eq.(21) in terms of eq.(20).

$$\left| \frac{B_i}{B_{i+2}} \right| = (\frac{p_3}{p_2})^2 \cdot$$

$$[\frac{1 + (\frac{k_4}{k_3})(\frac{p_3}{p_4})^{i+1} \frac{(1 - (\frac{p_2}{p_4})^2)(1 - \frac{p_2}{p_4})^2 (1 - \frac{p_1}{p_4})^2}{(1 - (\frac{p_2}{p_3})^2)(1 - \frac{p_2}{p_3})^2 (1 - \frac{p_1}{p_3})^2} + \ldots}{1 + (\frac{k_4}{k_3})(\frac{p_3}{p_4})^{i+3} \frac{(1 - (\frac{p_2}{p_4})^2)(1 - \frac{p_2}{p_4})^2 (1 - \frac{p_1}{p_4})^2}{(1 - (\frac{p_2}{p_3})^2)(1 - \frac{p_2}{p_3})^2 (1 - \frac{p_1}{p_3})^2} + \ldots}] \quad (21)$$

As i increases, eq.(21) converges to $(\frac{p3}{p2})^2$. Hence the equation for the third pole approximation is expressed as:

$$p_3 = p_2 \sqrt{\frac{B_0}{B_2}} \qquad (22)$$

A.2 Method-2: Approximation of 3 poles using 5 moments

A.2.1 First pole approximation

The equation for approximating the first pole using 5 moments is expressed in terms of eq.(13) as:

$$p_1 = \frac{m_4}{m_5} \qquad (23)$$

A.2.2 Second pole approximation

The equation for approximating the second pole using 5 moments is expressed in terms of eq.(17) as:

$$p_2 = p_1 \cdot \left| \frac{A_2}{A_3} \right| \qquad (24)$$

A.2.3 Third pole approximation

For the third pole approximation using 5 moments, we define C_i as:

$$C_i = \frac{A_i}{A_{i+1}} - \frac{A_{i+1}}{A_{i+2}} \qquad (25)$$

From eq.(17), we obtain eq.(26),

$$
\begin{aligned}
C_i &= \frac{p_2}{p_1}[(\frac{k_3}{k_2})(\frac{p_2}{p_3})^{i+1}(1-\frac{p_2}{p_3})^2 \frac{(1-\frac{p_1}{p_3})^2}{(1-\frac{p_1}{p_2})^2} \\
&+ (\frac{k_4}{k_2})(\frac{p_2}{p_4})^{i+1}(1-\frac{p_2}{p_4})^2 \frac{(1-\frac{p_1}{p_4})^2}{(1-\frac{p_1}{p_2})^2} + \ldots]
\end{aligned} \qquad (26)
$$

and we can derive eq.(27) in terms of eq.(26).

$$
\left| \frac{C_i}{C_{i+1}} \right| = (\frac{p_3}{p_2})[\frac{1 + (\frac{k_4}{k_3})(\frac{p_3}{p_4})^{i+1}\frac{(1-\frac{p_2}{p_4})^2(1-\frac{p_1}{p_4})}{(1-\frac{p_2}{p_3})^2(1-\frac{p_1}{p_3})} + \cdots}{1 + (\frac{k_4}{k_3})(\frac{p_3}{p_4})^{i+2}\frac{(1-\frac{p_2}{p_4})^2(1-\frac{p_1}{p_4})}{(1-\frac{p_2}{p_3})^2(1-\frac{p_1}{p_3})} + \cdots}]
$$
$$(27)$$

As i increases, eq.(27) converges to $\frac{p_3}{p_2}$. Hence the equation for the third pole approximation using 5 moments is expressed as:

$$p_3 = p_2 \cdot \left| \frac{C_0}{C_1} \right| \qquad (28)$$

B. Stability of the Proposed Method

For linear, finite and lumped circuits, the stability (in the sense of Lyapunov) can be analyzed by searching the poles of circuits [13,14]. For the circuit response to converge at $t = \infty$, all the poles must be on the left hand side of the *Laplace* plain, which implies that every pole has a negative real part. We show that all the poles obtained by the proposed algorithms, $Method-1$ and $Method-2$, have negative real parts intrinsically in the following:

*Proposition*1: Poles obtained by $Method-1$ and $Method-2$ are real numbers.

This proposition follows from the fact that the proposed algorithms obtain the poles through the multiplication and division of real numbers.

*Proposition*2: Poles obtained by $Method-1$ and $Method-2$ are negative numbers.

Since the moments of RC-circuit always satisfy $m_{2i} > 0, m_{2i+1} < 0 (i : 0, 1, 2, \ldots)$, the ratio of successive moments is a negative number. Hence, p_1s in eq.(14) and eq.(23) are negative numbers, and so are p_2s in eq.(18) and eq.(24), and p_3s in eq.(22) and eq.(28).

C. Algorithm for Residue Approximation

For a system with N poles, we can obtain N residues from the following equation [2]:

$$
\begin{bmatrix}
1 & 1 & \cdots & 1 \\
\frac{1}{p_1} & \frac{1}{p_2} & \cdots & \frac{1}{p_N} \\
\vdots & \vdots & \ddots & \vdots \\
\frac{1}{p_1^{N-1}} & \frac{1}{p_2^{N-1}} & \cdots & \frac{1}{p_N^{N-1}}
\end{bmatrix}
\begin{bmatrix}
k_1 \\ k_2 \\ \vdots \\ k_N
\end{bmatrix}
=
\begin{bmatrix}
m_0 \\ m_1 \\ \vdots \\ m_{N-1}
\end{bmatrix} \qquad (29)
$$

For simplicity, we transform eq.(29) to;

$$
\begin{aligned}
k_1 &= \frac{-m_2 + (D_2 + D_3) \cdot m_1 - D_2 D_3 \cdot m_0}{D_1(D_3 - D_1)(D_1 - D_2)} \\
k_2 &= \frac{-m_2 + (D_3 + D_1) \cdot m_1 - D_3 D_1 \cdot m_0}{D_2(D_1 - D_2)(D_2 - D_3)} \\
k_3 &= \frac{-m_2 + (D_1 + D_2) \cdot m_1 - D_1 D_2 \cdot m_0}{D_3(D_2 - D_3)(D_3 - D_1)}
\end{aligned}
$$
$$(30)$$

where $D_i = \frac{1}{p_i}$. Hence we can calculate residues algebraically using eq.(30).

D. Delay Time Estimation

In terms of the poles and residues, the output waveform at a circuit node can be approximated as:

$$h(t) = k_1 e^{p_1 t} + k_2 e^{p_2 t} + k_3 e^{p_3 t} \qquad (31)$$

By the definition of the delay time, which is the time between 50% points of input and output waveforms, the delay time of the step input, t_D, is calculated from the following equation:

$$k_1 e^{p_1 t_D} + k_2 e^{p_2 t_D} + k_3 e^{p_3 t_D} = 0.5 V_{out} \qquad (32)$$

IV. EXPERIMENTAL RESULTS

In this section, we present the experimental results to verify the accuracy and efficiency of the proposed method. We simulated practical RC tree circuits having different number of nodes, from 100 to 1000. The simulation was performed on $SUN\ UltraSparc - V$ workstation. The contents of following table-1 are the delay times for each circuit at the fan-out nodes. From the table-1, we know that the proposed analytic algorithms guarantee allowable error tolerance when compared to the results obtained from AWE and HSPICE.

Evaluation time comparison is shown in table-2 and table-3. As shown in table-2 and table-3, the proposed

# of nodes	HSPICE	AWE	Method-1	Method-2
100	1.2128e-11	1.2333e-11(1.69)	1.2333e-11(1.69)	1.2333e-11(1.69)
200	5.0442e-11	5.0567e-11(0.25)	5.0568e-11(0.25)	5.0567e-11(0.25)
300	1.0634e-10	1.0634e-10(0)	1.0634e-10(0)	1.0634e-10(0)
400	1.8282e-10	1.8171e-10(-0.61)	1.8171e-10(-0.61)	1.8172e-10(-0.60)
500	2.7434e-10	2.7373e-10(-0.22)	2.7374e-10(-0.22)	2.7375e-10(-0.22)
600	3.7438e-10	3.7502e-10(0.17)	3.7504e-10(0.18)	3.7506e-10(0.18)
700	4.9196e-10	4.8804e-10(-0.8)	4.8807e-10(-0.79)	4.8812e-10(-0.78)
800	6.2669e-10	6.2076e-10(-0.95)	6.2159e-10(-0.81)	6.2253e-10(-0.66)
900	7.7612e-10	7.6538e-10(-1.38)	7.5458e-10(-2.78)	7.5512e-10(-2.71)
1000	9.2790e-10	9.0804e-10(-2.14)	9.0793e-10(-2.15)	9.0822e-10(-2.12)

TABLE II
CALCULATION TIMES OF 3 POLES(AVERAGED OVER 10
EXPERIMENTS, UNIT:MS)
(SPEED RATIOS COMPARED TO THE EXISTING AWE METHOD ARE
INDICATED IN PARENTHESES)

AWE	Method-1	Method-2
1.8551(1)	0.0221(88)	0.008(232)

TABLE III
CALCULATION TIMES OF 3 RESIDUES(AVERAGED OVER 10
EXPERIMENTS, UNIT:MS)
(SPEED RATIOS COMPARED TO THE EXISTING AWE METHOD ARE
INDICATED IN PARENTHESES)

AWE	Method-1	Method-2
0.2702(1)	0.0063(43)	0.0086(31)

methods are faster than AWE, the speed-up of which is of 2-3 orders for evaluating the poles and of 2 orders for evaluating the residues. The reason that $Method - 1$ requires longer evaluation time for pole computation than $Method - 2$ is that $Method - 1$ handles more number of moments than $Method - 2$. In case of computing residues, both proposed methods yield about the same speed-up compared to the AWE results.

V. CONCLUSION

In this paper, we presented an analytic algorithm to compute the poles and residues of on-chip RC circuits, which not only overcomes numerical sensitivity and instability problems of moment matching methods, but requires less evaluation time than AWE. Although the proposed method is restricted to the 3rd order approximation, which yields good results for most practical RC circuits, it is easy to expand the equations to higher order ones due to its regularity when technology compels.

As the order of equation increases, the proposed method will guarantee allowable error tolerances compared to the results obtained from AWE and the evaluation time will shrink superlinearly compared to AWE. Hence the proposed method is expected to improve the performance in electrical and physical design such as placement & routing which requires iterations of delay time calculation.

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