Circuit Performance Oriented Device Optimization using BSIM3 Pre-Silicon Model Parameters

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Abstract

We propose a circuit performance oriented device optimization methodology using pre-silicon parameters and critical paths which represent the performance of the chip. Based on our methodology, we successfully reduced the power consumption by 90% and, at the same time, increased the frequency by 30% from the initial design. The key to this optimization methodology is the pre-silicon parameter generation method, which can predict the device performance within 5% accuracy in a few minutes.

1. Introduction

In the deep sub-micron regime, it is becoming very difficult to fabricate new products, within a short term, which satisfies the target specification. The appropriate power supply voltage and threshold voltages should be determined based on the application of the product, i.e. low power or high speed [1]. The device structure should be also optimized based on the targets of the product. For example, reducing the oxide thickness improves Ids, but does not always improve the speed and only increases the power consumption [2][3]. It is therefore imperative to optimize the device specifications including the structures of interconnects before circuit design. For circuit performance oriented device optimization, we need several sets of accurate device model parameters of the next generation (pre-silicon parameters).

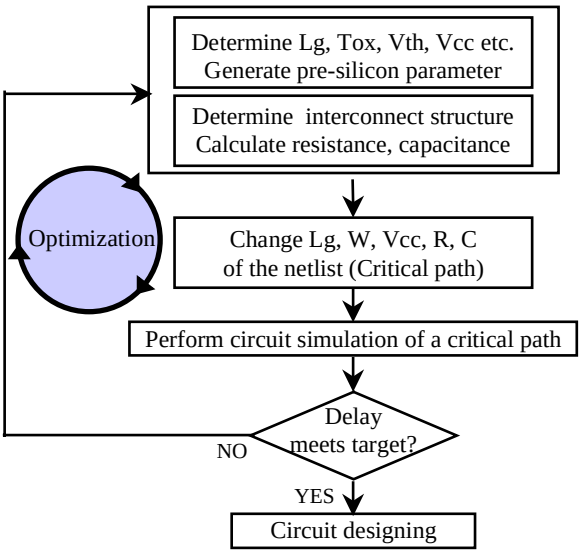


Fig. 1. Circuit performance oriented device optimizing flow using pre-silicon parameters.

We have proposed an accurate pre-silicon parameter generation methodology using BSIM3 [4], which uses "a physical extraction method" to make the model predictable and accurate enough to optimize the device performance of a specific device structure. The key to the physical extraction of the base parameter is to divide the parameters in "hierarchical groups" and then extract the parameters based on each physical phenomena described by BSIM3. The pre-silicon parameters can predict the device performance within about 5% accuracy in a few minutes.

In this paper, we propose the circuit performance oriented device optimization methodology using the pre-silicon parameters and the critical paths which represents the performance of the chip to determine an appropriate device condition, as shown in Fig. 1. In Section 2, we will briefly describe the method to generate pre-silicon parameters of a new technology from base-parameters of a current technology. In Section 3, we will show the accuracy of our methodology. In Sections 4 and 5, we will give an example of the circuit performance oriented device optimization.

2. Pre-Silicon Parameter Generation Methodology

DC parameter generation method

Using the physically extracted base parameters of an existing device [4], the pre-silicon parameters for the process of the next generation are generated by changing some process parameters and leaving other parameters as is (Fig.2). The details are as follows,

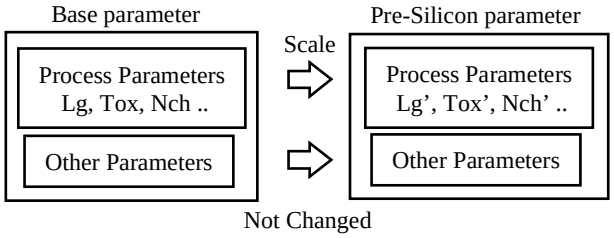


Fig. 2. DC pre-silicon parameter generation.

(1) Set channel length and Tox to the target value.
(2) Determine Nch so that the threshold voltage meets the target value.
(3) Determine Nsub and Xt so that the body effect meets the target value.
(4) Determine the doping concentration and the length of the pocket to adjust the Vth-lowering.
(5) Calculate several parameters using the analytical equations described in the BSIM3 manual.
(6) Leave other parameters as is.

AC parameter generation method

AC parameters for the pre-silicon parameters are calculated as follows, assuming that constant electric field scaling is done.

(1) Bottom side diffusion capacitance: The value of the capacitance is multiplied by the factor of root K, where K is 0.25/0.20 when generating the parameters for the 0.20μm process device from that of a 0.25μm process device.
(2) Side wall diffusion capacitance: Not changed.
(3) Fringing capacitance: Recalculated using the fringing capacitance model.
(4) Overlap capacitance: The width of the overlap (Parameter DLC) is scaled by the factor of 1/K.

3. Accuracy of the Pre-silicon Parameters

Here we show the accuracy of the pre-silicon parameters. The device conditions of the base parameters and for the pre-silicon parameters are listed on Table1.

Fig. 3 shows the prediction results of drain saturation current versus the threshold voltage plots of 0.20μm process MOSFETs. The dots were obtained by measurement of 10 wafers which were fabricated to have different threshold voltages, and the line is from simulations using the pre-silicon parameters which were generated from a base parameter set of a 0.25μm device. The simulation results show very good agreement with accuracy within 5%.

Fig.4 shows the waveform of the Vds-Ids and Fig.5 shows the Vgs-Ids characteristic. The waveforms obtained by simulation using pre-silicon parameters are quite similar to the ones obtained from measurement

Fig. 6 shows the accuracy of the AC factors by comparing with the measured delay of ring oscillators consisting of inverters and NAND gates, which have fan-outs of 1 and 3. Again good agreement with accuracy of around 5% is shown.

TABLE 1
DEVICE CONDITION OF THE BASE AND PRE-SILICON PARAMETER

	Base Parameter	Pre-Silicon Parameter
Lg	0.25 μm	0.20 μm
Tox	5.2 nm	4.5 nm
Vth	0.4 V	0.5 V
Vcc	1.8 V	1.8 V

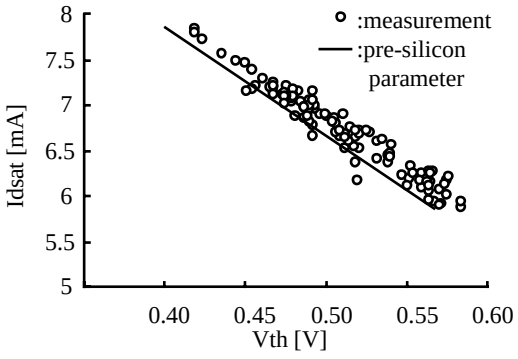


Fig. 3. Drain saturation current versus threshold voltage of measured and predicted MOSFET. (L=0.20μm, W=15μm, Vds=Vgs=1.8V)

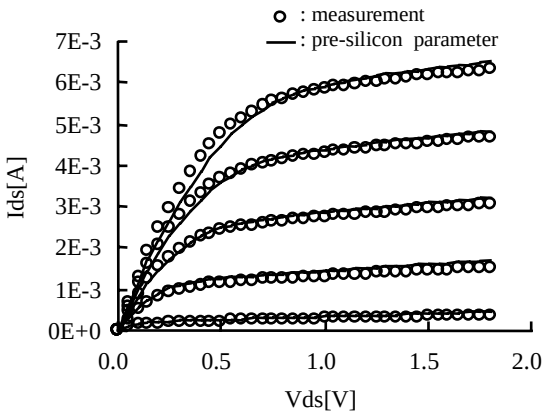


Fig. 4. Ids-Vds curve of a measured and predicted MOSFET. (L=0.20μm, W=15μm)

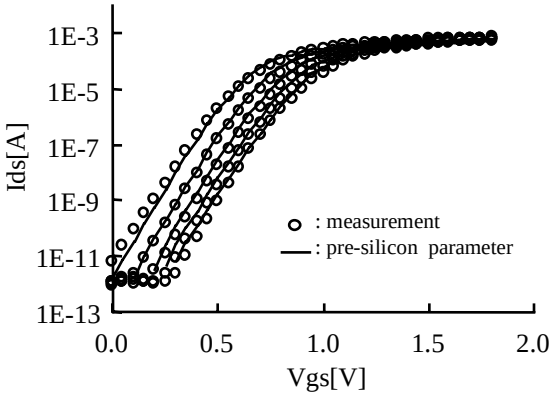


Fig. 5. Ids-Vgs curve of a measured and predicted MOSFET. (L=0.20μm, W=15μm, Vds=0.05V)

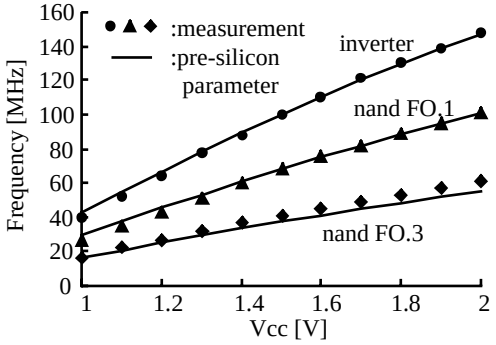


Fig. 6. Frequency of ring oscillators from measurement and simulation using pre-silicon parameters. (L=0.20μm)

Another advantage of pre-silicon parameters is that the parameters can be created in a short time. For instance, sets of pre-silicon parameter with 10 different device conditions can be created in just one hour, thus making it possible to use for the purpose of device optimization.

4. Sensitivity simulation using Pre-silicon Parameters

Before performing device optimization, we perform sensitivity analysis to create base data for the circuit performance oriented device optimization. We generate many sets of pre-silicon parameters, changing conditions

of the device including threshold voltage, oxide thickness, power supply voltage, etc. Then we perform circuit simulation using some critical path to see how each device condition influences the delay.

The simulations were done using two benchmark circuits of a microprocessor, one for the critical path of the CPU block, and another for the critical path of the BUS interface block, both of which directly indicate the performance of the chip. Here, we show some examples of the analysis that we have performed.

Oxide thickness dependency

Fig. 7 shows the relationship between oxide thickness and the delay of the critical path of the CPU block, with different power supply voltages. The results show that the change in oxide thickness does not make a big difference in speed, and it shows that there is an optimum point, which has already been demonstrated by K. Chen et. al [3] using a ring oscillator. We have shown that this is also true for critical paths.

Threshold Voltage Dependency

Fig.8 shows the relationship between threshold voltage and delay. This results show that the threshold voltage variations, influences the delay more when the power supply voltage is lower.

Fig. 9 shows the relationship between the threshold voltage and the power consumption of the leakage current. From these results, we can determine the appropriate threshold voltage and power supply voltage, which meets the specification in both speed and standby power consumption.

Cell Height Dependency

Fig. 10 shows the relation between cell height and delay, with normal and thin metal interconnect structures of the two critical paths. The capacitance of interconnect were calculated using Raphael ™. The results show that in the CPU path, the thin metal structure shows better performance in speed, while the opposite is true in the high cell height regime of the bus controller path. This difference occurs because the delay of the bus controller path is dominated by the interconnect delay, where the delay of the CPU path is dominated by the gate delay.

Saturation Current Dependency

Fig. 11 shows the relationship between the drain saturation current of a NMOS and the delay of a critical path, with different device conditions. The results show that even if the saturation current is the same, the delay differs because of the difference in gate capacitance or the difference in the linear region characteristics of the I-V curve. This also shows that it is better to reduce threshold voltage to decrease the delay, rather than reducing the parasitic resistance or the oxide thickness.

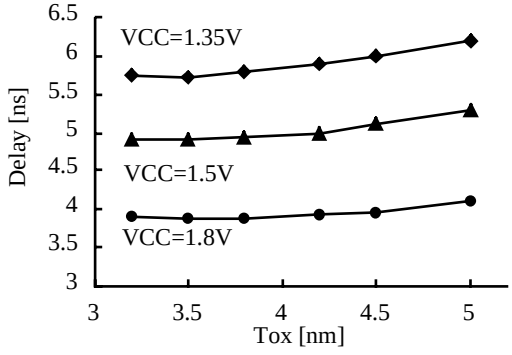


Fig. 7. Oxide thickness dependency of path delay.

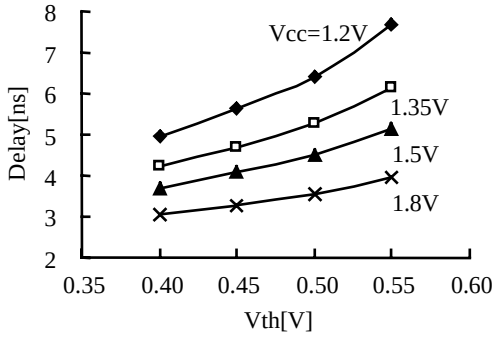


Fig.8. Threshold voltage dependency of path delay.

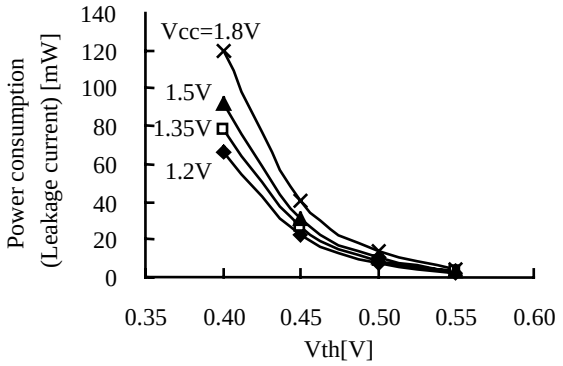
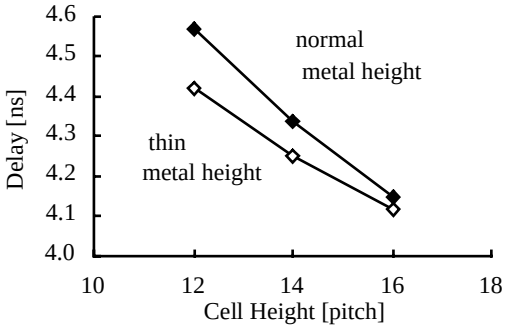
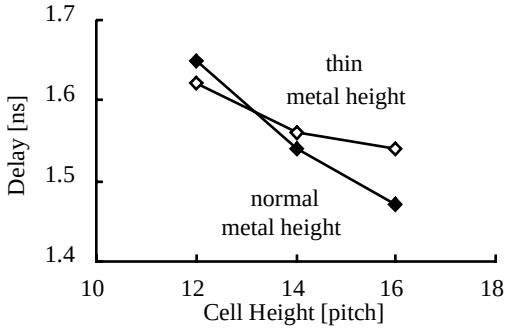


Fig.9. Threshold voltage dependency of power consumption of the leakage current.



(a) CPU path



(b) Bus controller path.

Fig. 10. Cell height and metal thickness dependency of critical path delay.

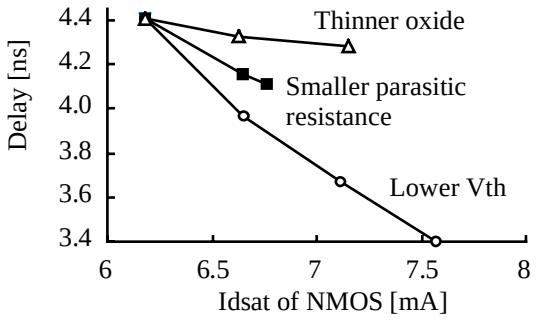


Fig. 11. Relationship between saturation current and critical path delay under different device conditions.

By performing the sensitivity analysis described above, we can see how the device condition influences the speed and power, and we can perform device optimization by combining the conditions.

5. Circuit Performance Oriented Device Optimization

The pre-silicon parameters have been used in designing our products to decide the optimum device condition that meets the speed and power consumption goals of the chip. The circuit performance oriented device optimization is performed, using the results obtained from the sensitivity analysis, which is described in the previous section. Fig.12 shows an example of device optimization. The initial point is the performance of the previous product. The target of the next product was to reduce the power consumption to 12%, and to increase the frequency to 133%. Starting from the initial point, we first did device shrinking. This shrink was done assuming constant electric field scaling. At this time, it was still far from the target in terms of the power consumption. So we reduced the height of the cell, power supply voltage, and increased the oxide thickness to make the power suit the specification. And finally, we lowered the threshold voltage so that the frequency met the target.

Using this circuit performance oriented device optimization method, we were able to reduce the power to 12% and at the same time, increase the frequency to 133%.

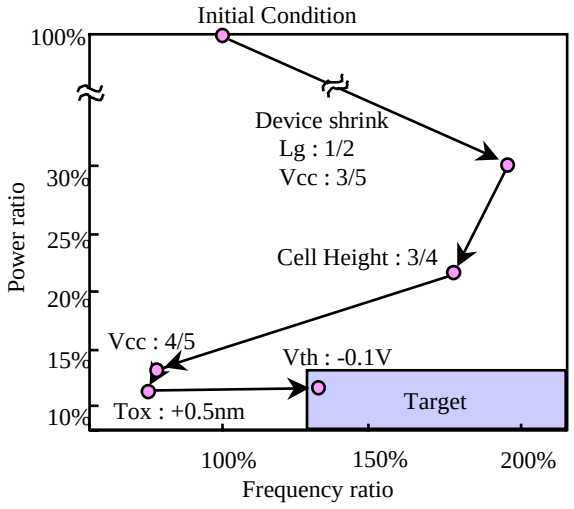


Fig. 12. Example of device optimization.

TABLE 2
RESULT OF DEVICE OPTIMIZATION

	Initial value	After optimization
Power consumption	100%	12%
Frequency	100%	133%

6. Conclusion

We propose a circuit performance oriented device optimization methodology using pre-silicon parameters and the critical paths which represent the performance of the chip. Based on our methodology, we successfully reduce the power consumption by 90% and, increase the frequency by 30% from the initial design. The key of this optimization methodology is the pre-silicon parameter generation method, which can predict the device performance with 5% accuracy in a few minutes.

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