Taiwan Foundry for System-In-Package (SIP)

Albert W. Lin

APack Technologies Inc.
Hsinchu, Taiwan, ROC
Tel: 886-3-578-8766
Fax: 886-3-563-2129
E-mail: Alin@apack.com.tw

Abstract -- System-In-Package (SIP) is a cost-effective alternative to System-On-Chip (SOC) and chips with embedded memory. The key elements of SIP technology include I/O redistribution, solder bumping, flip chip assembly, and high density thin film interconnect substrate with/without integrated passives. To meet the need of SIP, as well as other advanced packaging solutions, APack Technologies has been set up to serve worldwide customers. High quality of the APack's service is built upon the SIP technology licensed from Bell Labs of Lucent Technologies, and the experience of cost competitive wafer fabrication of foundries in Taiwan.

I. Introduction

To achieve System-On-Chip (SOC) performance has been the ultimate goal of IC designers. Recently, personal computers and related components are beginning to be manufactured using SOC. However, it is soon realized that the SOC approach does not provide cost savings as expected, and even may not be "the best solution." For example, graphic processors integrated with DRAM for high performance 3D applications, or other logic chips with embedded memories, demand compromising in terms of chip design, mask level, wafer processing, chip size, yield and testing. This is especially true when the price of DRAM reaches bottom of market. It is not economically wise to integrate different function blocks with large price differential on one piece of silicon real estate.

As more devices are packed in BGA (ball grid array) packages to meet the challenge of high pin count and to improve SMT (surface mount technology) assembly yield at board level, an evolution of micro BGA or Chip Scale Package (CSP) quickly push the microelectronic packaging to higher level of integration. Solder bumping technology is the key driver behind all these advancement of integration. When wafer bumping service becomes available recently, Wafer Level Packaging (WLP) is gaining a lot of attention. This ultimate form of IC device packaging can be realized now. Suddenly packaging becomes an extension of wafer process.

With flip chip assembly, it is very easy to integrate solder-bumped chips into a compact size. In fact, the short interconnect distance (about 50 μm) along with low inductance (ca. 0.1 nH) provided by the solder joints results in better signal propagation than any other means. The flip chip assembly can be carried out on wafer level. A combination of wafer level bumping and assembly is the foundation of SIP technology. This packaging solution offers a very attractive alternative to SOC in terms of cost and performance. In addition, it offers a freedom of integrating very different IC technologies such as, CMOS and Bipolar, or even Si and GaAs devices.

In this paper, we will introduce APack Technologies, an advanced packaging foundry that offers a complete manufacturing technology of wafer level packaging and assembly to meet the need of system integration. Its SIP process, design rules and reliability data will be discussed.

II. Foundry Setup

Solder bumping technology was first developed and applied onto large computer system in early 70's by IBM. However, its C4 (controlled collapse chip carrier) technology using evaporation to form solder bumps had been captive for internal use until recently. Many other bumping technologies, such as plating, printing, dispensing, ball placement, etc. have been developed.

In view of increasing market demand and unavailability of solder bumping and flip chip assembly, APack Technologies was set up in October 1996 to provide manufacturing service of wafer level packaging. A complete set of technologies, including low cost solder bumping by printing lead-free solder paste, were transferred from Bell Labs of Lucent Technologies.

III. SIP Process and Design Rules

The key elements of APack SIP Technology are I/O Redistribution, Solder Bumping, and Flip Chip Assembly. All of the processes are conducted at wafer level. Before the SIP processing is started, all wafers should be functionally tested, and the test results in wafer map format should be received. Bad chips on the wafers can be marked with

special ink. Preferably, wafers should have a minimum thickness of 508 μm (20 mils) with little or no backside thinning.

Wafers of the chips to be mounted on another chip or Si substrate are processed for redistribution of I/O pads first. If the chips need to be burn-in tested before assembly or tall solder joints are required, the wafers are solder bumped using a printing method, then are diced into individual chips.

Once the wafers are diced, good chips can be picked and then placed on a wafer of another chip or a Si interconnect substrate (called Base Wafer) for flip chip assembly. After assembly, these chips can be tested to confirm their functionality. Once the base wafer is diced, the chip assemblies (called Tiles) can be picked and placed in a conventional package such as a PQFP or a BGA using wire bonding. APack also offers the Tiles in advanced packages such as flip chip BGA and Chip Size Module (CSM) using solder assembly instead of wire bonding.

The SIP process flow is illustrated in Figure.1 and Figure.2.

A. Key Materials

Polyimide is used as inter-level dielectric material to ensure the electrical performance of the integrated devices in SIP as good as their original ones in individual packages. Polyimide has been widely used as part of the passivation/encapsulation material of Si devices, and especially on DRAM chips where it also serves as a protection layer to reduce soft errors caused by alpha particles. Photosensitive polyimide is used to reduce processing steps and save cost. The polyimide needs to be processed at $350\,^{\circ}C$ 1 hour in nitrogen for a final cure. Each of the wafers may be subject to the final cure process no more than two times after receiving by APack. For the wafers with limited thermal budget, this heat treatment should be taken into consideration.

The under bump metallization (UBM) is a multilevel structure of sputtered Cr, Cr-Cu, and Cu thin films. The UBM provides an interface between the solder bump and the aluminum I/O pad. While Cr provides excellent adhesion to Al pad, Cu offers a solder wettable surface. This UBM structure ensures a strong solder joint to the chips.

Two types of solder material are available for wafer bumping, i.e. SnSb and SnPb. Their composition, melting points and reflow temperatures are given in Table.1. The SnSb solder is specially formulated for applications where a lead-free environment is required or the device performance is sensitive to alpha particle radiation such as DRAM chips.

B. Design Rules

Most of the APack SIP design rules are dictated by the limitations of manufacturing processes and materials. Table.2 lists the composition and design values of each mask level.

To enhance process yield and reliability, chip I/O pads are redistributed to form an area array of solder-wettable pads. The I/O rerouting paths normally avoid crossing over performance-sensitive areas in the chip. However, preliminary data indicate that the rerouting paths over laser repair windows and memory cells do not degrade the performance of 100 MHz SDRAM devices. Details of the I/O redistribution design rules are illustrated in Table.3 and Figure.3.

It is preferred to redistribute chip I/O pads in order to enhance flip chip assembly yield and reliability. However, I/O redistribution may be omitted to save two processing steps and cost, when the pitch of original I/O pads is adequate for solder bumping (with a minimum pitch of 150 μm). For ultra high-speed devices such as RF chips, extra parasitic from the rerouting path should be minimized. In this case, solder wettable UBM pads and solder are deposited directly on the original I/O pads. The design rules for undistributed I/O pads are illustrated in Table.4 and Figure.4.

IV. Production Capability

APack has set up a class 100 clean room facility to process 8-inch (200 mm) Si wafers. The capacity is expandable to 50,000 wafers per month. Preferably the device wafers to be processed at APack facility should not to be thinned using back grinding. The acceptable minimum wafer thickness is 508 μm (20 mils). Wafers with a diameter less than 8-inch, as well as the integration of passives on Si substrate, can be processed in our Phase II facility which is scheduled to be set up in the second half of year 2000. Wafer level flip chip assembly is conducted in a class 1000 clean room facility with a capacity of assembling more than 10 million devices per month. The SIP products can be packed as PQFP, BGA or CSP (chip size package).

V. Reliability of Solder Bumping and Flip-Chip Assembly

Reliability of solder bumping and flip chip tiles has been studied. The results of temperature cycling, thermal aging, and temperature humidity tests under various conditions show that APack's solder bumping and flip chip assembly are very robust. Some of the reliability test results are summarized below.

A. Reliability Studies of Solder Bumps

Temperature Cycling Test of Solder Bumps

5 wafers with more than 121,000 95Sn5Sb Solder Bumps (220 μm diameter and 140 μm height) were subject to temperature cycling between -55 ~ 125 $^{\circ}C$ (10 min. dwell time at each temperature extreme). All the bump's shear strength remained high after 1000 cycles as shown in Figure5 (a).

Thermal Aging Test of Solder Bumps

2 wafers with more than 48,000 95Sn5Sb Solder Bumps (220 μm diameter and 140 μm height) were thermally aged at 150 $^{\circ}C$ up to 1000 hours. The bump shear strength remain high after 1000 hours as shown in the Figure 5(b).

Chips with 63Sn37Pb eutectic solder bumps (200 μm diameter and 140 μm height) were aged at 185 $^{\circ}C$ for 1000 hours. It was impressive to find that the bumps remained to be very strong even after being exposed to a high temperature near its melting temperature for extensive time. The average shear strength of the bumps after various test time is presented in the Table 5.

In another experiment, the SnPb eutectic bumps were put on a hot plate at 250 $^{\circ}C$ under melting condition for 100 minutes. The bumps were re-solidified after cooling down to room temperature and then subject to shear test. Its averaged shear strength is 107±11 grams. Still no degradation of bump shear strength was observed.

The robustness of UBM was also demonstrated by successful multiple reflows of 95Sn5Sb solder bumps (200 μm diameter and 140 μm height). The peak heating condition was 260 $^{\circ}C$, 2 min. The shear strength of the lead-free solder bumps remained high after 10 times of reflows are 168 ± 18 grams for 1 reflow, 171 ± 20 grams for 5 reflows, 168 ± 20 grams for 10 reflows, respectively.

Temperature Humidity Test of Solder Bumps

48 chips with a total of 7488 95Sn5Sb Solder Bumps (350 μm diameter and 109 μm height) were accelerated aged in a steam bomb under the following test condition 135 $^{\circ}C$, 85 %RH, 2.7 atm. The solder bumps survived through such harsh condition and their shear strength remained high after the test.

B. Reliability Studies of Flip-Chip Tiles

Flip Chip Tile as shown in Figure.7 was used for reliability studies. Two chips were assembled on each tile to form a daisy chain of 96 solder joints. Since there is a good match of CTE (coefficient of thermal expansion) between the chips and the Si substrate, no underfill was used on the tile. The results of temperature cycling, thermal aging and temperature humidity tests are summarized below.

Temperature Cycling Test of Flip Chip Tiles

48 Tiles with a total of 96 chips were assembled using 95Sn5Sb solder. A total of 4608 solder joints (each with 350 μm diameter and 75 μm height) were subject to temperature cycling test between -40 and 125 $^{\circ}C$ (15 min. dwell time at each temperature extreme). All samples passed the test. The test results are summarized in Table.6.

Thermal Aging Test of Flip Chip Tiles

48 Tiles with a total of 96 chips and 4608 solder joints (95Sn5Sb solder joints with 350 μm diameter and 75 μm height) were aged at 150 $^{\circ}C$ for 1000 hours. All the samples passed the test and their results are shown in Table.7.

Temperature Humidity Test of Flip Chip Tiles

Similar to the previous two tests, 48 Tiles with a total of 96 chips and 4608 solder joints (95Sn5Sb solder with 350 μm diameter and 75 μm height) were accelerated aged in a steam bomb under 135 $^{\circ}C$, 85 %RH and 2.7 atm up to 168 hours. All the samples passed the harsh test and the shear strength of solder joints remained high after the test. The test results are summarized below in Table.8.

VI. Summary

APack's SIP technology provides a cost-effective alternative to System-On-Chip (SOC) and chips with embedded memory. The process flow and the design rules of the SIP technology have been presented. Various preliminary reliability test results of solder bumps and flip chip tiles have shown that the SIP technology is robust. The reliability of complete SIP, such as in the format of PQFP, BGA or CSM, is yet to be demonstrated on real products.

References

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Solder Materials	95%Sn 5%Sb	63%Sn 37%Pb
Melting Temperature	232 ~ 240 $°C$	183 $°C$
Reflow Temperature	260 $°C$	210 $°C$

Table 1. Comparison of solder materials

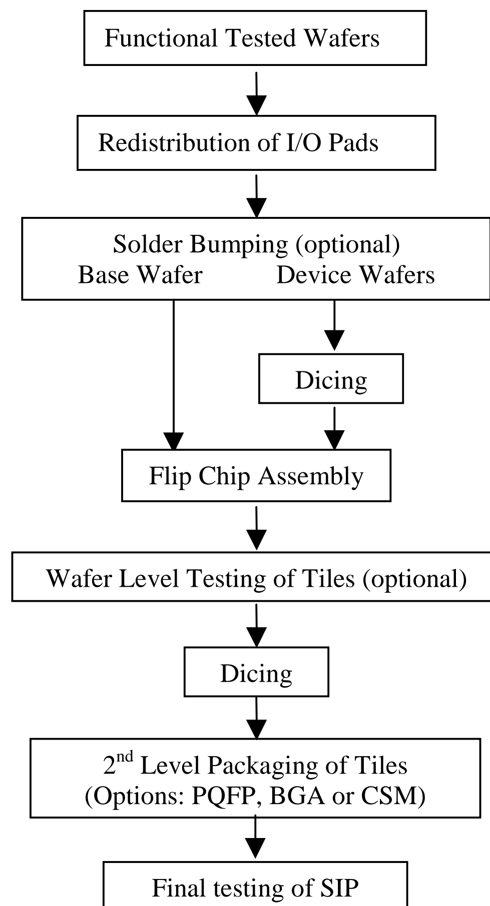
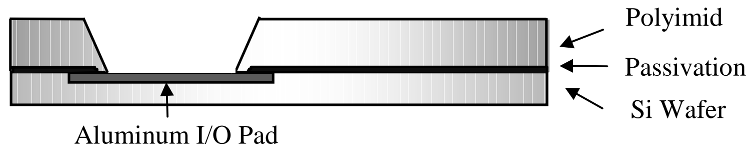
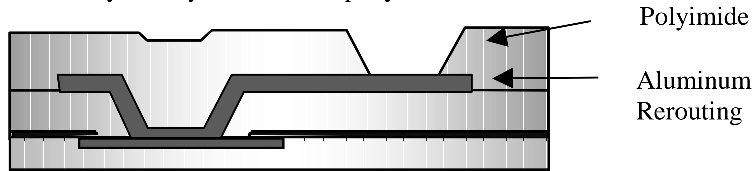


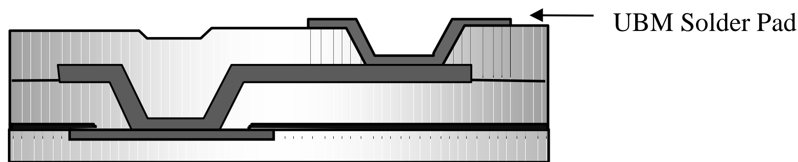
Figure.1 SIP process flow



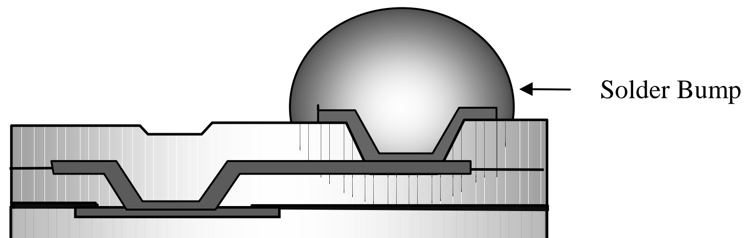
a) Step 1 of I/O redistribution: As-received wafers may or may not have a top layer of



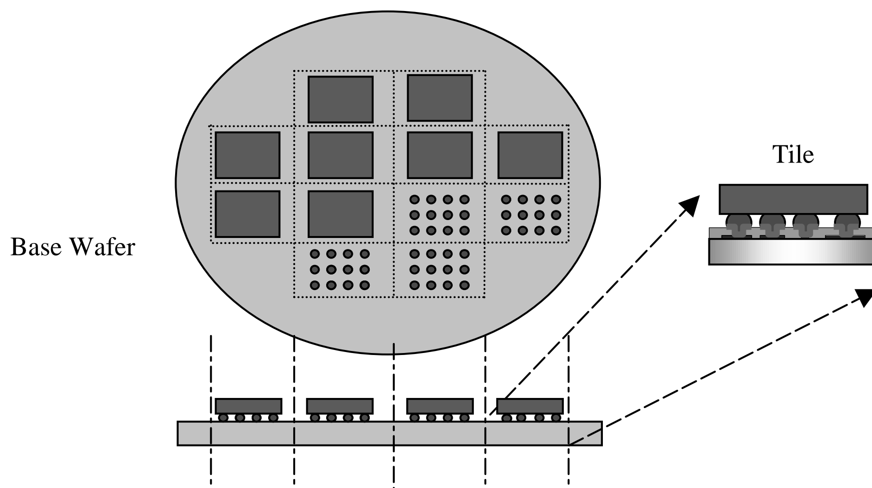
b) Step 2 of I/O redistribution: Aluminum I/O pads are rerouted and an additional polyimide layer is spin-coated and patterned.



c) Step 3 of I/O redistribution: Under Bump Metallization (UBM) is sputtered and patterned.



d) Solder Bumping: Solder bumps are formed on UBM using wafer-level printing and reflow processes.



e) Wafer Level Flip Chip Assembly: Good chips are picked from device wafers according to their test results (as presented in wafer maps) and then flip assembled on the substrate using flip chip bonding and reflow processes.

Figure.2 Key process steps of SIP

Mask Levels	Materials	Typical Thickness	Minimum Feature Size	Preferred Feature Size
D1	polyimide	3 µm	15 µm	40µm
M1	aluminum	2 µm	20 µm	35 µm
D2	polyimide	3 µm	15 µm	50 µm
UBM	Cr/CrCu/Cu	1K Å/3K Å/6K Å	100 µm	150 µm
Solder	SnSb or SnPb	200 µm	75 µm	400 µm

Table 2. Composition and design values of each mask level

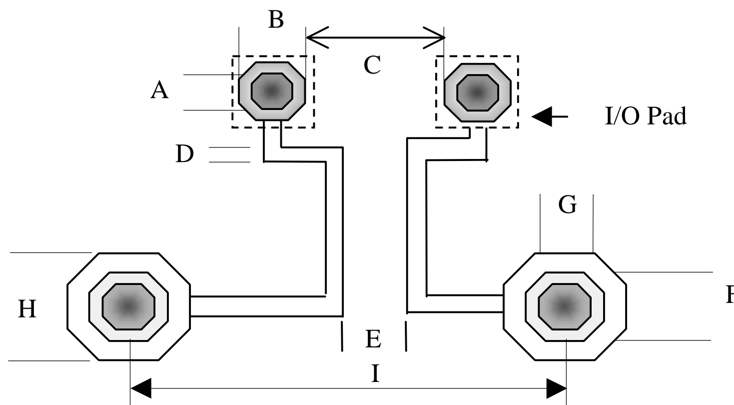


Figure3. I/O redistribution design rules

Items	Description	Mask Level	Minimum Dimension	Preferred Dimension
A	Via diameter of AL I/O pad	D1	25 µm	40 µm*
B	AL I/O via capture pad	M1	50 µm	80 µm
C	Separation of AL I/O via capture pads	M1	20 µm	50 µm
D	Linewidth of AL rerouting path	M1	20 µm	35 µm*
E	Separation of AL rerouting paths	M1	20 µm	35 µm
F	AL pad (solder via capture pad)	M1	80 µm	100 µm
G	Via diameter of UBM solder pad	D2	60 µm	80 µm*
H	Diameter of UBM solder pad	UBM	100 µm	150 µm
I	Pitch of UBM solder pads (center-to-center spacing)	UBM	350 µm	>400 µm

* This dimension may vary depending on resistance requirement.

Table 3. I/O redistribution design rules

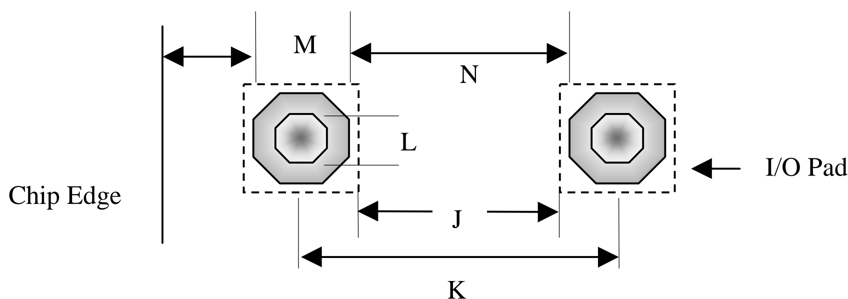


Figure4. Design rules for undistributed I/O

Items	Description	Mask Level	Minimum Dimension	Preferred Dimension
J	Separation of AL I/O pads (original wire bonding pad on IC)	-	50 µm	100 µm
K	Pitch of AL I/O Pads	-	150 µm	350 µm
L	Via diameter of AL I/O pad	D1	25 µm	40 µm*
M	Diameter of UBM solder pad	UBM	75 µm	100 µm
N	Separation of UBM solder pads	UBM	75 µm	100 µm
O	Separation between UBM solder pad edge and chip edge	UBM	75 µm	100 µm#

* This dimension may vary with resistance requirement.
# This dimension may vary with next level assembly process.

Table 4. Design rules for undistributed I/O

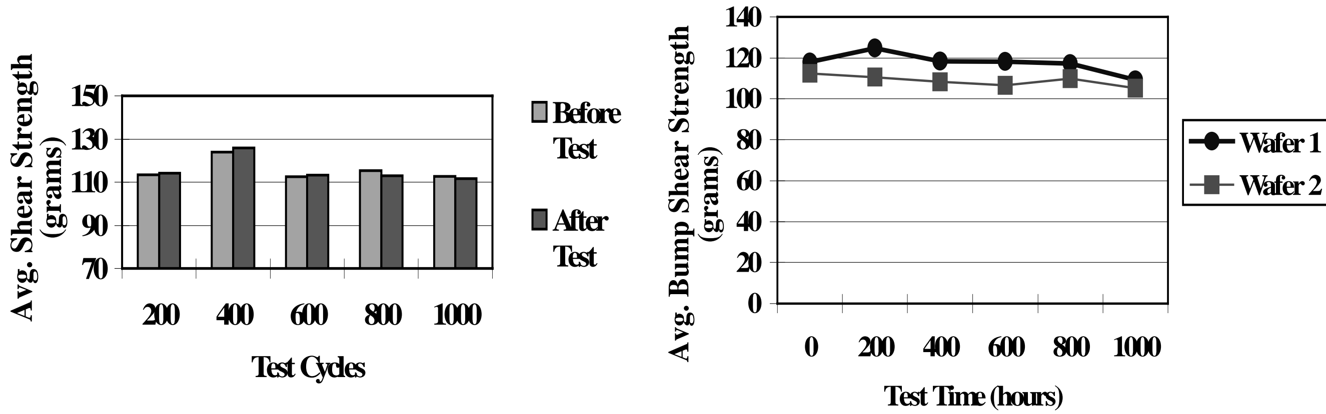


Figure 5. (a) Temperature aging test of solder bumps. (b) Thermal aging test of solder bumps

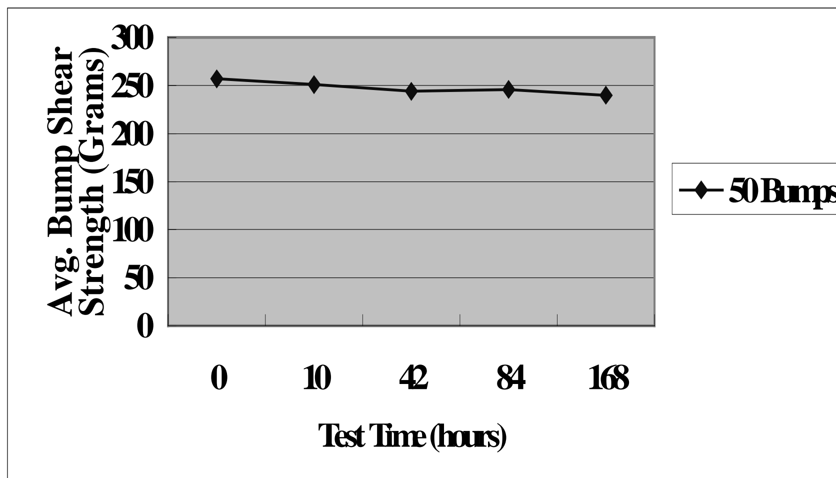


Figure 6. Temperature humidity test of solder bumps

Test Time (hours)	0	100	500	1000
Avg. Shear Strength of 50 Bumps (grams)	109±10	107±11	106±10	100±11

Table 5. Average shear strength of the bumps after various testing time at 185 $^{\circ}C$.

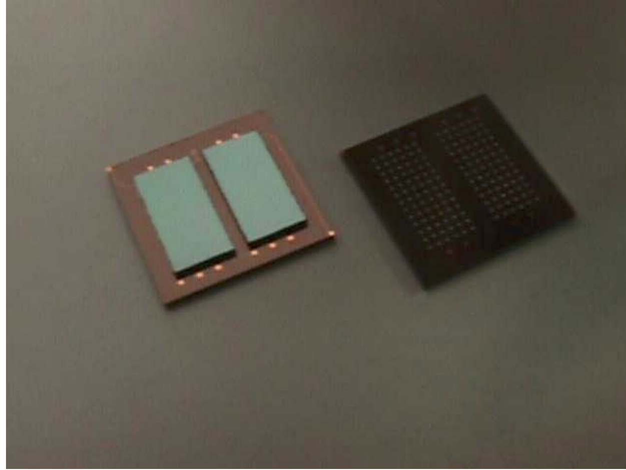


Figure 7. Flip-chip testing tile

Test Cycles	0	100	250	500	1000
Failed Chips/Tested Chips Failed Joints/Tested Joints	0/96 0/4608	0/96 0/4608	0/84 0/4032	0/72 0/3456	0/60 0/2880
Avg. Shear Strength of 12 chips (3x16 bumps per chip)	25±4 Kg	19±3 Kg	20±2 Kg	19±2 Kg	18±3 Kg

Table 6. Temperature cycling test of flip-chip tiles

Test Time (hours)	0	24	120	216	504	768	1008
Failed Chips/Tested Chips Failed Joints/Tested Joints	0/96 0/4608	0/96 0/4608	0/96 0/4608	0/84 0/4032	0/72 0/3456	0/60 0/2880	0/48 0/2304
Avg. Shear Strength of 12 chips (3x16 bumps per chip)	25±4 Kg	-	16±2 Kg	15±3 Kg	13±1 Kg	13±2 Kg	12±2 Kg

Table 7. Thermal aging test of flip-chip tiles

Test Time (hours)	0	10	42	84	168
Failed Chips/Tested Chips Failed Joints/Tested Joints	0/96 0/4608	0/96 0/4608	0/96 0/4608	0/84 0/4032	0/72 0/3456
Avg. Shear Strength of 12 chips (3x16 bumps per chip)	25±4 Kg	-	16±3 Kg	16±3 Kg	12±2 Kg

Table 8. Temperature humidity test of flip-chip tiles