An 8 x 8-b nRERL Serial Multiplier for ultra-low-power applications

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Abstract— An 8 x 8-b nRERL serial multiplier is implemented in a 0.6-μm n-well 3-metal CMOS process. nRERL (nMOS Reversible Energy Recovery Logic) is a new reversible adiabatic logic circuit, which can be operated at the leakage-current level for ultra-low-energy applications. Measurement results showed that the nRERL serial multiplier consumed only 0.9 % of the energy dissipation of the static CMOS one at the operating frequency 100 kHz at 5V, where its adiabatic and leakage losses were about equal.

I. Introduction

RERL (Reversible Energy Recovery Logic) [1][2] is a fully adiabatic logic that uses transmission gates and 8-phase clocked power. nRERL is an improved version of RERL, which reduced both the energy consumption and area overhead substantially by using only nMOS transistors and 6-phase clocked power [3]. It eliminates the non-adiabatic loss by using reversible logic. Therefore, it can be operated at the leakage-current level and has substantial advantage in the energy consumption compared with any other logic circuits at the low-operating frequencies.

II. nRERL and Its Clocked Power Generator

An nRERL buffer is shown in Fig. 1, as well as its 6-phase clock and its reversible pipeline connection. The bootstrapped switches M1 and M2 (M3 and M4) compose a forward (backward) logic function, which determines a charging (discharging) path to one of the output nodes. The nMOS switches M5 and M6 (M7 and M8) are forward (backward) isolation switches, which isolate charging (discharging) paths from the outputs. The clamp transistors M9 and M10 make an undriven output node grounded. Because there is no abrupt voltage drop in the nRERL circuit, any non-adiabatic loss does not occur. The rising ϕ_1 supplies the energy to X_1, whereas the falling ϕ_3 recovers the energy of X_1 [3].

We can generate the 6-phase clocked power with a small control logic circuit and an off-chip inductor, which is similar to the 8-phase CPG (clocked power generator) proposed in [1][2].

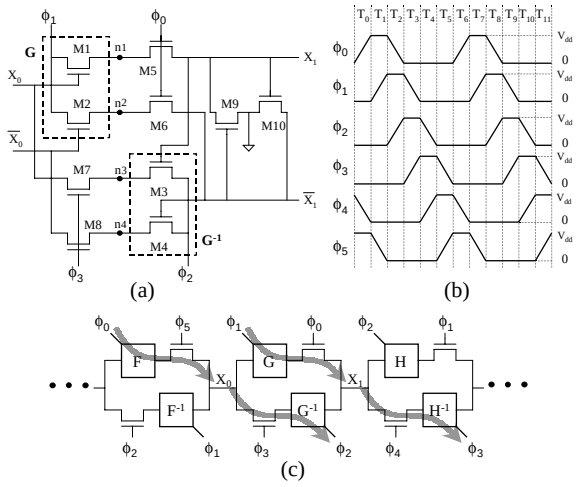

Fig. 1. nRERL: (a) a buffer (b) its 6-phase clocked power, and (c) pipeline connection and energy-flow. F, G, and H are forward functions of each logic stage, and F^{-1}, G^{-1} and H^{-1} are their backward functions, respectively.

III. Bit Serial Multiplier

Genarally a fully reversible logic has large overhead to maintain reversibility. We can reduce this overhead by using nRERL's inherent pipeline property with 6-phase clocks. After modifying the serial multiplier in [4], we applied it to nRERL for an 8 x 8-b serial multiplier.

For simplicity we present a 4 x 4-b serial multiplier block diagram in Fig. 2. It consists of delay cells, AND gates, full adders and control switches. The control switches sample inputs into the delay cell at each cycle in Fig. 2. A delay cell is a flipflop in the static CMOS circuit and a buffer-chain in nRERL. Two inputs (X, Y) are serialized from the LSB bit to the MSB bit. The lower three output bits (S0 - S2), are generated separately at their corresponding terminals. S3, S4, S5 and S6 are generated sequentially at the node Z every four cycles. An 8 x 8-b multiplier is its simple extension.

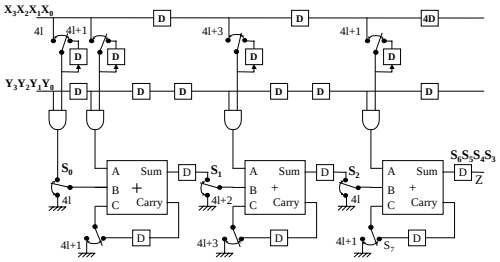

Fig. 2. Block diagram of 4 x 4-b serial multiplier.

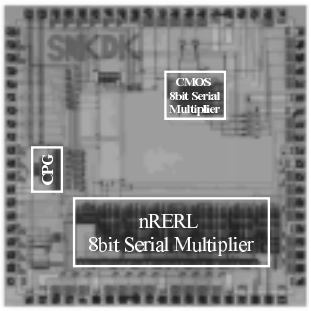

Fig. 3. Photomicrograph of the test chip.

IV. Measurement Results

A test chip with an nRERL 8 x 8-b serial multiplier and its CPG was implemented. A static CMOS multiplier with the same architecture was also included in the test chip for fair comparison. Fig. 3 is a photomicrograph of the test chip. The sizes of the nRERL multiplier, the CPG and the static CMOS multiplier were 2.7 x 0.88 mm^2 and 0.4 x 0.54 mm^2, 0.84 x 0.58 mm^2, respectively. The area overhead of the nRERL was approximately 5, excluding the CPG.

The energy dissipation of the nRERL multiplier, including its CPG, was compared with that of the static CMOS, as shown in Fig. 4. When V_{dd} was 5 V, the nRERL multiplier consumed only 0.9 % of the energy consumed in the static CMOS one at 100 kHz, where the adiabatic and leakage losses were about equal. However, if the operating frequency is lower than 100 kHz, the consumed energy increases because the leakage loss, which is inversely proportional to the operating frequencies, becomes dominant to the adiabatic loss, which is proportional to the operating frequencies.

The supply voltages that minimizes the energy dissipation of each circuit were 2.5 V for the nRERL and about 0.9 V (= $\mid V_{tp} \mid$) for the static CMOS. Note that 0.9 V is the theoretical lower limit of the supply voltage for the static CMOS circuit. In this case, the nRERL multiplier consumed 7 % of the energy consumed in the static CMOS one at 100kHz and less energy than static CMOS one up to 1MHz. Furthermore, the nRERL multiplier does consume more energy than the CMOS multiplier at the operating frequencies higher than 1MHz.

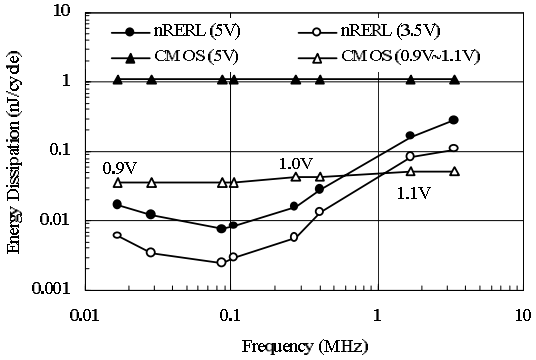

Fig. 4. Measured energy consumption of nRERL and static CMOS 8-b serial multipliers. The supply voltage for each curve is shown in the parenthesis. The minimum supply voltage in the static CMOS circuit needs to be higher than 0.9 V for proper operation if the operating frequency is higher than 300 kHz.

V. Conclusion

We implemented an serial multiplier with nRERL to verify its usefulness. We found that nRERL could be operated at the leakage current-level so that it consumed much less energy than the static CMOS logic at lower speed. In conclusion, nRERL is suitable for the applications that do not require high performance but low-energy consumption.

Acknowledgements

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References

[1] J. Lim and D. -G. Kim and S. -I. Chae, "Reversible energy recovery logic circuit and its 8-phase clocked power generator for ultra-low-power applications," *IEICE Trans. on Electronics*, vol. E82-C, no. 4, pp. 646-653, April 1999.

[2] J. Lim and D. -G. Kim and S. -I. Chae, "A 16-b carry-lookahead adder using reversible energy recovery logic for ultra-low-energy systems," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 898-903, June 1999.

[3] J. Lim and D. -G. Kim and S. -I. Chae, "nMOS reversible energy recovery logic for ultra-low-energy applications," *unpublished* .

[4] K. K. Parhi, "A systematic approach for design of digit-serial signal processing architectures," *IEEE Trans. on Circuits and Systems*, vol. 38, no. 4, pp. 358-375, April 1991.