A 16-bit Redundant Binary Multiplier Using Low-Power Pass-Transistor Logic SPL

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Abstract— We have designed a 16-bit redundant binary multiplier using pass-transistor logic SPL on a 0.35 μm technology. Number of transistors is 12,349, and area is 1,322 μm $\times$ 332 μm. Measured power dissipation and maximum delay at T=25 °C and VDD=3.3 V are 33.7 mW/100 MHz and 7.4 nsec, respectively.

I. Introduction

In recent years, power consumption, as well as area and speed, is one of most important issue in VLSI design. Pass-transistor logic has been intensively studied as a breakthrough for high-speed and low-power digital circuit. Various kind of pass-transistor logics have been proposed, including CPL (Complementary Pass-transistor Logic), LEAP (LEAn integration with Pass-transistors), and SPL (Single-rail Pass-transistor Logic)[1]. While most pass-transistor logics are based on double-rail structure to achieve high-speed, LEAP and SPL are based on single-rail structure to reduce number of transistors and thus achieve low-power. Especially, SPL uses a long series of pass-transistors to a non-critical path if it is of benefit to reduce number of transistors. This paper reports design and measurement results of a 16-bit multiplier using SPL.

II. Design

A. Multiplication Algorithm

The multiplication algorithm used in this design is based on RB (Redundant Binary) addition[2]. RB adder, as well as carry save adder, is a high-speed carry-propagation-free adder. Detailed techniques proposed in [3] is adopted in our design. As shown in Fig. 1, the multiplier consists of four blocks, (1) Booth's recoder, (2) partial product generator, (3) RB adders, and (4) RB-to-binary converter. For (4), we used carry select adder. Inputs and output of the multiplier are signed binary numbers (2's complement).

B. Circuit and Layout

Basically, an SPL circuit is obtained from BDDs[4] by replacing each BDD node with two pass-transistors. For example, BDDs of a 1-bit RB adder shown in Fig. 2 are converted to an SPL circuit shown in Fig. 3. Note that a trickle pull-up PMOS is attached to each output of a series of NMOS pass-transistors, because NMOS pass-transistor cannot drive CMOS gates. In the left part of the circuit in Fig. 3, inverters are inserted as intermediate buffers to improve performance.

After circuit design is completed, SPL cells are designed manually. For example, the circuit in Fig. 3 (66 transistors) is implemented as two cells (26.6 μm $\times$ 15.4 μm and 37.8 μm $\times$ 15.4 μm) on 0.35μm technology. Finally, cells are placed and routed. Placement is manually designed, while routing is automatically performed by AquariusXO.

Total number of transistors and area is 12,349 and 1,322 μm $\times$ 332 μm, respectively.

III. Measurements and Conclusion

The multiplier is fabricated by 0.35 μm triple metal CMOS process. Micrograph of the multiplier TEG is shown in Fig. 4. Power dissipation for pseudo-random pattern measured at T=25 °C and VDD=3.3 V is 33.7 mW when input rate is 100 MHz. From schmoo plot in Fig. 5, maximum delay at VDD=3.3 V is 7.4 nsec. Delay is measured as clock-to-clock delay of input and output FFs. This means that measured delay includes delay of the input FFs and setup time of the output FFs (approx. 0.5 nsec and 0.2 nsec, respectively, at VDD=3.3 V).

For comparison, physical design and circuit simulation of a 16-bit multiplier generated by a logic synthesis tool for the same target technology is performed. Its power dissipation and maximum delay are 83.0 mW/100 MHz and 5.4 nsec, respectively. Note that energy-delay product of our multiplier is 44% smaller.

From these results, we can see that a low-power 16-bit

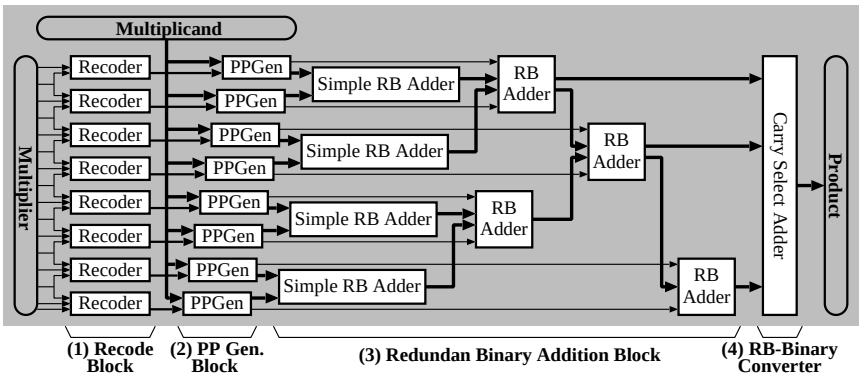

Fig. 1. Block Diagram of the Multiplier

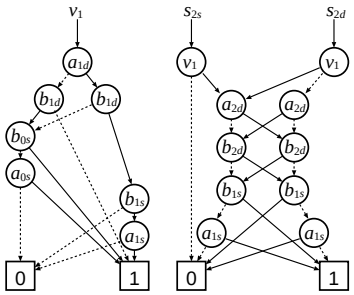

Fig. 2. BDDs of 1-bit RB Adder

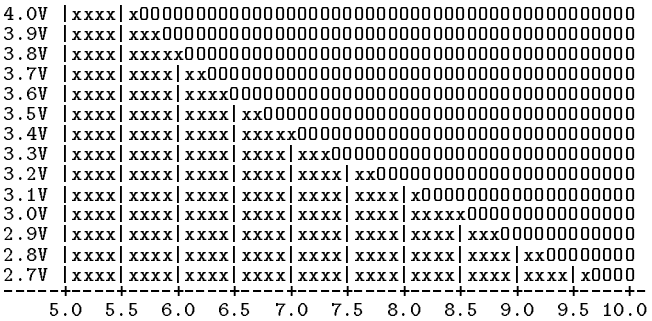

Fig. 5. Schmoo Plot of the Multiplier

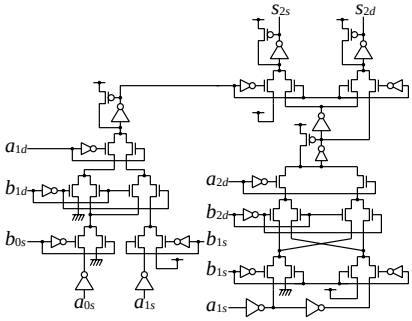

Fig. 3. Circuit of 1-bit RB Adder

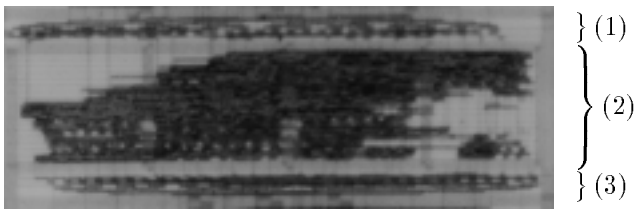

Fig. 4. Micrograph of the Multiplier TEG
(1) Input FFs, (2) Multiplier, (3) Output FFs

multiplier is successfully developed using pass-transistor logic SPL. As a future work, we are planning to develop multipliers of other architectures using SPL.

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