A Binary Image Sensor with Flexible Motion Vector Detection using Block Matching Method

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Abstract— A binary image sensor with motion vector detection has been developed and successfully tested. The sensor acquires binary images and detects motion vectors using block matching method. The size of matching blocks and the search area of motion vectors are variable. The block matching is realized by a 2-D shift-register, XOR circuits and block current-sum circuits. The sensor integrates 32×32 pixels on a 7.3mm×7.3mm die in a 1.2μm CMOS 2-Metal 2-poly-Si process.

I. Introduction

Motion vector detection is one of the key techniques in the field of image processing and requires large computational power for real-time image processing. In several applications, such as robotics, the frame rate higher than the normal video frame rate, such as 100-1000 frames/sec or higher, is required. The smart sensor is an approach to process images at a high frame rate, where image sensors are integrated with pre-processing circuits on the same chip.

The merit of the smart sensor is that it can process image data quickly. While, the flexibility of image processing with smart sensors tends to be limited. In the previous studies on image sensors with motion vector detection [1][2], the size of matching blocks or the search area of motion vectors are limited. In this study, a binary image sensor with motion vector detection has been developed and tested. The size of matching blocks and the search area of motion vectors can be varied flexibly using analog current-sum circuits to calculate the sum of absolute differences.

II. Circuit realization

The sensor has circuits to detect motion vectors using block matching method. Figure 1 shows the circuit diagram of a pixel. Each pixel has a photo detector, a flip-flop, a 1-bit latch, a shift-direction controller and two XOR circuits. The photo detector is composed of a photo-diode and a 1-bit binary latch (LATCH1). The photo-diode integrates photo-current and LATCH1 converts the output voltage of the photo-diode to a binary

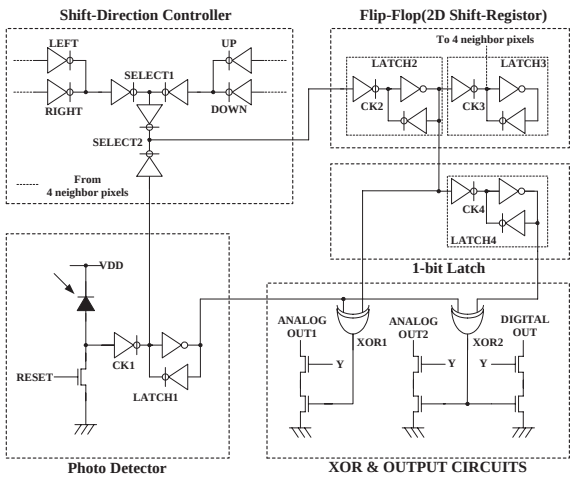


Fig. 1. Schematic of a pixel

value. LATCH2 and LATCH3 compose a flip-flop. The flip-flop is connected to four neighbor pixels, up, down, left and right, through their shift-direction controllers. Thus, the 2-D quad-directional shift-register is composed of the flip-flop array in pixels. The 2-D shift-register stores the image of the previous frame and shifts the entire stored image to up, down, left or right in one cycle. Using the 2-D shift-register, the image can be shifted to any location, so that the search area of the motion vector is flexible.

XOR1 in Figure 1 compares the image of the current frame and the image of the previous frame which is shifted by the 2-D shift-register. XOR2 compares the image of the current frame and the shifted image in LATCH4. Here, LATCH4 stores the shifted image of the previous frame whose sum of absolute differences is the temporary minimal value in the process of motion vector detection. Output nodes of two XOR circuits are connected to current source transistors. Two current source transistors are connected to two sets of block current-sum circuits in Figure 2, respectively.

Figure 2 shows a circuit diagram of current-sum circuits and an analog comparator. A current-sum circuit sums up absolute differences in a selected region, which is a matching block in the case of motion vector detection.

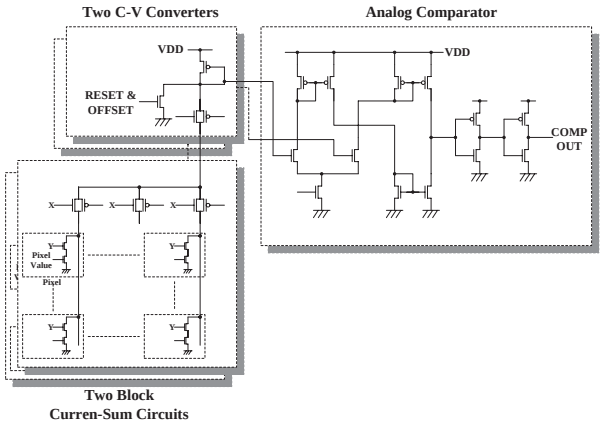


Fig. 2. Schematic of block current-sum circuits and an analog comparator

TABLE I
Summary of the image sensor

Process	CMOS 1.2μm 2-metal 2-poly-Si
Chip size	7.3mm×7.3mm
Num. of pixels	32×32
Pixel size	175μm×175μm
Photo diode size	35μm×55μm
Fill-factor	6.3%
Num. of FETs in a pixel	111 Transistors
Num. of FETs	120k Transistors

The output of one current-sum circuit is proportional to the sum of absolute differences between the current frame and the shifted previous frame in LATCH2. The output of the other current-sum circuit is proportional to the temporary minimal sum of absolute differences between the current frame and the shifted previous frame in LATCH4. The analog comparator in Figure 2 compares the output currents of the two current-sum circuits. If the sum of absolute differences takes a smaller value than the temporary minimal value, the output flag of the comparator becomes "HIGH". Thus, motion vectors are determined by watching the flag output of the comparator. The number of cycles required for the block matching process does not depend on the size of matching blocks, but it depends on the size of the search area. For example, $(2n+1)^2$ cycles are required, when the search area is limited within the nth nearest neighbors.

Figure 3 shows a photograph of the image sensor chip, and Table I shows a summary of the image sensor. The sensor integrates a 32×32 sensor array, two sets of block current-sum circuits, a block logical-OR circuit and an analog comparator on a 7.3mm×7.3mm die in a CMOS 1.2μm 2-metal 2-poly-Si process.

III. Measurements and evaluations

Figure 4 shows a measurement result of motion vector detection with a fabricated chip. Here, the entire image is divided to 8×8 matching blocks. In the case of Figure 4, motion vectors are searched in the eight nearest neighbors and the original position. The image of each matching block is compared with shifted images of the previous frame to determine a local motion vector. Figure 4(a) shows an acquired image, where an object is moving upward. In Figure 4(b), the motion vectors of matching blocks containing the moving object indicate upward directions.

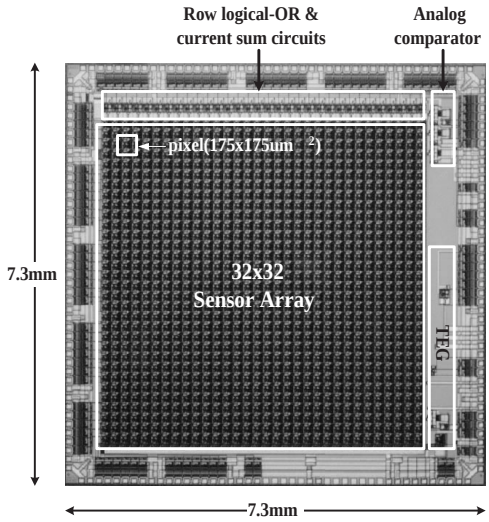
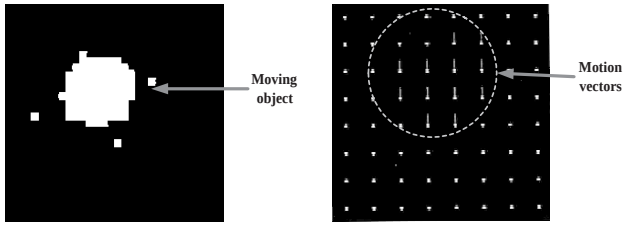


Fig. 3. Photograph of the image sensor chip

Measurements are done at 10-50 frames/sec. This is due to a slow I/O board of PC that controls the image sensor and acquires data. As a result of circuit simulation, the sensor can calculate the motion vectors (in Figure 4) within 250μs. Using a faster controller, the sensor can achieve higher frame rate up to 2000frames/sec, assuming that the time required for image acquisition and calculation ratio is 1 to 1.



(a)Acquired image (b)Motion vectors

Fig. 4. An acquired image and motion vectors

IV. Conclusions

A binary image sensor with motion vector detection has been developed and successfully tested. The search area of motion vectors is variable using a 2-D shift-register which can shift acquired images flexibly. The sensor can calculate the sum of absolute differences in one matching block in one cycle. The size of each matching block is variable, using block current sum circuits to calculate the sum of absolute differences.

References

[1] R. A. Deutschmann and C. Koch, "Compact real-time 2-D gradient-based analog VLSI motion sensor," Proc. of SPIE, Vol.3410, pp.98-107, 1998.

[2] Z. Li, K. Aizawa and M. Hatori, "Motion vector estimation on focal sensor plane by block matching," Proc. of SPIE, Vol.3410, pp.215-221, 1998.