A Smart Imager for the Vision Processing Front-End

Noriaki Takeda, Mituru Homma, Makoto Nagata, Takashi Morie and Atsushi Iwata
Advanced Sciences of Matter, Hiroshima University
1-4-1 Kgamiyama, Higashi-Hiroshima, 739-8527 Japan
{take,nagata,morie,iwa}@dsl.hiroshima-u.ac.jp

Abstract-- A CMOS PWM imager which realizes block summation and 2D projection of a thresholded image, in addition to row-parallel PWM readout with gray scale, is reported. An imager including 56 x 56 pixels, an address signal generator, and a signal processing circuit is fabricated in a 6mm x 6mm chip with a 0.8μm CMOS technology.

I. Introduction

To realize intelligent vision processing systems, high functionarity of CMOS imager attracts attentions.

This paper introduces a 2D image processing CMOS sensor using pixel level PWM signal processing and Charge-Packet Counting techniques. The imager realizes 1) row parallel single or multi-bit PWM readout, 2) block summation, and 3) 2D projection of thresholded images. Block summation is useful to obtain the local feature of the input image. 2D-projection gives the roughly shape of input and it can be applicable to motion detection.

II. PWM Signal Processing

A PWM (Pulse Width Modulaton) signal expresses an analog value on the pulse width with a binary voltage or current amplitude. Time domain expression eliminates voltage/current domain analog processing, and provide immunity to dynamic range reduction caused by a low voltage operation.

A switched current integration technique realizes PWM arithmetic. Switched current sources (SCSs) convert voltage PWM pulses into current PWM pulses. Current integration on a capacitor results in asynchronous, parallel addition of those pulse widths [1].

III. Imager Architecture and Circuit Configuration

Fig.1 shows a blockdiagram of the PWM imager. A pixel comprises an N^+P junction photo detector, a sampling capacitor, and a comparator. It has two operation modes for gray scale conversion and thresholding, where each pixel generates a PWM signal with the width proportional to the pixel value in the former mode, and generates a pulse or nothing in the latter. An address signal generator supply linear upward ramp voltages to the selected column pixels in the gray scale conversion, or a reference voltage to them in the thresholding.

Pixels asserted by both of the column and row address shift registers, become active for readout. These registers provide pixel readout modes of arbitrary addressing, row parallel column sequential addressing, and block accesses of arbitrary pixel sub-matrices. Row pixels share a readout bus which is driven by the current pulses in parallel in the block access mode.

In the block summation, pixels in an arbitrary sub-matrix (up to 8x8) generate current mode PWM pulses in parallel, and these currents are integrated on the capacitor C_{int}, as shown in Fig.2(a). Here, each readout bus has a local integration capacitor and a local PWM signal generator that forwards a current PWM signal proportional to the local integration charge to C_{int} through the vertical current bus (B_{vc}).

Integrated charge Q_{int} on C_{int} gives a sum of pixel values. The charge packet counter (CPC) converts a small reference charge amount Q_{ref} to a pulse and removes it from Q_{int} successively during the integration, and a block average is calculated dividing the sumtotal of pulse counts by the number of sub-block pixels.

In the 2D projection shown in Fig.2(b), pixels work for the thresholding, and generate voltage pulses by the row parallel readout. Y-projection values are obtained as the number of pulses counted by the row counters. On the other hand, X- projection values are obtained by the switched current integration, and the use of CPC. [2]

IV. Experimental Results

An experimental PWM functional imager chip is fabricated in a 0.8μm CMOS technology. A microphotograph and details are given in Fig.3.

Fig.4(a) shows output of the voltage mode PWM pulses in the row parallel gray scale readout when a gradation test pattern (Fig.4(b)) was focused on the imager surface. Fig.4(c) shows the experimental results of block summation under the same input condition, where the block size changes from 1x1 to 8x8 pixels (1): from the bright part to the dark part, (2): form the dark part to the bright part and (3): from the lower left part to the upper right part. The solid line and the broken line show pulse counts of CPC, and summation of PWM pulse width in Fig.4(a) as the expected value, respectively. The increase in errors from the expected values for pulse counts more than 250 is owing to the decrease in current among pixel SCSs, where current source MOSFET is out of saturation.

Fig.5(b) and (d) shows the experimental results of X-projection when the binary test pattern (a) and (c) were focused on the imager surface, respectively. The features of input patterns are obtained well and the pulse count errors from the expected values are within 3 pixels. The operation time is 112 μs.

These functions are useful for a flexible vision processing, like character recognition and face recognition [3].

V. Conclusions

A test chip of a PWM imager with functions of block summation and 2D projection in addition to row parallel gray scale readout and thresholding was introduced. From experiment results we confirmed operations of these functions.

Acknowledgments

This work was partially supported by the M.E.S.S.C. Japan under Grant-in-Aid for Scientific Research on Priority Areas

(No. 269), and also by NEDO and FEDO, Japan. Authors thank to NTT Electronics Corp. for the test chip fabrication.

REFERENCES

[1] M.Nagata and A.Iwata,"A PWM Signal Processing Core Circuit Based on a Swiched Current Integration Technique,"IEEE J. Solid-State Circuits, Vol. 33, No. 1, pp. 53-60, Jan.1998.

[2] M.Nagata, M.Homma, N.Takeda, T.Morie, and A.Iwata,"A Smart CMOS Imager with Pixel Level PWM Signal Processing,"Symp. on VLSI CIRCUIT, pp. 141-144, Jun.1999.

[3] A.Iwata, M.Nagata, M.Homma, H.Nakamoto, H.Higashi, N.Takeda, and T.Morie,"A CMOS Intelligent Feature Associative Processor with Functional Image Sensing and A-D merged Parallel Architecture," ISFIIE, P2.18, pp. 401-411, 1999.

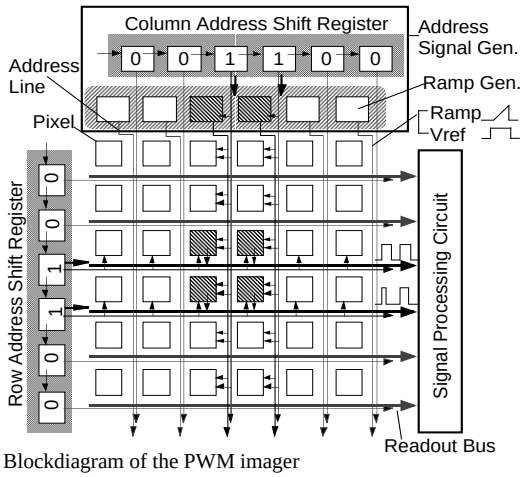

Fig. 1. Blockdiagram of the PWM imager

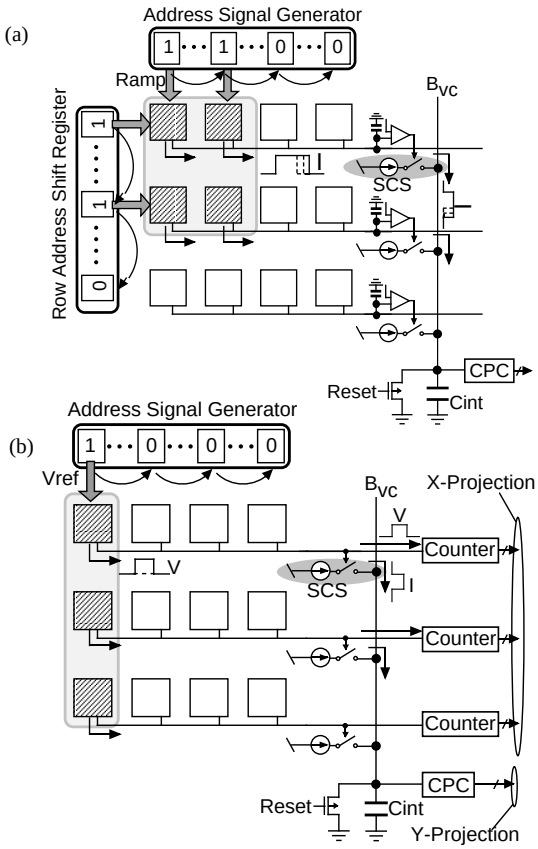

Fig. 2. Circuit configurations for (a) the block summation and (b) the 2D projection

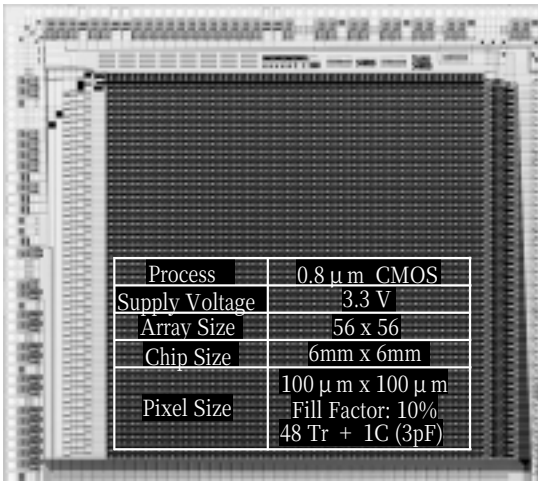

Fig. 3. Imager chip micrograph

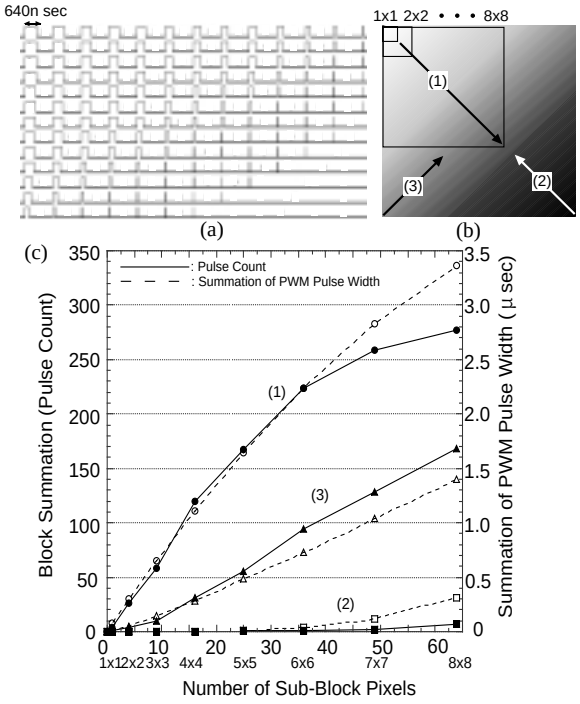

Fig. 4. (a):Voltage mode PWM pulse outputs for test pattern (b), (c):Block summation results in current PWM mode

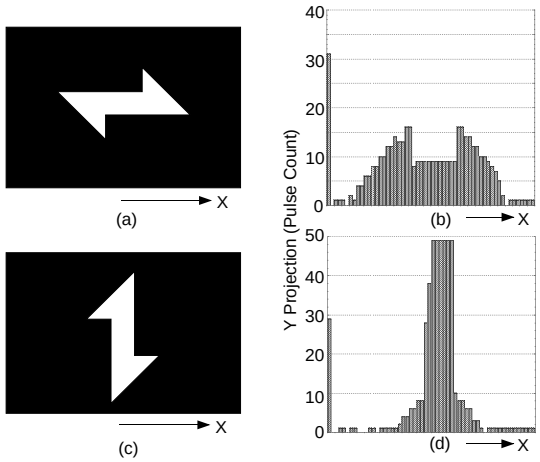

Fig. 5. X-projection experimental results