Table of Contents

Foreword iv
Symposium Organization v
Table of Contents vi

Session 1.0: Welcome and Keynote Address

Moderator: Dwight Hill (Synopsys)

• Welcome to ISPD-99
  D.F. Wong (UT-Austin)

• Tales From the Trenches
  C. Malachowski (nVidia)

Session 1.1: Tutorial on Clocks

Moderator: Sachin Sapatnekar (U. Minnesota)

• Challenges in Clock Distribution Networks
  Eby Friedman, Niraj Bindal (U. Rochester, Intel)

Session 1.2: Tutorial on Noise

Moderator: Manfred Wiesel (Intel)

• The Deep Sub-micron Signal Integrity Challenge
  D. Kirkpatrick (Intel)

Session 1.3: Analog Design and Signal Analysis

Moderator: C.K. Cheng (UCSD)

• Methodology to Analyze Power, Voltage Drop and Their Effects on Clock Skew/Delay in Early Stages of Design
  M. Iwabuchi, N. Sakamoto, Y. Sekine, T. Omachi (Hitachi)

• EMI-Noise Analysis Under ASIC Design Environment
  S. Hayashi, M.I. Yamada (Toshiba)

• An Efficient Sequential Quadratic Programming Formulation of Optimal Wire Spacing for Cross-Talk Noise Avoidance Routing
  P. Morton, W. Dai (UCSC)
Session 1.4: Posters on Timing and Circuits

Moderator: Rob Rutenbar (CMU)

- Post-Routing Timing Optimization with Routing Characterization
  C. Changfan, Y.-C. Hsu, F.-S. Tsai (Avant!)
  30
- Buffer Insertion for Clock Delay and Skew Minimization
  X. Zeng, D. Zhou, W. Li (Fudan U., UNC)
  36
- Incremental Capacitance Extraction and its Application to Iterative Timing Driven Detailed Routing
  Y. Yuan, P. Banerjee (Northwestern U.)
  42
- Interconnect Coupling Noise in CMOS VSLI Circuits
  K. Tang, E. Friedman (U. Rochester)
  48

Session 1.5: Panel: SCR Physical Design Top Ten Problems

Moderator: Chuck Alpert (IBM)

- SRC Top Ten Physical Design Problems
  J. Parkhurst, N. Sherwani, S. Maturi, D. Ahrams, E. Chiprout (Intel, LSI Logic Corp., National Semiconductor, IBM)
  55

Session 2: Benchmarks

Moderator: Jochen Jess (Eindhoven)

- Towards Synthetic Benchmark Circuits for Evaluating Timing-Driven CAD Tools
  D. Stroobandt, P.I. Verplaetse, J. Van Campenhout (U. Ghent)
  60
- Generation of Very Large Circuits to Benchmark the Partitioning of FPGA’s
  J. Pistorius, E. Legai, M. Minoux (Mentor, Pierre et Marie Curie)
  67
- Transistor-Level Micro Placement and Routing for Two-Dimensional Digital VLSI Cell Synthesis
  M. Riepe, K. Sakallah (U. Michigan)
  74

Session 2.1: Partitioning, Placement, and Floorplanning

Moderator: Massoud Pedram (USC)

- Partitioning by Iterative Deletion
  P.H. Madden (SUNY)
  83
- Optimal Partitioners and End-Case Placers for Standard-Cell Layout
  A.E. Caldwell, A.B. Kahng, B.I.L. Markov (UCLA)
  90
- Slicing Floorplans with Range Constraints
  F.Y. Young, D.F. Wong (UT-Austin)
  97
Session 2.2: Tutorial on Manufacturing

Moderator: Andrew Kahng (UCLA)

- Arbitrary Convex and Concave Rectilinear Block Packing
  K. Fujiyosi, H. Murata (Tokyo U.)

Session 2.3: Sizing and Buffering, Plus Lithography

Moderator: Jason Cong (UCLA)

- Optimal Phase Conflict Removal for Layout of Dark Field Alternating Phase Shifting Masks
  P. Berman, A.B. Kahng, D. Vidhani, E.H. Wang, F.A. Zelikovsky (UCLA, Penn State, Georgia State)

- Gate Sizing with Controlled Displacement
  W. Chen, C.-T. Hsieh, M. Pedram (USC)

- Simultaneous Buffer Insertion and Non-Hanan Optimization for VLSI Interconnect Under a Higher Order AWE Model
  J. Hu, S. Sapatnekar (U. of Minnesota)

Session 2.4: Posters on Placement and Partitioning

Moderator: Carl Sechen (U. Washington)

- Efficient Solution of Systems of Orientation Constraints
  J. Ganley (Cadence)

- Behavior of Congestion Minimization During Placement
  M. Wang, M. Sarrafzadeh (Northwestern U.)

- Partitioning with Terminals: A "New" Problem and New Benchmarks
  C. Alpert, A. Caldwell, A.B. Kahng, I. Markov (UCLA and IBM)

- Transistor-Level Placement for Full Custom Datapath Cell Design
  D. Vahia, M. Ciesielski (U. Mass)

- Circuit Clustering Using Graph Coloring
  A. Singh, M. Marek-Sadowska (UCSB)

Session 2.5: Dinner Talk

Moderator: Martin Wong (UT-Austin)

- Why So Many Start-ups Today? A Designer and Venture Capitalist’s View
  A. Bechtolsheim (Silicon Valley)
Session 3.0: Thermal and MCM

Moderator: Naveed Sherwani (Intel)

- Interconnect Thermal Modeling for Determining Design Limits on Current Density
  D. Chen, E. Li, E. Rosenbaum, S.-M. Kang (U. Illinois)  172

- Standard Cell Placement for Even On-Chip Thermal Distribution
  C.-H. Tsai, S.-M. Kang (U. Illinois)  179

Session 3.1: Global Routing

Moderator: Patrick Groeneveld (Magma)

- Measuring Nets Routability for MCM’s General Area Routing Problems
  Kusnadi, J.D. Carothers (U. Arizona)  186

- Getting to the Bottom of DSM II: The Global Wiring Paradigm
  D. Sylvester, K. Keutzer (U. Berkeley)  193

- Crosstalk Constrained Global Route Embedding
  P. Parakh, R.B. Brown (U. Michigan)  201

Session 3.2: Routing

Moderator: Ren-Song Tsay (Axis)

- Timing Driven Maze Routing
  S.-W. Hur, A. Jagannathan, J. Lillis (U. Illinois at Chicago)  208

- Via Design Rule Consideration in Multi-Layer Maze Routing Algorithms
  J. Cong, J. Fang, K.-Y. Khoo (UCLA)  214

Session 3.3: Panel Physical Synthesis

Moderator: Wayne Dai (UCSC)

- Layout Driven Synthesis or Synthesis Driven Layout
  W. Dai (UCSC)  222

Author Index  222