The Deep Sub-micron Signal Integrity Challenge

INVITED TUTORIAL

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Abstract

Maintaining signal integrity in digital VLSI systems has become increasingly difficult due to the rising number of analog effects in deep sub-micron design. This paper provides an outline of the tutorial to be presented, as well as essential background material on the principle mechanisms behind signal integrity issues. The goal is to put forth a set of signal integrity challenges for future research and development.

1 Motivation

To fully comprehend why signal integrity has become an increasing challenge to high performance design, it is necessary to understand the tradeoff of noise margin versus speed. Almost every avenue for increasing performance comes at the cost of increasing susceptibility to noise failures. Faster devices require lower transistor thresholds, increasing noise susceptibility. Faster wires tend to introduce more coupling capacitance and therefore more crosstalk between wires.

In the past, signal integrity has come from circuits with built-in noise margin: level-restoring fully complementary CMOS has large noise margin and tolerates high levels of signal degradation from noise. But changes in process and circuit technology have eroded noise margins to the point where they need to be actively managed. Signal integrity is no longer globally managed by selecting process voltages and designing standard libraries, but rather must be locally and actively managed.

While signal integrity is now a major issue for custom high-performance design, the degree to which signal integrity is an issue for the ASIC community is still an open question. But if one looks to the reasons that signal integrity has become a large issue, it is reasonable to expect that if signal integrity can be managed through automation, those ASIC designers that incorporate some custom techniques will have an increasingly large performance differentiation.

While post-layout verification is a requirement for signal integrity management, the largest opportunity for signal integrity management lies within physical design synthesis. Since coupling, the largest component of controllable signal noise, is related to wire proximity, the physical design community has the clearest opportunity for automating the management of signal integrity.

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1.1 Scaling Increases Resistance

The primary performance benefit of semiconductor process scaling is reduction of both gate and interconnect capacitance. However, ideal scaling (where all dimensions scale together) implies that interconnect resistance rises by the scaling factor S, where dimensions scale by $1/S$. Until 0.25μ process dimensions, metal resistances were, for the most part, negligible. The first impact of increasing metal resistance is in the well-studied RC delay problem: delay associated with wire resistance has remained steady, while other components of delay have decreased, and now RC delay is a significant component of overall delay. Chip size has gradually increased, and the RC delay of a global net has long passed an inversion delay so that now buffers are used to restore the signal at intermediate points along its way.

As metal resistances increased, process engineers have migrated to wires with higher and higher aspect (thickness/width) ratios. This has improved wire resistance to the detriment of increased coupling capacitance.

A final trend is that target frequencies of high-performance designs have scaled faster than the underlying process, leading to increased pipelining, shorter logic paths, fewer stages per clock, and increased pressure to use faster circuitry.

1.2 Noise Margins Decrease

The quest for higher clock frequencies has led to the use of circuit topologies which trade off noise margin for shorter stage delays. While traditional static logic families such as true CMOS, consist of fully restoring, noise-immune stages, high-performance designers have almost universally adopted dynamic logic for its speed. Dynamic logic has smaller capacitive load (often one transistor – the pull-down transistor – is driven), and switches at a transistor threshold instead of at half of VCC. But this increased speed comes directly at the cost of reducing noise immunity both by reducing the threshold and by eliminating the restoring circuit.

1.3 New Materials Bend Rules

It is notable that the industry is in the midst of transitioning to Cu metalization, and looking forward to a progression of low-k dielectrics in the future [1]. With the resistance of Cu almost 30% lower than Al, this would appear to stave off resistive increases for a process generation (1/S = 0.7). However, "because Cu processing is still an immature technology you can't do lines as thick as you could with Al at the same pitch" [2]. Therefore in the Cu generation, the RC delay component will increase, though not as much as in a traditional process transition, and coupling may actually decrease. Beyond Cu, low-k dielectrics can partially offset RC delay encroachment, but will not slow the increase of coupling concerns, especially if process engineers must gradually increase wire aspect ratios once again. Material replacement will shift, but not change the scaling trend-lines.

2 Noise Effects

Digital logic is inherently noise-immune, due to its use of the digital circuit abstraction of binary logic and restoring logic stages. However, noise impacts digital systems by causing two different kinds of problems: delay and logic noise effects.

2.1 Delay Effect

Noise impacts performance by slowing voltage transitions through a Miller-like effect: an aggressor couples charge into a victim while the victim is trying to transition, potentially slowing it down. Thus, the delay effect is caused by *delay noise*, or increased delay uncertainty. The effect is, loosely, a doubling (nullification) of the effective capacitance seen between the two wires switching in the opposite (same) direction. The min-delay, or earliest time at which a signal may switch, can be accelerated by aggressors switching in the same direction. The max-delay, or latest time at which a signal may switch, can be delayed by aggressors switching in the opposite direction. These effects can be exaggerated by threshold conditions. For delay effects, the concern is when a data signal is slowed by coupling while the clocking signal is accelerated, narrowing the amount of time the data signal has to setup when entering a latch. These problems can be solved by slowing the global system clock and a functional, though slower, design results.

2.2 Logic Effect

Noise can induce logic errors in certain kinds of fast circuitry, as well as in latches or any other circuit which maintains state. Dynamic circuits are fast because they disable restoring transistors, and trip at a transistor threshold. These characteristics also make them susceptible to noise failures. Not only is the threshold for accidentally tripping much lower, but once tripped by a noise event, there is no restoring circuitry to prevent propagation of a false value. Thus, the logic effect is caused by *voltage noise*. While CMOS circuitry is essentially noise-immune, noise may accumulate in several stages, especially long parallel repeated wires, and propagate significant noise into a sensitive circuit such as a latch.

Another type of functional failure is noise-induced race failures. These occur when a hold-time is violated because a signal delay is accelerated and races ahead of the clocking signal designed to block its propagation. Slowing the global clock frequency does not eliminate this effect, therefore this is a functional failure. These problems are exacerbated by increasing coupling capacitance, which in turn increases delay uncertainty.

3 Noise Sources

Sources of noise for digital circuits that are not random, but related to the operation of nearby circuitry are candidates for signal integrity management. Other noise sources that affect transistors, such as power supply ringing, or more directly, cosmic rays or alpha rays emitted by packaging materials, are essentially random or extremely difficult to predict. Such noise sources must be controlled through global design. The set of noise sources to consider for signal integrity management are:

- Capacitive coupling: charge injection from a capacitive divider formed when an aggressor switches adjacent to a victim line. This is a function of the ratio of coupled to total capacitance on the victim (C_C/C_T) as well as the relative time constants of aggressor and victim.
- Supply noise: voltage noise on the supply from switching nearby signals or local IR drop.
- Charge sharing: charge injection on the output of a stage due to the formation of a new circuit path to a large diffusion capacitance at a different voltage.

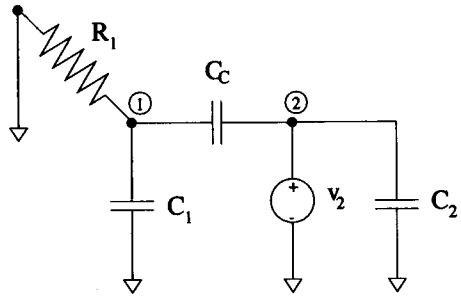

Figure 1: Basic Coupling Circuit

- Source-drain leakage: dramatic increase in standby drain currents at today's low threshold voltages.

Note that signal inductance (self-inductance as well as mutual inductance) is not included. For narrow width wires, inductive effects are far outweighed by the lossy RC effects. Once wires become wider, the more complex effects of frequency dependent return paths have a large role in determining signal inductance and lie outside the scope of this tutorial. Power supply inductance contributes to supply noise as dI/dt voltages and return paths play a large role here.

Design automation can have a large amount of control on coupling capacitance; the context of other noise sources provides a bound on the amount of coupling a signal can handle. The goal of design automation should be to synthesize circuits which don't fail by controlling these noise components during synthesis. A very important part sub-problem is managing coupling noise during layout.

3.1 Victim Coupling Response

The most important noise source to understand is capacitive coupling as it is both the largest source as well as the most often overestimated. It is also the easiest to control through the introduction of increased space or shielding. The victim response voltage of C_C/C_T is reached asymptotically only when the aggressor rises much more quickly than the victim. Here we provide the victim response to an exponential aggressor input ([3]), given the circuit in Figure 1:

$$C_{T_1} = C_C + C_1$$

$$v_1(t) = \frac{C_C}{C_{T_1}} \begin{cases} \frac{t}{\tau_1} e^{-\frac{t}{\tau_1}} & \text{if } \tau_1 = \tau_2 \\ \frac{\tau_1}{\tau_2 - \tau_1}\left(e^{-\frac{t}{\tau_2}} - e^{-\frac{t}{\tau_1}}\right) & \text{otherwise} \end{cases}$$

3.2 Noise Superposition

Multiple noise sources act upon a victim circuit and must be considered simultaneously. For example, consider the circuit in Figure 2. Here, up-going coupling noise on a transistor gate v_g creates an equivalent amount of noise current i_d on the transistor drain as the same amount of down-going supply noise on the transistor source v_s. While the receiving transistor is typically off, multiple noise sources may combine, and v_{gs} may approach or surpass the transistor threshold, perturbing the transistor into the linear (triode) region and producing a noise current. The drain node of the receiving transistor may be perturbed directly by charge sharing and leakage.

The worst combination of all noise sources may flip the state of the drain node if it is not restored or is weakly held. For coupling noise, superposition principles apply as voltage noise impinges on

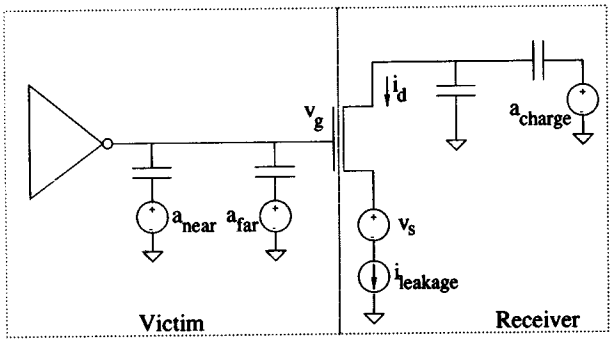

Figure 2: Noise Sources

the receiving transistor in the linear (triode) region of operation. Parallel transistors cause noise currents to add; wide nor structures create a sum of output noise currents, whereas transistor stacks impose a MAX function (noise propagates in a stack when all other transistors in an N-stack are on). These currents are weighted by transistor width and superimpose or sum due to linearity.

An important consideration when superposing noise sources is to consider how their peaks align. An aggressor located at the *near-end* or driver portion of a wire must fire sooner than an aggressor located at the *far-end* or receiver portion of a wire in order to align their effects. Receiver failure is conservatively considered if noise sources are aligned such that their superposition maximizes i_d's effect on the receiver. This means i_d must be high enough and last long enough to flip state. While i_d may not be strong enough to flip the output state of the receiver, it may propagate and combine with other noise to flip some state in the transitive fanout.

A final consideration for superposition is to include propagated or residual noise on the previous driver output.

4 Managing Signal Integrity

One way to organize signal integrity is to consider how a signal may be naturally isolated from noise sources. Here is a set of very general categories of noise isolation:

- Analog isolation: the noise injected into a victim signal (in concert with other noise sources) is immediately dissipated or does not reach a threshold voltage.
- Physical isolation: the noise source is separated by space or other wires which effectively shield the victim from the noise source.
- Temporal isolation: the noise source is active during a time interval when its effects on the victim signal will not being sampled (or when other sources under consideration are not active).
- Logical isolation: the noise source is active under logic conditions for which the victim cannot be observed (or when other noise sources under consideration are not logically enabled).

Design automation support for managing signal integrity is very much a new field. While some support exists in routers, there is little evidence of effective techniques when applied to large numbers of signal integrity constraints. Let analysis, verification, and synthesis represent three increasing stages of CAD technology maturity (for example, consider logic design, from DeMorgan to MOSSIM to SIS). Noise automation is fairly immature, with most techniques lying somewhere between analysis and verification.

4.1 Signal Integrity Verification

Some of the earliest digital signal integrity checks were simple voltage threshold checks using simple coupled capacitance models based on aggressor rise-time [4]. Today, the state of the art is represented by propagation approaches such as [5] which parallel static timing algorithms by pushing noise values along circuit paths in a pattern-independent way. Still, full hierarchical models or models that encompass both timing and noise, have yet to be developed.

A parallel development has been timing window analysis which determines which aggressors may fire together. A clear circularity exists here: how do you find out which aggressors fire together using timing windows if their action may impact delay and shift those windows? Only rudimentary approaches completing timing analysis with delay noise have been proposed.

The problem of finding if a coupling effect can be sensitized (similar to the problem of finding sensitization criteria for the true path delay) remains an open problem.

4.2 Signal Integrity Synthesis

The area of synthesis to avoid noise failures remains largely unexplored. Here are proposed goals of signal integrity synthesis:

- Circuit Synthesis Goals: to size circuits to meet both timing and noise constraints simultaneously.
- Layout Synthesis Goals: to isolate signals with spacing or shields to robustly meet circuit noise constraints with minimal cost (area, power).

4.2.1 Signal Integrity Constraint Generation

As with synthesis for performance, where slack allocation transforms high-level performance goals into nodal constraints, there is a need for transforming noise constraints into something manageable by physical design tools. One notable contribution here is our work in digital sensitivity analysis as a framework for constraining synthesis for signal integrity [3]. Each level of isolation described in Section 4 is addressed in a constraint system for managing both delay and logic noise effects.

4.2.2 Routing for Signal Integrity

There have been several contributions in routing ([6], [7]) to avoid crosstalk, both in global and detailed wiring. These tools introduce either spacing or shielding to minimize coupling until node bounds on coupling are met. A common problem in current synthesis approaches is minimizing an objective function that is not truly the goal of signal integrity management. For robust design, the goal should be to satisfy all signal integrity conditions, minimize area, and minimize the number of conditions which are at their limit. If large numbers of signals are at their integrity limits, the robustness of the design will be poor. For instance, if the design were ported to a slightly different process, fixing it to make it work would be futile.

5 Key Sub-Problems

We propose a set of key sub-problems to signal integrity management which are still open:

5.1 Circuit Analysis

- Distributed Coupling Analysis: The efficient analysis of aggressors which couple with a victim over some distance. While moment-matching techniques can be employed, are we sure we have the right moments for noise?
- Inductive Return Analysis: Comprehending the frequency dependent behavior of return currents in analyzing signal inductance. This problem is one of the most difficult to fully analyze, and clearly a simple model of the behavior is desirable.

5.2 Global Analysis

- Coupling Delay Timing Analysis: This ranges from topological path delay with guaranteed time bounds to exact delay computation with full delay and coupling sensitization conditions.
- Hierarchical Noise Analysis: Extending the parallel between noise propagation and topological path delay analysis to a hierarchical model of noise, noise slack, constraints for synthesis, etc.
- Logical Crosstalk Prediction: Sensitization conditions for the controllability and observability of coupling effects. See [3] for one attempt.

5.3 Layout Synthesis for Signal Integrity

- Layout and circuit building-block architectures: Correct-by-construction techniques for signal integrity can be considered, such as PSSG (power/signal/signal/ground) layout architectures. Are there new libraries/cell architectures that can avoid the difficulties of noise analysis while delivering the performance of dynamic logic?
- Constraint systems (Noise bound 'allocation'): Transforming the requirement of zero noise failures into physical constraints that are feasible for physical synthesis tools.
- Crosstalk avoidance routers: Incorporating shielding, spacing, and relative shielding, along with a constraint system, to produce layout free from noise effects.

6 Conclusions

The RC delay problem has received a large amount of attention in both analysis and performance-driven physical synthesis (wire sizing, tapering, etc). While reducing RC delay is the most direct way of optimizing performance, it is intimately related to signal integrity through the tradeoffs for performance made from process feature design to circuit family selection. Solving signal integrity problems fundamentally impacts how fast circuits can be driven. Furthermore, while RC delay increases may be slowed by the introduction of new materials, after the Cu generation, coupling noise is destined to increase with process scaling. Ultimately, signal integrity is what will limit obtainable design performance.

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