Mixed-Swing QuadRail for Low Power Dual-Rail Domino Logic

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ABSTRACT

This paper describes a new mixed-swing topology for dual-rail domino logic that results in a simultaneous energy and delay reduction. HSPICE simulation results for a 1-bit full adder cell show a 24% delay decrease and a 24% energy reduction for the mixed-swing topology compared to standard dual-rail domino. Energy and delay trends with supply voltage scaling are also presented for the adder cell. An 8-bit by 8-bit multiplier design with mixed-swing dual-rail domino adders is presented. Simulation results show this implementation to be 10% faster with an 18% energy savings.

1. INTRODUCTION

Domino CMOS [1] has become the prevailing logic family for high performance CMOS applications and it is extensively used in most state-of-the-art processors due to its high speed capabilities. The drawback of domino CMOS is that it provides only non-inverting functions because of its monotonic nature. Dual-Rail Domino logic, (also known as clocked Cascode voltage switch logic [2]) where both polarities of the output are generated, provides a robust solution to this problem. Other techniques either have latches built into the gate [3], [4], resulting in very finely pipelined designs, or make use of delayed clocks [5], making the design sensitive to manufacturing variations. The penalty associated with dual-rail domino logic is the increased power dissipation compared to static CMOS as well as dynamic circuit techniques which use single-ended logic gates. In this paper we explore a mixed-swing topology wherein multiple supply voltages are used in a dual-rail domino logic gate that offers simultaneous power and delay reductions.

In Sec. 2, we present the new Mixed-Swing Dual-Rail Domino (MSDRD) topology, contrast it with conventional Dual-Rail Domino methods, and explore the energy-delay space for a mixed-swing implementation of a dual-rail domino full adder. Sec. 3 describes a mixed-swing implementation of an 8-bit multiplier which uses the adder cell of Sec. 2. Sec. 4 presents simulation results comparing standard dual-rail domino and mixed-swing dual-rail domino implementations of the multiplier in an Hewlett-Packard 0.6µm drawn CMOS fabrication process.

2. Mixed-Swing Dual-Rail Domino Logic

Mixed-Swing QuadRail is a multiple power supply methodology in which each gate has multiple power supply voltages available to it. This expands the number of degrees of freedom available in the energy-delay optimization space of the design. A four-power-rail methodology called Mixed-Swing Quadrail has been proposed previously to construct static CMOS digital logic gates using multiple voltages [8], [9]. In this paper we present a variation of that Quadrail methodology for dual-rail domino circuits that can provide power reduction and delay reduction [12]. The fact that the critical transition in domino circuits is always uni-directional, has been used to evolve a topology that can meet the twin objectives of power reduction and delay reduction.

2.1 Gate-Level Circuit Design

Fig. 1 shows a mixed-swing dual-rail domino gate. The VDD_{INV} and VSS_{INV} supplies are routed to the output inverters, and the VDD_{LOG} and VSS_{LOG} supplies are supplied to the internal logic transistors. In the evaluate phase, this circuit topology is essentially a static DCVSL gate. It exhibits DC recovery, thus providing static circuit testability. The combination of static logic within a clocked structure resembles Pulsed Static Logic (PS-CMOS) [7]. Note, if standard domino logic with pfet pull-up transistors and pfet keeper transistors is used, the noise margin is set by V_{tn}; and, it is relatively poor. In order to improve and control the noise margin, we employ a modified circuit topology, called cross-coupled domino [6]. The cross-coupled pfets can be sized up without significantly affecting the delay through the domino gate since they do not contend with the nmos stacks during evaluation. The input noise margin is determined by the ratio of the sizes of the pfet keeper to that of the nfet stack. For the circuit of Fig. 1 the keeper can be sized up until the noise margin approaches that of static CMOS. This technique improves the noise margin considerably with little impact on delay or energy. Like cross-coupled domino logic, mixed-swing dual-rail domino logic can be switched into completely static operation by keeping the clock high. The circuit can be switched between high-speed dynamic operation and low-power static operation. This feature can also make the circuit significantly easier to test.

In QuadRail operation, the voltage swing across the inverter is reduced by pulling up its lower rail, so that $VSS_{INV} > VSS_{LOG}$. Simultaneously, the voltage swing across the logic circuit is reduced by pulling down its upper rail, so that $VDD_{INV} > VDD_{LOG}$. Obviously, this moves the V_{OL} of the gate up by $VSS_{INV} - VSS_{LOG}$ which illustrates why the cross-coupled topology is essential for

mixed-swing techniques to work. Note, as with any dual-rail domino implementation transistors can be shared between the nmos trees for the true and the complement functions to generate more compact circuits.

The worst case evaluation delay through the gate is determined by the discharge delay through the dynamic circuit and the pull-up delay through the inverter. The precharge time is usually hidden and does not contribute to the worst case delay. Assuming a long channel approximation for the fets, the worst case gate delay is approximately

$$td \approx \frac{k_1(VDD_{LOG} - VSS_{LOG})}{\beta_{neff}(VDD_{INV} - VSS_{LOG})^2} + \frac{k_2(VDD_{INV} - VSS_{INV})}{\beta_p(VSS_{LOG} - VDD_{INV})^2}$$

Assuming dynamic power to be much larger than static or short circuit power, the power dissipation of the gate is approximately

$$Power \approx C_{dyn}\alpha(VDD_{LOG} - VSS_{LOG})^2 f + C_{inv}\alpha(VDD_{INV} - VSS_{INV})^2 f$$

where C_{inv} is the total load capacitance driven by the inverter, C_{dyn} is the total load capacitance driven by the dynamic logic gate, α is the activity factor and f is the frequency. From these equations it can be seen that performance improvement and power reduction can be obtained simultaneously by minimizing the voltage swing in the logic block and the inverter and by maximizing the difference VDD_{INV} - VSS_{LOG}. Two different operating modes are possible for this circuit depending on the value of VDD_{LOG}. When $VDD_{LOG} = VDD_{INV}$ we have Trirail. The topology shown in Fig. 1 is called Quadrail since it has four distinct supply rails.

2.2 Exploring the Energy-Delay Space

To explore the energy-delay space of the mixed-swing dual-rail domino methodology in a more realistic manner, a full adder was considered. Detailed HSPICE simulations were carried out using the Level 13 BSIM1 models in the Hewlett-Packard 0.6µm drawn CMOS process. The outer rails, VDD_{INV} and VSS_{LOG}, were fixed at 2.4V and 0V respectively. Fig. 2 and Fig. 3 show the energy and delay, respectively, as a function of the difference between the inner and outer rails for the Trirail and Quadrail topologies. For the Quadrail case both the inner rails, VDD_{LOG} and VSS_{INV}, were moved by the same amount from the outer rails.

From Fig. 2, for the Trirail case, the optimal point for VSS_{INV} is a V_{tn} above VSS_{LOG}. Beyond this point the nfets in the dynamic gate are turned on and there is a significant short circuit current in the dynamic logic circuit. For Quadrail the increase in short circuit

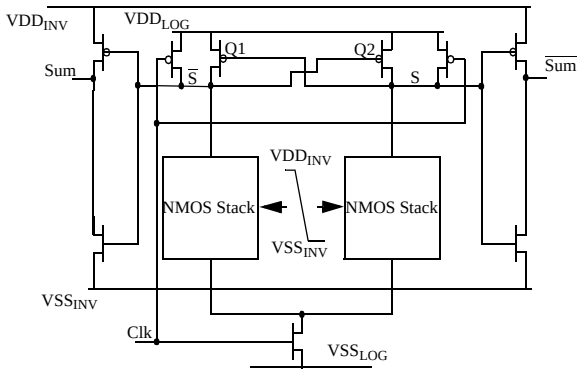

Figure 1. Mixed Swing Dual-Rail Domino Logic.

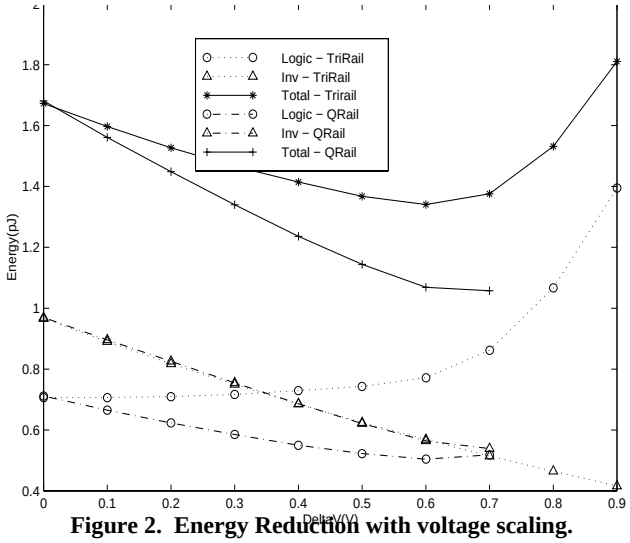

Figure 2. Energy Reduction with voltage scaling. (DeltaV = VSS_{INV} - VSS_{LOG} = VDD_{INV} - VDD_{LOG})

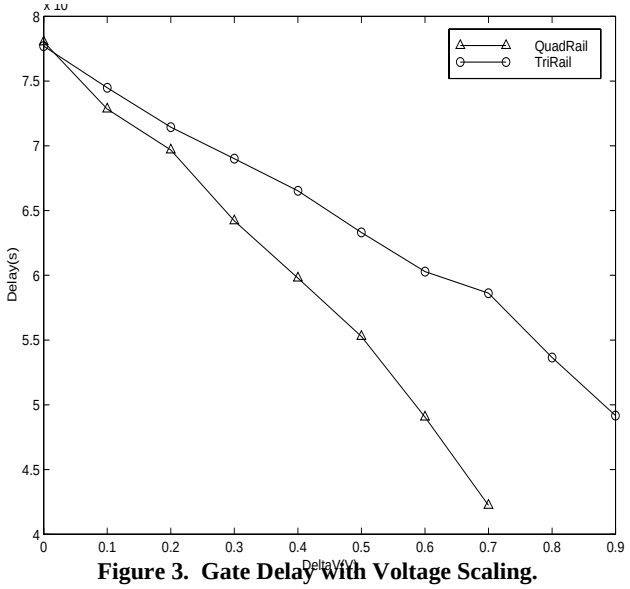

Figure 3. Gate Delay with Voltage Scaling.

current is offset by the reduced voltage swing across the logic circuit. And, the optimal voltage is set by noise margin constraints.

Table 1 gives the energy-delay comparisons for a mixed-swing dual-rail domino adder with a standard dual-rail domino adder. The VDD_{INV} and the VSS_{LOG} were fixed at 2.4V and 0V respectively. VSS_{INV} was set to 0.5V and VDD_{LOG} was set to 2.2V to give a noise margin of about 0.6V, which is around a V_{tn}, the typical noise margin in single-ended domino circuits. The standard dual-rail domino adder cell is operated on a single 2.4V power supply. As can be seen from Table 1, mixed-swing dual-rail domino delivers significant reductions in energy and delay over standard domino.

3. Multiplier Architecture

Multipliers are an important part of most DSP and processor cores. With escalating demand for higher performance in both of these areas, domino CMOS finds increasing use in multiplier circuits to keep up with increasing performance demands. The inverting nature of the functions involved in a multiplier necessitates the use

of dual-rail domino logic in order to design robust, low latency, high performance multipliers.

Fig. 4 shows the block diagram of the multiplier to which the Mixed Swing methodology was applied to demonstrate the power savings obtained with the mixed swing approach. The multiplier was designed to be part of an FIR filter. It takes in 8 bits of the filter coefficient *a(i)* and multiplies it with an 8-bit input and adds this result to 20-bits of sum and carry from the previous tap and gives out an 8-bit answer. The delay elements between the Wallace tree and the final adder are implemented using C^2MOS [10] latches which also serve to pipeline the design. The PPgen and the booth encoder [11] were implemented in static CMOS. The Wallace tree which is the energy and delay critical module in the whole design was implemented in dual-rail domino logic. The final adder was implemented in single-ended domino logic.

	Energy (pJ)	Delay (ns)	Energy*Delay (10^{-21} J-s)
Standard Domino	1.68	.78	1.31
Mixed Swing Domino	1.27 (-24%)	0.59 (-24%)	0.75 (-43%)

Table 1: Mixed Swing vs. Standard Domino for a 1-bit adder

The filter coefficient *a(i)* is essentially static, i.e. it changes at a slow rate compared to the input data rate. The worst case delay is thus either through the PPgen (Partial Product generator), the Wallace tree and a latch or through the final adder. The precharge time in this design is hidden by having all the domino circuits in the design precharge while the PPgen block is generating the partial products.

4. Experimental Results

Table 2 presents the simulation results for the mixed-swing dual-rail domino multiplier. All simulations were carried out in HSPICE using BSIM1 CMOS models for the HP 0.6µm drawn CMOS process. The simulations were carried out using nominal models at 25° C. Clock skew and clock buffering were not taken into account in these results. The Wallace tree was simulated with the netlist extracted from an actual layout while the rest of the modules were simulated without layout parasitics. The Wallace tree layout was generated automatically using the place and route tool Silicon Ensemble™. The layout for the leaf cells was also generated automatically using LAS™, a device level layout synthesizer.

The worst case delay is through the PPgen block, the Wallace tree and the setup time in the pipeline latch. The Mixed Swing implementation of the adder cells in the Wallace tree reduces delay by 19% and energy by 23%. For the multiplier this translates into a 10% delay decrease with an 18% energy/operation reduction.

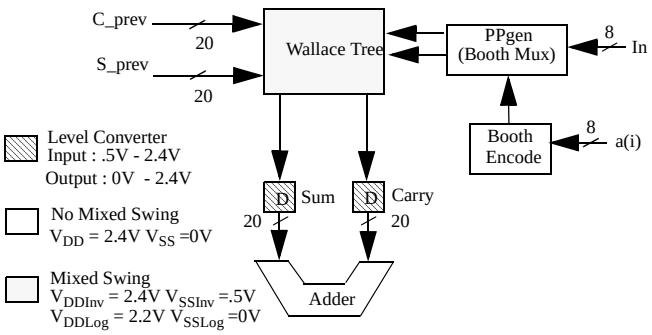

Figure 4. Multiplier Block Diagram

	Mixed energy (pJ)	Mixed delay (ns)	Std. energy (pJ)	Std. delay (ns)
Wallace Tree	69.7 (-23%)	2.5 (-19%)	90.5	3.1
Clock	20.3	-	20.3	-
PP gen	13.2	1.0	13.2	1.0
Latch	20.1	.5	32.7	.3
Final Add	24.0	2.8	24.0	2.8
Total	147.3 (-18%)	4.0 (-10%)	180.7	4.4

Table 2: Energy and Delay Comparison
Mixed Swing Domino vs. Standard Domino

5. Conclusions

In this paper we presented a novel Mixed Swing topology for dual-rail domino logic which can yield simultaneous power and delay reductions. For a simple full adder cell this method results in a 43% reduction in the Energy-Delay product. Energy and delay trends with voltage scaling were also presented for the adder cell. The performance improvements possible with mixed-swing dual-rail domino logic for larger blocks were demonstrated for a 8-bit by 8-bit multiplier. From these simulation experiments the proposed mixed-swing dual-rail domino logic approach appears to offer an interesting avenue for exploration in the design of robust high-performance low-power digital circuit.

6. Acknowledgements

This work was funded in part by DARPA under Order A564, NSF under Grant MIP9408457, and SRC under Contract 068.007.

7. References

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