Variable Supply-Voltage Scheme with 95%-Efficiency DC-DC Converter for MPEG-4 Codec

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ABSTRACT

A variable supply-voltage (VS) scheme with a high power-conversion-efficiency DC-DC converter is presented. A new pulse width modulation (PWM) circuit for the DC-DC converter is proposed to reduce both of power consumption and chip area. The power conversion efficiency reaches up to 95%, and the area is less than half of the conventional design. The VS scheme contains critical path replica circuits of an MPEG-4 codec LSI, and its output voltage is controlled by monitoring delay time of the replica circuits. Consequently the VS scheme can automatically generate minimal internal supply voltage that meets the demand from the operation frequency of an MPEG-4 codec LSI. The advantages of this circuit are successfully demonstrated through fabrication of a test chip using a 0.3μm CMOS technology.

Keywords

DC-DC, low power, low voltage, PWM, variable supply voltage.

1. INTRODUCTION

Lowering the supply voltage $V_{DD}$ is very effective for lowering the power consumption of CMOS LSIs [3][4][7]. However, in system LSIs, many kinds of circuits are integrated in a single chip and some of them cannot be operated in low voltages, for example analog circuits, I/O circuits, and DRAMs. Since several kinds of supply voltages are required in a chip, an integrated DC-DC converter comes to be an important component. Until now, many types of DC-DC converters have been proposed [2][8][12]. However, it is difficult to improve the power conversion efficiency, especially for low-power applications, because the power dissipation of the DC-DC converter itself cannot be neglected compared with that of such low-power application circuits. This paper presents a new circuit of DC-DC converter that can reduce both of power dissipation and chip area. The efficiency reaches up to 95% in the supplying power range of 40-100mW.

Further, the output voltage of this DC-DC converter is variable and adjusted to the optimal voltage by the feedback control [5][11][13]. There are many types of supply-voltage control schemes [1][6][10], but we have chosen the VS scheme [14], which contains critical path replica circuits of LSI and controls its output voltage by monitoring the delay time of them.

A test chip with the replica circuit of an MPEG-4 codec LSI [9] was fabricated using a 0.3μm CMOS technology. The measured results demonstrated the advantages of the VS scheme with the high efficiency DC-DC converter.

The next section presents an overview of the VS scheme. In Section III, new PWM circuit for the DC-DC converter is proposed and compared with the previous works. The experimental results are shown in Section IV. Section V is dedicated to a summary of this paper.

2. VS (Variable Supply-voltage) scheme

The VS (Variable Supply-voltage) scheme is a low-power technique that controls the internal supply-voltages using feedback. The diagram of the system is depicted in Fig.1. It consists of a) a DC-DC converter, b) a speed detector, and c) a timing controller [14]. The DC-DC converter generates an internal supply-voltage $V_{DD}$ from the external power supply...
voltage $V_{DD}$ according to the output of the timing controller, $N$, which is an integer between 0 and 63. The PWM generator is the essential part of the DC-DC converter that generates a waveform whose pulse width is modulated corresponding to the output voltage. The frequency of the modulated waveform, $f_R$, is 0.8 MHz and the duty cycle, $D$, is decided by $N$. The following LC filter filters out the high frequency components of the buffered PWM waveform and provides a stable DC value for the $V_{DDL}$. The timing controller revises $N$ at the rate of $f_R/8$ by adding the previous $N$ and the output of the speed detector whose value is –1, 0 or 1.

The speed detector monitors the delay time of the critical path replica. When $N$ is too small and $V_{DDL}$ is too low for chip operation at $f_{out}$, the speed detector outputs +1. When $N$ is too big and $V_{DDL}$ is too high and extra power is wasted, it outputs -1. When $N$ is appropriate and $V_{DDL}$ is minimal for operation at $f_{out}$, it outputs 0.

Since $V_{DDL}$ is controlled by feedback to be minimal in accordance with the operation frequency $f_{out}$ and ambient temperature, minimal internal supply-voltage is generated to keep extra power from being wasted.

### 3. PWM generator

Many types of PWM generators have been proposed for duty control of DC-DC converters. In this section we will propose a new duty controller and compare it with two conventional types. A 6-bit (64-resolution) PWM generator will be assumed in the following discussion.

One type of the PWM generator is called a “fast clocked counter type” [6]. An example of the schematic diagram is shown in Fig. 2 (a). It has a ring oscillator, a 6-bit counter and a set-reset flip-flop. When the output of the counter equals to $N$, a flip-flop is set. The flip-flop is reset when the output of the counter is “0”. Therefore the duty cycle of $Q$ (the output of the flip-flop) is proportional to $N$. This approach is simple and requires small area. It was employed in the previous VS scheme [14]. However this PWM generator consumes large power, because the oscillation frequency of the ring oscillator is 64 times as fast as that of the output $Q$.

**Figure 1.** VS (Variable Supply-voltage) scheme.

**Figure 2.** (a) Fast clocked counter PWM generator. Another type of the PWM generator is called a “tapped delay line PWM generator” [1] [10]. It has a ring oscillator and uses delay of signal propagation. The PWM generator has a tapped ring oscillator that is made of 64 buffers and an NAND gate. Fig. 2 (b) shows a schematic diagram of the PWM generator. Edge detectors detect edges of rectangle waveforms, and output short pulses. The set-reset flip-flop is set at the edge of A and reset at the edge of B, which is selected by a 64-to-1 MUX according to $N$. Signal $B$ comes latter than signal A. The bigger $N$, the larger the delay from A to B, and the larger is the duty cycle of the output $Q$. This PWM generator dissipates lower power dissipation than the “fast-clocked counter type”. This approach can reduce power dissipation, because the oscillation frequency of the ring oscillator is the same as that of the output signal. Large area is required, however, because it needs the 64-to-1 MUX and the ring oscillator that is composed of as many as 64 buffers.

**Figure 2 (b).** Tapped delay line PWM generator.

A new PWM generator is proposed whose power dissipation is smaller than the “tapped delay line type”, and its pattern area is as small as the “fast clocked counter type”. The schematic diagram of the new circuit is shown in Fig. 2 (c). The PWM generator requires smaller hardware than the “tapped delay line type”; a ring oscillator with 16 inverters instead of the 64 buffers, and a 16-to-1 MUX instead of the 64-to-1 MUX. On the other hand the ring oscillation runs much slower than the “fast clocked counter type”. Therefore proposed circuit has two advantages, small area penalty and low power dissipation.
A timing chart and a truth table of the 4-to-1 MUX are shown in Fig. 3 and Table 1, respectively. S0-S5 represent value of N, S0 corresponding to the LSB, and S5 corresponding to the MSB.

\[ N = S_0 + S_1 \cdot 2 + S_2 \cdot 2^2 + S_3 \cdot 2^3 + S_4 \cdot 2^4 + S_5 \cdot 2^5. \]

One signal is selected by the 16-to-1 MUX from 16 nodes in the ring oscillator as Fig. 2 (c). The signal, B, changes at the point \( S' \), where \( S' \) is represented by

\[ S' = S_1 + S_2 \cdot 2 + S_3 \cdot 2^2 + S_4 \cdot 2^3. \]

The delay of the inverters in the ring oscillator is designed to be twice as large as that of the NAND gate. Even if the delay of the inverters is not exactly twice, only the linearity of the output becomes slightly worse. Since propagation delay of the other elements (an inverter to generate \( \bar{A} \), a 16-to-1 MUX, the 4-to-1 MUX, and an Ex-OR gate) are less than 5% of the inverters and the NAND gate, they can be neglected in the following discussion. In the ring oscillator, rectangle waveforms with duty cycle of 0.5 and cycle time of \( T_R \) are generated. Since a signal passes the 16 inverters and one NAND gate twice in one cycle, the ring oscillation cycle \( T_O \) is given by,

\[ T_R = (16 \cdot 2d + d) \cdot 2 = 66d, \]

where \( 2d \) designates the delay of the inverters. Signal \( \bar{A} \) delays by \( d \) compared to the signal \( A \) because the NAND gate is inserted between \( A \) and \( \bar{A} \). Signal B rises or falls after \( \bar{A} \) falls with a delay, \( S' \cdot 2d \). Since \( X \) is an EXOR (B, S1), rises at \( S' \cdot 2d \), after \( \bar{A} \) falls. The 4-to-1 MUX selects one signal for \( Q \) from \( X, A, \bar{A} \), and \( S5 \) as summarized in the Table 1. Therefore \( Q \) is given as depicted in Fig. 3 according \( S5 \) and \( S0 \).

The pulse width of \( Q, T_H \), is given by

\[ T_H = S_0 \cdot d + S' \cdot 2d + S_5 \cdot \frac{T_R}{2}, \]

which is further calculated by equation (1)-(3) by

\[ T_H = (S_0 + S_1 \cdot 2 + S_2 \cdot 4 + S_3 \cdot 8 + S_4 \cdot 16 + S_5 \cdot 32 + S_5) \cdot d \]

\[ = \begin{cases} N \cdot d & \text{for } N \leq 31 \\ (N+1) \cdot d & \text{for } N \geq 32 \end{cases} \]

From equations (3) (4), the duty cycle \( D \) is given by,
4 Experimental Results

A test chip of the VS circuit is fabricated using a 0.3μm triple-metal CMOS technology. The chip size is 2.0×2.0mm², but the circuits occupy less than 1.0×0.5mm² excluding the PAD area. A die photo is shown in Fig. 5. As for the off-chip LC filter, 33μH inductance and 33μF capacitor are used. Chip features are summarized in Table 2.

![Die photo](image)

**Figure 5. Die photo**

Fig. 6 shows measured the output voltage, $V_{DDL}$, versus $N$ in the DC-DC converter. For feedback stability, $V_{DDL}$ should increase monotonously in response to the increase of $N$.

![Graph](image)

**Figure 6. Measured $V_{DDL}$ versus $N$.**

The proposed PWM generator is compared with the previous two types in Fig. 7 in terms of power dissipations and circuit area. They are all designed using the 0.3μm CMOS technology. The proposed type is the lowest in power dissipation and smallest in the chip area among the three. Measured efficiency of the VS circuit is shown in Fig. 8. The input clock frequency, $f_{in}$, is 40MHz, and $V_{DDL}$ is controlled to be about 2.5V by feedback control. This efficiency includes power loss at not only the DC-DC converter, but also the control circuits for the VS scheme. The efficiency is over 95% in the output power range of between 40mW and 100mW, and over 90% in 19mW-290mW range.

![Comparison graph](image)

**Figure 7. Power, area comparison of PWM generator.**

![Efficiency graph](image)

**Figure 8. Measured power conversion efficiency of VS circuit including DC-DC converter.**

<table>
<thead>
<tr>
<th>Process</th>
<th>0.3μm CMOS triple-metal triple-well</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip size</td>
<td>2.0×2.0mm²</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>Normal 0.55V/-0.70V (NMOS/PMOS)</td>
</tr>
<tr>
<td></td>
<td>Critical-Path Replica 0.10V/-0.10V</td>
</tr>
<tr>
<td></td>
<td>(NMOS/PMOS)</td>
</tr>
<tr>
<td>Output tr. size</td>
<td>12mm/4mm (PMOS/NMOS)</td>
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<tr>
<td>Power except I/O</td>
<td>1.7mW @40MHz</td>
</tr>
<tr>
<td></td>
<td>(operation frequency for CPR)</td>
</tr>
</tbody>
</table>

**Table 2. Chip features.**
5 Conclusion

The VS scheme with 95% efficiency DC-DC converter has been developed and implemented using the 0.3μm CMOS technology. The proposed PWM generator reduces both of power consumption and chip area to less than half of the previous design. The VS scheme with the proposed PWM generator has accomplished over 95% conversion efficiency in the range of 40-100mW, and over 90% in the range of 19-290mW. It is demonstrated that output voltage of the VS circuit varies in response to the operation frequency of the chip, and the output voltage is sufficiently inside and closely to the lower-limit of the pass region in the shmoo plot of the MPEG-4 codec LSI. The VS scheme is promising for low-power applications, especially for low-power system LSIs.

6 ACKNOWLEDGMENTS

The authors would like to thank Masafumi Takahashi, Fumitoshi Hatori, Mototsugu Hamada, Tsuyoshi Nishikawa, Hideho Arakida, Tetsuya Fujita, Akihiko Chiba, Yoshihiro Terazawa, Fumihiko Sano, and Yoshinori Watanabe for their contributions to this paper.

7 REFERENCES


