A Low Energy Architecture for Fast PN Acquisition

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1. ABSTRACT

Spread spectrum systems are being widely deployed today and are becoming more prevalent as most next-generation wireless systems are adopting it for their common air interface. These systems include the digital cellular IS-95A/B/C, IEEE 802.11 wireless local area networks, as well as third-generation wideband code-division multiple access systems. In spread-spectrum systems, the receiver must synchronize on to the transmitted pseudo-noise (PN) code to obtain the improvement performance achieved through spreading. Since PN acquisition must process the spread-spectrum signal at a speed much faster than the transmitted data rate, its energy consumption can become significant and should be minimized for portable applications. Typically, either matched filters or serial correlators are used to acquire the PN code timing. This paper describes a hybrid PN acquisition architecture which employs both matched filters and serial correlators to achieve a lower energy consumption and fast acquisition time as compared to the traditional approaches of using either matched filters or serial correlators alone. The hybrid architecture has been implemented in RTL VHDL and synthesized down to gate level in 0.5-micron CMOS library. Synthesis results show a factor of four reduction in energy for the hybrid scheme as compared to the matched filters architecture and a factor of two reduction in energy as compared to the serial architecture.

1.1 Keywords

Low Energy, PN Acquisition, Spread Spectrum.

2. INTRODUCTION

Today, wireless systems based on spread-spectrum are growing rapidly. These systems include the IS-95 digital cellular system, IEEE 802.11 wireless local area networks (WLAN), and the next generation wideband code-division multiple access (WCDMA) systems. Spread-spectrum transmission technique employs a pseudo-noise (PN) code to spread the user data to a much wider transmission bandwidth to improve link quality. In all of these systems, the portable device must synchronize the received PN code to a locally generated code in order to demodulate the transmitted data. This essential function is performed by the PN acquisition circuits residing in the digital receiver. The PN acquisition circuits process the spread-spectrum signal at a speed much faster than the transmitted data rate. As a consequence, acquisition energy consumption can become significant and should be minimized for portable applications. Furthermore, PN acquisition introduces system overhead such as call-setup delay in circuit-switched networks and increased packet header size for packet-switched networks. To reduce the overhead, the time needed to acquire the PN should be made as short as possible.

To modulate a spread-spectrum signal, data bits are multiplied with a wideband periodic PN sequence (or code), that is the PN sequence is clocked at a much faster rate than the data rate. Such sequences are usually binary and each binary bit in the sequence is called a *chip*. A sequence of these chips ordered in a pseudo-random manner gives the PN codes noise-like characteristics, hence the name *pseudo-noise*. Each data bit is spread over that length and the sequence length is often referred to as the processing gain.

Since the chip sequence is periodic, its timing can be detected by the receiver through a correlation process with respect to a locally generated PN code. The PN acquisition loop performs the correlation to estimate the phase delay, introduced by the channel on the transmitted PN code. The locally generated PN code is then realigned to eliminate the timing offset introduced by the channel. The correlation process exploits the autocorrelation property of the PN code, which displays a periodic peak with a period equal to that of the PN code. The PN acquisition loop detects the autocorrelation peak, and thus the code phase delay, by using a threshold to distinguish between the peak and the sidelobes present in the autocorrelation. The receiver then

demodulates the data bits by multiplying the received sequence with the locally generated sequence that has been time aligned by the PN acquisition circuits.

To compute the autocorrelation function, either matched filters [3] or serial correlators [1] can be used. The matched filters compute values for the autocorrelation function after each chip duration while serial correlators produce a value after each period of a data bit. Since a chip duration is much shorter than a data bit duration, the matched filters compute the autocorrelation values much faster than serial correlators. Consequently, the acquisition time, the amount of time it takes to find the autocorrelation peak and thus the alignment of PN sequences, is much shorter for a matched filter design than serial. However, a matched filter design requires significantly higher complexity and power than a serial correlator.

This paper describes a hybrid PN acquisition architecture which employs both a matched filter and a serial correlator to achieve a two to four fold reduction in energy consumption as compared to traditional approaches using a matched filter [3] or serial correlator alone [1]. In addition, the hybrid design achieves the low energy performance without sacrificing the acquisition time, which remains equal to that of matched filters. The rest of the paper is organized as follows. Section 3 describes the hybrid architecture. Section 4 shows detailed analysis in the amount of energy reduction attainable through the proposed architecture. Section 5 shows the simulation results based on a synthesized VHDL design using a 0.5-micron CMOS library.

3. HYBRID ARCHITECTURE

Figure 1 shows the hybrid PN acquisition architecture that employs both matched filters and serial correlators. Because carrier phase is unknown prior to PN acquisition, the hybrid design uses a noncoherent receiver. The noncoherent design requires an In-phase (I) and a Quadrature (Q) channel, thus the matched filters and serial correlators are instantiated once for each I and Q channel. The autocorrelation values from noncoherent detection are combined using a square-law envelope detector.

Due to the presence of noise and fading in the channel, an estimate of the PN code phase based on one period of the autocorrelation is usually unreliable. For better acquisition performance, a double dwell scheme, where each dwell refers to each estimation stage, is preferred over a single dwell scheme [5]. The second dwell is activated after the first dwell has made an estimate on the autocorrelation peak. The second dwell then averages the autocorrelation values at the estimated code phase over many PN code periods. From Figure 1, we can see that the second dwell averages the value of the square-law envelope detector output whereas the first dwell performs no averaging on the envelope value. This additional averaging makes the second dwell estimate much more reliable than that of the first dwell. The first dwell, however, is made shorter to improve the acquisition time.

The key to low energy dissipation in the hybrid architecture is to use low power serial correlators during the second dwell while during the first dwell the higher power matched filters are used so that a fast acquisition time can be maintained. In contrast, in the matched filters only approach, the filters are also used for the second dwell. Since the second dwell averages the autocorrelation value at a single code phase over many bits, the matched filters dissipate more energy than necessary. In the serial correlators only approach, each value of the autocorrelation function is computed at the data rate, which is much slower

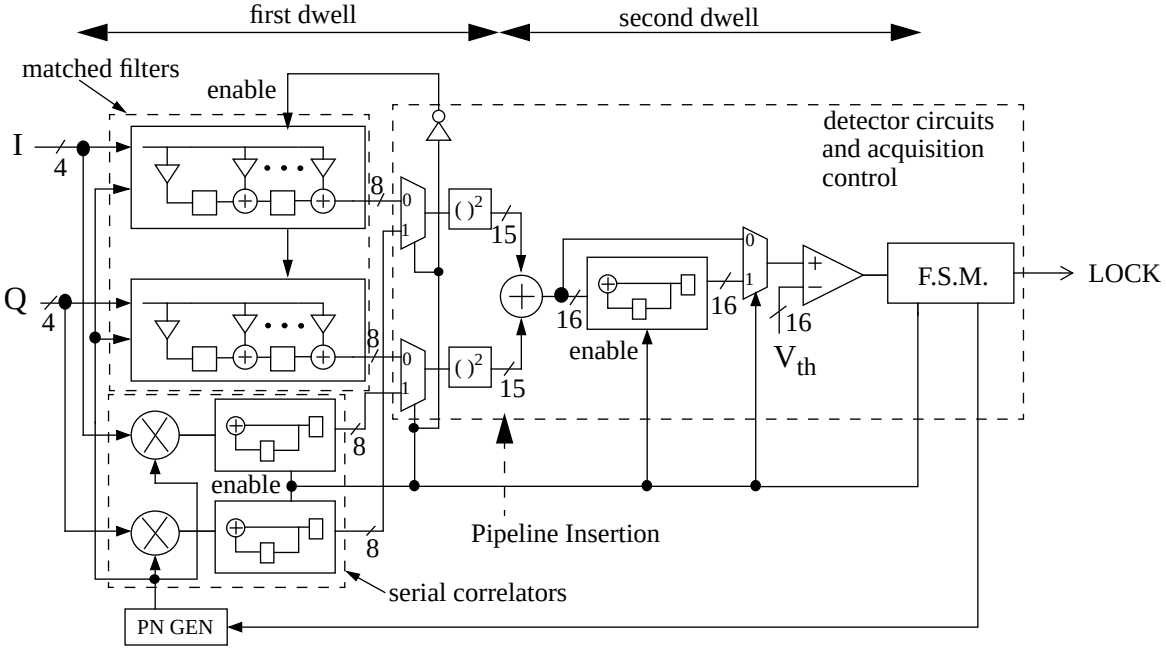

Figure 1. Hybrid PN Acquisition Architecture

compared to the chipping rate that the matched filters operate at. Therefore, the serial correlators have a long PN acquisition time even though they are low power components.

One of two algorithms can be chosen to detect the results of the autocorrelation function in the first dwell of the hybrid or matched filters architecture. One method is to find the first value of the autocorrelation function that appears at the comparator which exceeds the preset threshold. Another method is to find the sample that is the maximum value in one period of the autocorrelation function. This paper assumes that the latter method is adopted.

A prerequisite for the hybrid architecture is that the serial correlator should be equivalent to a matched filter so that it can be substituted during the second dwell. A digital matched filter output with an impulse response $h(n) = c(N-n)$, where $c(n)$ are the filter coefficients, is described below;

$$y(n) = \frac{1}{N} \sum_{k = n-N+1}^{n} x(k)c(k-n+N) \qquad (1)$$

where *x(k)* are the input samples. When $y(n)$ is sampled at integer multiples of N, the outputs are identical to that of a serial correlator which dump outputs at the correct phase. In other words at $n = N$,

$$y(N) = \frac{1}{N} \sum_{k=1}^{N} x(k)c(k). \qquad (2)$$

Equation (2) is, by definition, the operations performed by a serial correlator. Realizing the equivalence of a serial correlator to sampled outputs of a matched filter, we can replace the matched filters' operations by serial correlators during the second dwell. By doing so, the high power dissipation of the matched filters is minimized. The hybrid, though, still takes advantage of the fast acquisition performance of the matched filters by employing them for the first dwell to maintain a high overall system performance. The next section describes the analysis on the amount of energy reduction that can be achieved with the hybrid architecture.

4. ANALYTICAL ENERGY EXPRESSIONS

Energy dissipation is defined as $E = \int_0^T P(t)dt$ where *P(t)* is the power dissipation function. The average energy dissipation in the PN acquisition loops can be found by integrating the average power dissipation function to the average acquisition time.

$$E_k = \int_0^{\overline{T_{acq,k}}} P_k(t)dt \qquad (3)$$

where k = serial (ser), matched filter (MF), or hybrid, $\overline{T_{acq,k}}$ and $P_k(t)$ are the average acquisition time and the average power dissipation function of architecture k, respectively.

Since power dissipation for serial and matched filter architectures is nearly constant for the entire PN acquisition duration, their average energy dissipation can be simplified to

$$E_k = P_k\overline{T_{acq,k}}\ ,\ k = \textit{serial (ser), matched filter (MF)} \qquad (4)$$

For the hybrid architecture, the average energy dissipation is different at each dwell stage of the acquisition process, thus

$$E_{hybrid} = P_{MF}[(\text{Total First Dwell Time}) + LT_c] + P_{ser}[\text{Total Second Dwell Time}] \qquad (5)$$

where L is the processing gain in number of chips and T_c is one chip duration. The additional LT_c term added to the first dwell length in (5) represents an assumed overhead used by the matched filters for the first dwell. This overhead is an assumption that the implementation of a double dwell PN acquisition loop requires additional time to switch from the first to the second dwell stage.

In order to find the energy dissipation, the average acquisition time must be known. Under the assumption of high SNR, $\overline{T_{acq,ser}} \approx \tau_1\frac{L}{2} + \tau_2$ [2][1], where τ_1 and τ_2 are the first and second dwell durations. On the other hand, the hybrid and the matched filter architectures yield $\overline{T_{acq,hybrid}} \approx (\tau_1 + LT_c) + \tau_2$ [5][2]. With $\overline{T_{acq,hybrid}}$ known, (5) is expressed as

$$E_{hybrid} = P_{MF}(\tau_1 + LT_c) + P_{ser}\tau_2 \qquad (6)$$

The matched filter architecture provides faster acquisition than the serial method by sacrificing more complexity and higher power dissipation. To compare energy dissipation of these two architectures, we derive expressions for the ratio of their average energy dissipations. The ratio of average energy dissipation of the serial PN acquisition loop to the matched filter design is

$$\frac{E_{ser}}{E_{MF}} = \frac{((L/2)\tau_1 + \tau_2)P_{ser}}{(\tau_1 + LT_c + \tau_2)P_{MF}} \qquad (7)$$

(7) can be simplified further by using the following substitutions. Let

$$P_{MF} = P_{other} + P_{filters} \qquad (8)$$
$$P_{filters} \approx LP_{cors}$$
$$P_{ser} = P_{other} + P_{cors}$$

where P_{other} is the power consumption for the squarer circuits, the second dwell accumulator, the comparator, the

muxes, and the state machine summed together, as indicated in Figure 1, P_{cors} is the power for the I and Q channel correlators as shown in Figure 1, and $P_{filters}$ is the power for the I and Q channel matched filters. Due to the circuitry similarities between a correlator and a tap in the matched filter, $P_{filters} \approx LP_{cors}$ is a sufficient assumption for analysis. Moreover, we can also let

$$\begin{aligned} \tau_1 &= K_1 L T_c \\ \tau_2 &= K_2 L T_c \end{aligned} \tag{9}$$

where K_1 and K_2 are the number of bits used in the first and second dwell, respectively. K_1 and K_2 are usually constant as processing gain changes. Substituting (8) and (9) into (7), we arrive at

$$\frac{E_{ser}}{E_{MF}} = \frac{(K_1/2 + K_2/L)P_{ser}}{(K_1 + K_2 + 1)(P_{cor} + P_{other}/L)} \tag{10}$$

Since hardware complexity and acquisition time are significant for large processing gains, which are often used in practical applications, the energy ratio for large L is of interest to observe.

$$\text{Large } L, \quad \frac{E_{ser}}{E_{MF}} \to \frac{P_{ser}K_1}{2(1 + K_1 + K_2)P_{cors}} = \frac{(1 + P_{other}/P_{cors})K_1}{2(1 + K_1 + K_2)} \tag{11}$$

In order to prevent frequent false alarms during PN acquisition, the second dwell length K_2 is always much larger than K_1 [5]. To satisfy the condition that $K_2 \gg K_1$ [5], we choose an integer such that K_2 is at least ten times K_1. For implementation convenience, we set $K_2 = 16$ and $K_1 = 1$ which are integer powers of base 2. From the architecture diagram in Figure 1, we estimate that the complexity of other circuits is about three times larger than the correlators alone. Then setting $P_{other}/P_{cors} = 3$, $K_1 = 1$ and $K_2 = 16$, (11) indicates that $E_{ser}/E_{MF} \to 1/9$, that is the matched filter architecture consumes 9 times more energy than the serial architecture.

The hybrid method, on the other hand, is designed to acquire just as quickly as the matched filters' architecture but dissipates less energy. The expression for the energy ratio of the hybrid design to the matched filters' architecture is shown below.

$$\frac{E_{hybrid}}{E_{MF}} = \frac{(\tau_1 + LT_c)P_{MF} + \tau_2 P_{ser}}{(\tau_1 + LT_c + \tau_2)P_{MF}} = \frac{\tau_1 + LT_c + (\tau_2 P_{ser})/P_{MF}}{\tau_1 + LT_c + \tau_2} \tag{12}$$

Once again, substituting (8) and (9) into (12), we arrive at

$$\text{Large } L, \quad \frac{E_{hybrid}}{E_{MF}} \to \frac{K_1 + 1}{K_1 + K_2 + 1} \tag{13}$$

(13) shows that matched filter architecture will always dissipate more energy than the hybrid method because K_2 is always positive. For example, using $K_1 = 1$ and $K_2 = 16$, (13) reduces to $E_{hybrid}/E_{MF} \to 1/9$. We will see in simulations that even though an ideal savings of 9 times more energy is not achieved, a significant energy savings can still be attained by using the hybrid architecture.

The energy ratio between hybrid and serial architecture is

$$\frac{E_{ser}}{E_{hybrid}} = \frac{((L/2)\tau_1 + \tau_2)P_{ser}}{(\tau_1 + LT_c)P_{MF} + \tau_2 P_{ser}} \tag{14}$$

By substituting (8) and (9) into (14) and setting K_1 to one bit duration, (14) simplifies to

$$\text{Large } L, \quad \frac{E_{ser}}{E_{hybrid}} \to \frac{P_{ser}}{4P_{cors}} \tag{15}$$

Assuming that $P_{other}/P_{cors} = 3$ and using results from (8), $E_{ser}/E_{hybrid} \to 1$. That means the hybrid architecture only dissipates as much energy as a serial correlator design but its acquisition time is as short as that of matched filters. As we will see from layout simulations, the ratio E_{ser}/E_{hybrid} will actually be greater than one.

5. SIMULATED ENERGY RESULTS

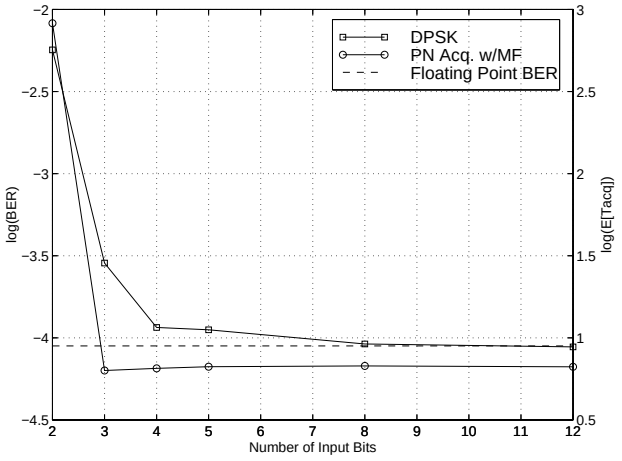

Figure 2. Fixed Point Simulations (chip to noise ratio = -5 dB, *L*=31)

To simulate the average power dissipation at the implementation level, the bus width of the datapaths must be determined. Moreover, circuit complexity and power dissipation depends on the number of input bits. This is

especially true for the matched filters which have many taps and increasing the input bus width by even one bit will affect all the taps and thus the total complexity. Because quantization is a nonlinear process, we rely on system simulations to determine the minimum number of input bits required for comparable performance to a non-quantized architecture. Fixed point simulations in Figure 2 indicates that using a 4 bit input bus will yield both adequate acquisition time and BER. The quantization constraints on other internal datapaths are indicated in Figure 1.

5.1 VHDL Implementation

The RTL VHDL describing the hybrid PN acquisition loop is optimized in Synopsys and synthesized to a HP 0.5µm CMOS technology. The optimized netlist is then fed into the *Epoch*™ compiler to produce an IC layout. In addition, power estimation is also performed using *Epoch*™ after layout is completed. The design process is shown in Figure 3 and the resulting IC performance is summarized in Table 1.

Table 1: Design Characteristics

Clock rate	20 MHz
Vdd	3.3 Volts
Area	4.8mm x 5.1 mm
No. of Gates	39,000

The final layout of the PN acquisition loop is targeted for 20 MHz operation. A pipeline is inserted in the envelope detector circuitry, as shown in Figure 1 to meet the 50 ns clock cycle constraint. The matched filters were synthesized with 126 taps but when selected for lower processing gains all of the 126 taps are still enabled even though some taps are not used for actual computations at lower processing gains. In general, the unused taps may be turned off to save even more power. In power simulations, we assume 1 sample/chip operation so that we can compare to the analytical energy dissipation results.

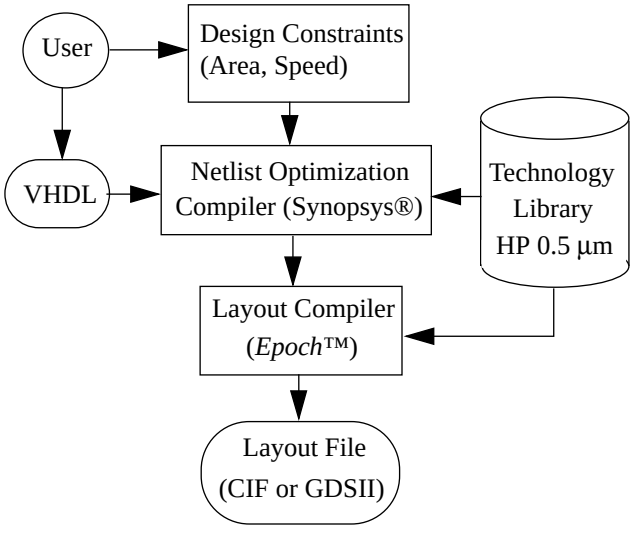

Figure 3. Synthesis Methodology

5.2 Simulation Results

To find the energy dissipation through estimated average power consumption, we use *Epoch*™ to estimate power from layout results. The parameters used to estimate the power dissipation are set as follows: clock frequency is 20 MHz, the inputs are assumed to switch on every other clock edge, and the maximum supply voltage drop is 0.15 volts. Table 2 shows the estimated power dissipation results. Each power estimate is inclusive of components for both the I and Q channel. Because the entire matched filter is enabled even for lower processing gains, there is only one power estimate for $P_{filters}$.

Table 2: Estimated Power

P_{cors}	$P_{filters}$	P_{ser}	P_{other}
1.867 mW	89.716 mW	15.7 mW	13.83 mW

With the power consumption of the matched filter and serial correlator modules, we can calculate and plot the energy dissipation for different architectures against processing gain. Using equations (4) and (5), and setting $\tau_1=LT_c$ and $\tau_2=16LT_c$ (same parameters as analysis), the average energy dissipation versus processing gain is plotted in Figure 4.

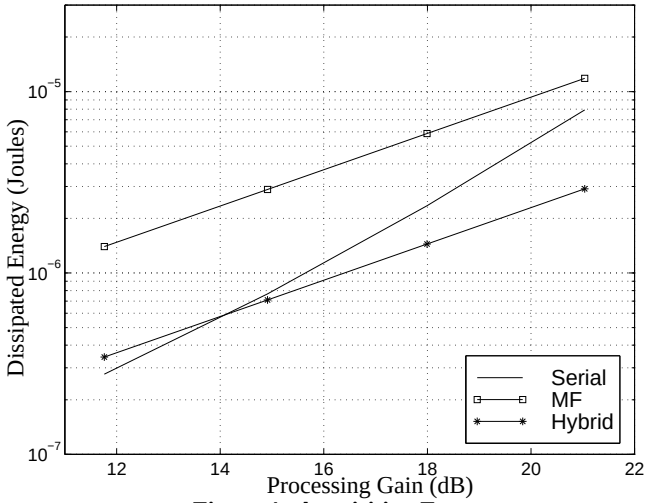

Figure 4. Acquisition Energy

Figure 4 shows that by extrapolating the energy dissipation for the serial and matched filter architectures, the serial will actually dissipate more energy than the matched filter at much higher processing gains. This result does not matched the expression found in (11) because we assumed that $P_{filters} = LP_{cors}$ and $P_{other}/P_{cors} = 3$ in analysis. Simulation results actually show that $P_{filters} \approx 40P_{cors}$ for $L = 126$ and $P_{other}/P_{cors} \approx 7$. The discrepancy between $P_{filters}$ and simulated value is caused by additional circuitry in each correlator as compared to a tap in the filter. For example, each correlator contains dump registers and

counters to keep track of the dump intervals, which are not parts of a tap in the filters. In the result for P_{other}, implementation includes the clock buffering into the other circuits. From architecture diagram alone, analysis didn't account for any clock buffering into the other circuits and so the estimated ratio P_{other}/P_{cors} is smaller than simulations. Due to these differences, the observations in Figure 4 should not be extrapolated to match results from equation (11).

The energy savings of the hybrid architecture over the traditional matched filter design is about a factor of four. Analytical approximation from (13) indicates a maximum energy savings of 9 times over the matched filter architecture with the same dwell parameters. This discrepancy is the result of the approximation made in equation (8) where $P_{filters} = LP_{cors}$. The simulation results in Table 2 only indicate a factor of 40 for L = 126, hence the simulation results show a factor of 4 savings in energy consumption by using hybrid architecture over matched filters.

Another interesting result is that the serial correlator method consumes more energy per acquisition as compared to the hybrid architecture when processing gain is over 14 dB. This phenomenon can be explained by substituting $P_{ser} \approx 8P_{cors}$ into equation (16). In this case,

$$\text{Large } L, \quad \frac{E_{ser}}{E_{hybrid}} \rightarrow 2 \tag{16}$$

Analytical results yielded an energy ratio of 1 because P_{other}/P_{cors} is about twice as small as what was obtained from simulations. Simulation results in Figure 4 shows that at 21 dB processing gain, a fairly large L, the serial architecture indeed dissipates about two times more energy than the hybrid architecture.

6. CONCLUSION

We've derived analytical expressions for the ratios of energy dissipation for the different architectures. Analytical results indicate that lower energy dissipation is achieved by using the hybrid method rather than the matched filter scheme. The hybrid PN acquisition architecture yields four times lower energy dissipation than matched filter based designs and it also dissipates less energy than the serial correlator architecture when the processing gain is greater than 14 dB. By realizing that in the second dwell stage of PN acquisition, sampled matched filter outputs are equivalent to serial correlator dump outputs, the hybrid method can be exploited to achieve lower energy dissipation than the designs in which either the matched filter or the serial correlator is used. Moreover, the hybrid architecture also provides fast PN acquisition equivalent to that of matched filters but without any power penalty. Simulation results from actual layouts confirm these conclusions.

7. ACKNOWLEDGEMENTS

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