Fault Modeling and Simulation for Crosstalk in System-on-Chip Interconnects*

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Abstract

System-on-chips (SOCs) using ultra deep sub-micron (DSM) technologies and GHz clock frequencies have been predicted by the 1997 SIA Road Map. Recent studies [3,4], as well as experiments reported in this paper, show significant crosstalk effects in long on-chip interconnects of GHz DSM chips. Recognizing the importance of high-speed, reliable interconnects in GHz SOCs, we address in this paper the problem of testing for glitch and delay errors caused by crosstalk in buses and interconnects between components of a SOC.

Since it is not possible to explicitly test for all the possible process variations and defects that can lead to crosstalk errors in SOC interconnects, we present an abstract model, Maximum Aggressor (MA) fault model, and its test requirements. The attractiveness of the model is that it can abstract crosstalk defects in interconnects with a linear number of faults, while the corresponding MA tests provide complete coverage for all physical level defects related to cross-coupling capacitance between the interconnects. A SPICE-level fault simulation methodology is presented which allows simulation of a small subset of the potentially exponential number of defects. The simulation methodology also enables validation of the proposed fault model and the resulting test set.

1 Introduction

With deep sub-micron technology and clock frequencies in the GHz range, signal integrity problems, due to increasing cross-coupling capacitance and mutual inductance, will have significant adverse effect on the proper functioning and performance of VLSI systems. Several design techniques, including physical design [1,2] and analysis tools [3,4,5,6], are being developed to help design for margin and minimize signal integrity problems. However, the amount of over design may be prohibitive. Moreover, it is impossible to anticipate in advance, process variations and manufacturing defects that may significantly aggravate the cross-coupling effects. Hence, the need to test for manufacturing defects leading to signal integrity problems.

Traditionally in the digital domain, device defects are modeled with abstractions such as stuck-at-faults. However, with the emergence of previously negligible EM effects that introduce analog behavior, test methodology based on earlier models can not accurately measure circuit performance. The new effects manifest themselves in the form of self-induced and crosstalk noise. Developing a methodology for exciting and detecting faults related to signal integrity problems requires closer examination of the underlying physics involved.

1.1 Crosstalk Effects in Interconnects

Figure 1 illustrates a circuit model of the elements influencing the interaction of two adjacent interconnects (Y1, Y2) running in parallel. The model contains distributed values of capacitance (C1, C2), resistance (R1, R2) and inductance (L1, L2) of each line, cross-coupled capacitance (CC), and mutual inductance (M_{12}). Also included are drivers with a characteristic "ON" resistance (R_{ON}) and capacitive loads (C_{L1}, C_{L2}) for each line.

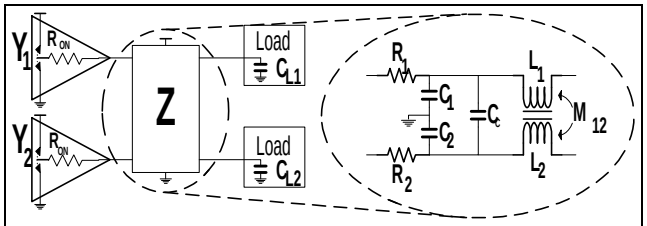

Figure 1 Circuit model for adjacent interconnects.

For sub-micron size processes, driver resistance (R_{ON}), line resistance (R_1, R_2), line capacitance (C_1, C_2), and load capacitance (C_{L1}, C_{L2}) dominate circuit behavior. With the use of simple static models such as lumped-sum and Elmore-delay, their effect on signal delay can be accurately modeled and compensated for during design.

However, for technology on the deep sub-micron scale, other intrinsic properties become equally important. Analysis has shown that cross-coupled capacitance (C_C) becomes a considerable contributor to problems with signal integrity [3,4,7,8]. Similar to cross-coupled capacitance, it is illustrated in [9] that for feature sizes in DSM technology, line inductance (L_1, L_2) and mutual inductance (M_{12}), may also contribute to the noise mixture. The increase of these parameters can be attributed to the decrease in spacing between conductors, the increase of height to width ratio of each conductor, the increase of length for which conductors may run adjacent to each other, and the increase in density due to the increase in metal layers.

In general, the degree of crosstalk depends on several factors. Attributes such as drive strength (R_{ON}), line length, clock speed, skew, driver balance, load to load balance, and impedance matching all contribute to the degrees in which crosstalk can vary. In order to avoid crosstalk noise, analysis with the aforementioned parameters introduced into the model is required during the design phase.

However, even if crosstalk noise is minimized during design, process variations and defects during manufacturing may introduce excessive cross-coupling capacitance and inductance between interconnects, resulting in increased noise. For example, manufacturing defects can introduce new factors such as bridging resistance and floating nets. Figure 2 illustrates the effect of a floating net Y_3 on the cross-coupled capacitance of two adjacent nets, Y_1 and Y_2. The dotted lines represent electric field. If Y_3 becomes floating due to a manufacturing problem, the Y_1/Y_3 capacitance and the Y_2/Y_3 capacitance are effectively coupled

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between Y_1 and Y_2, thus increasing the overall coupling capacitance between Y_1 and Y_2.

The adverse effects of increased cross-coupling capacitance and inductance on signal integrity can be threefold. When cross-coupled capacitance becomes a first order parameter between two bus lines, two basic signal anomalies can take place as a result to step inputs. When one signal is switched (for example, Y_1 switched high) and the other is driven steady (Y_2 driven low) the energy transfer through C_C results in a voltage glitch on the steady signal (Y_2). This is shown in Figure 3(a).

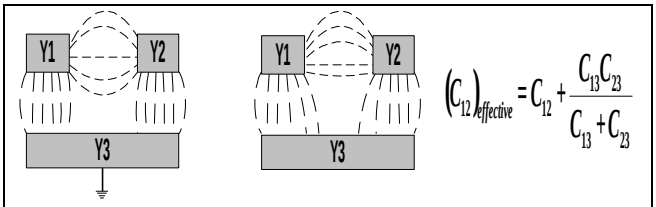


Figure 2 Effect of a floating conductor on cross-coupled capacitance [10].

The second anomaly, when the two lines are switched to opposite values (for example, Y_1 switched high and Y_2 switched low), the result is an increase in transition time, as shown in Figure 3(b).

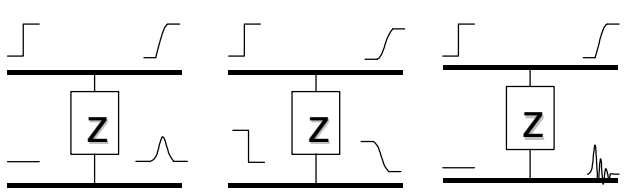


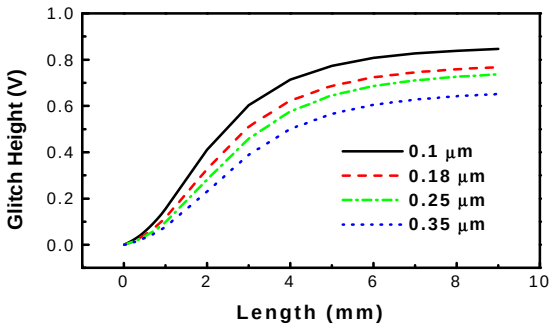
Figure 3 (a) Glitch , (b) Delay, and (c) Oscillations

When inductance is combined with the other elements of the circuit model, the voltage relationship generally results in a high-order differential equation. In addition to glitches and delays, the solution may result in damped voltage oscillations superimposed on top of a glitch or delay, as illustrated in Figure 3(c). If the damping is large enough, the effects of this third case may be approximated by one of the first two cases.

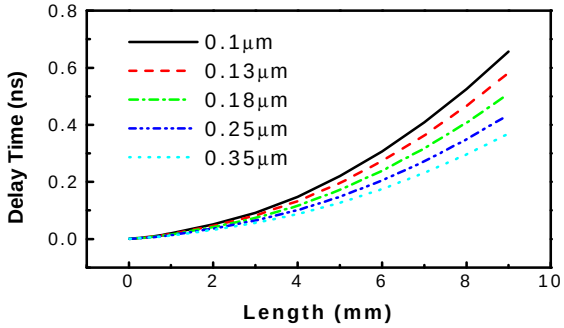
1.2 Focus Motivation

Using HSPICE [16] and technology parameters listed in the SIA Road Map [4], we performed several experiments to confirm the length of interconnect and the technology scaling where DSM effects become significant. The experiments were performed using a transmission line model of a 1V, 6-wire interconnect system with wires running in parallel in a single layer and with pulses driven at the inputs with 100ps transition times. Figure 4 shows the magnitude of the DSM noise generated at the output of the middle wire with varying degrees of DSM technology scaling, length of the interconnects, and use of Al or Cu technology.

Figures 4(a) and 4(b) show glitch and delay effects respectively on the middle wire for various wire lengths up to 10mm and technology scaling from 0.35µm down to 0.1µm. In the glitch experiment, the input of the middle wire is held low, while the inputs of the others are transitioned high. For the delay experiment, the input of the middle wire is transitioned low while the inputs of the others are simultaneously transitioned high. As shown in the figures, these experimental results, in agreement with earlier studies [3,4], show significant increase in signal delay and glitch hazards due to cross-coupling capacitance between bus interconnects, the effects becoming significant for wire lengths as short as 2mm in 100 nm technology. These DSM effects will most adversely affect circuits with very low threshold voltage (Figure 4(a)), and very high-performance circuits (Figure 4(b)). For example, Figure 4(b) shows a crosstalk delay of 0.1ns generated by a 3-mm long interconnect system. This delay has a greater impact on the performance of a high-speed system operating at a GHz clock frequency than that of a circuit operating in the MHz.



(a)



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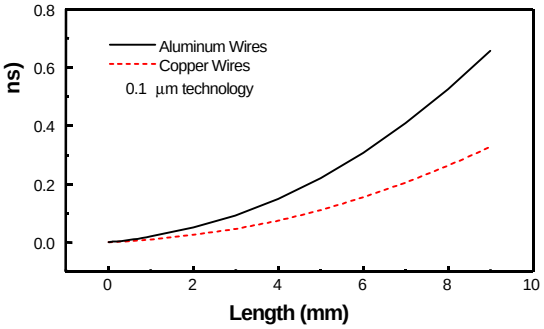

(c)

Figure 4 Variation of DSM effects with changing technology and wire lengths

With the more frequent use of copper technology in DSM circuits, propagation delay of long interconnects is being minimized. Figure 4(c) shows the results of repeating the delay experiment with Cu interconnects, instead of Al interconnects. Though the use of Cu significantly reduces the crosstalk delay effects, the results nevertheless show significant delay effects with longer wires (> 4 mm). Hence, the focus on long interconnects will still be critical as designs migrate to Cu technology.

Not only are the current and future system-on-chips susceptible to DSM noise due to the low voltage and high

performance requirements, but they will be dominated by a large number of very long interconnects and buses needed for the integration and communication of the cores in the chip. Our experiments reported above show the critical need to develop signal integrity test methodologies for long interconnects on low-voltage, high-performance system-on-chips. This is confirmed by the 1997 NTRS objectives of providing high-speed, reliable interconnects and buses in electronic systems in the deep sub-micron era. Consistent with the above findings and the NTRS objectives, we focus on developing test and diagnosis methodologies for crosstalk in buses and global interconnects of a system-on-chip.

1.3 Paper Outline

Several crosstalk extraction and analysis methods [3, 5, 6, 7, 8] have been recently developed; while useful for design validation, they cannot be used for manufacturing testing, and the generation of the simulation vectors is not clear. Research has also started in test pattern generation for crosstalk noise [3,11,12,13]. The techniques have focussed on test generation for glitches and delay faults introduced by cross-coupling capacitance in gate level circuits.

In this work, we address the problem of glitch and delay errors caused by crosstalk defects in global interconnects and buses between components in a system-on-chip. Our goal is to develop a simplified fault model that reduces the necessary test vector set for exciting all possible defects that lead to errors. We also develop a simulation methodology, which allows simulation of a small subset of the potentially exponential number of defects, thus making crosstalk defect simulation at the SPICE level, computationally feasible. The simulation methodology enables us to validate the proposed fault model and evaluate resulting test sets. The remainder of this paper is organized as follows.

Section 2 discusses the underlying physical phenomena behind crosstalk noise and shows how fault models can be used to simplify the description of this behavior. The result is the derivation of a fault model that greatly reduces the required test set to excite and detect crosstalk defects. In section 3 we present a simulation methodology for determining the crosstalk defect coverage of a set of test vectors. The key aspect of our method is that we can use a subset of all possible crosstalk defects to represent the entire defect space, thus greatly reducing the required simulation time. Section 4 presents our simulation results. In these simulations, we use the methodology in section 3 to validate our MAF model and to verify our representative subset of crosstalk defects.

2 Fault Model for Signal Integrity Problems in Interconnects

When considered at the process level, signal integrity problems result from what can be considered as the cumulative behavior of a continuous distributed function of parameters spread over a set of interconnects. The number of possible process variations and other defects (such as a bridging resistance) can be extensive even for the simple two-conductor model shown in the previous section. For wide buses, as shown in Figure 5(a), considering all such variations explicitly is prohibitive.

In an attempt to reduce the complexity of this process level model, we first consider a circuit level model where the cumulative effect of process variations can be described behaviorally by a courser mesh of lumped circuit elements. Each conductor is coupled to every other conductor of the bus through cross-coupling impedance (capacitance and/or inductance) as shown by Z-elements in Figure 5(b). In such a model, we can consider a fault as a Z-element or a combination of Z-elements that, under a set of input transitions, can influence any particular wire adversely. In this manner, a Z element set that is considered a fault, covers any combination of process variations that behave as that particular set of Z elements.

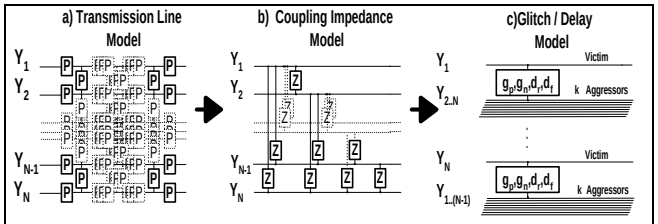

Figure 5 Fault Model Simplification

Although this coupling impedance model simplifies the problem to some extent, two factors still make the size of the fault space large. First, several different possible values of the impedance need to be considered. The second is the necessity to consider all possible subsets of Z-elements from among the $^{N}C_{2}$ Z-elements shown in Figure 5(b).

To address the first problem, we can further abstract to a functional fault model that captures potential glitch and delay effects of out-of-margin Z-elements, as shown in Figure 5(c). In this model, we consider a fault as affecting only one wire, termed victim, at a time. A subset of the remaining wires is designated aggressors, and act collectively to generate an error condition on the victim. To include the general case, in which the drivers of the associated lines are unbalanced, we consider the following four error conditions on the victim. These are positive glitch (g_p), negative glitch (g_n), delay in a rising transition (d_r), and delay in a falling transition (d_f). Each of these is only considered an error condition if they meet some minimum amplitude threshold and duration specified for a given technology. These error criteria are more precisely defined in section 3.2. For an N-wire bus, the total number of possible crosstalk faults (different combinations of aggressors) is $N(2^{N-1})$. Hence, although the above functional model simplifies the problem by eliminating the necessity to explicitly consider impedance values, the number of faults that need to be considered is still $O(2^N)$, a prohibitively high number.

2.1 Maximal Aggressor Fault (MAF) Model

We further reduce the fault set by considering the worst case combinations of coupling impedance among all possible aggressors. In the case of resistive/capacitive coupling, we observe three effects when all aggressor wires are transitioned simultaneously in the same direction.

1) The effect of all capacitance between the victim and aggressors sum constructively.
2) The effect of capacitance between the aggressors is reduced since the voltage between these lines is, ideally, zero for transitions on aggressors in the same direction.
3) The total impedance through the aggressors from the voltage source to the victim is minimal since the impedance of each aggressor adds in parallel.

Thus, we may infer a *Maximal Aggressor Fault (MAF) model* by considering all N-1 aggressors on a bus to be transitioning in the same direction as a fault. As we will see in section 3.3, this conjecture is supported by simulation data used to relate these MAF faults to actual defects.

Unlike the previous model, in the *MAF Model*, there is only one modeled fault for each error on a victim line Y_i, and only one set of transitions that can excite that fault. Figure 6 shows the required transitions on the victim and aggressor wires to excite the four different possible faults for a victim wire Y_i under the maximal aggressor fault model.

Note that when the propagation delay of a long interconnect is integral in designing for setup and hold times, speed up of the signal from a nominal delay is possible, giving rise to two more possible errors conditions and thus two more faults. While our proposed fault model and fault simulation methodology can be extended to crosstalk speed-up errors, we do not explicitly address them in this paper.

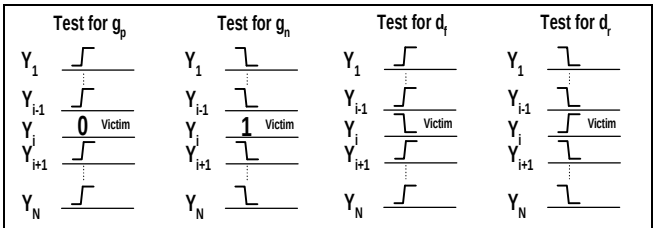

Figure 6 Required Transitions for MAF Model

For an N-line wide set of interconnects, the fault model has 4N faults, and requires 4N two-pattern tests. When the actual defects are capacitive or resistive, the linear number of faults in the maximum aggressor model is sufficient in covering the exponential number of faults in the glitch-delay fault model in figure 4(c), as is illustrated in the next section.

2.2 Relationship between Maximal Aggressor Fault Model and Defect Universe

Figure 6 illustrates the relationship between the MAF model and *crosstalk defects*, which include manufacturing defects and process variations that lead to variations in crosstalk capacitance, resulting in crosstalk errors like glitches and delayed transitions. In deriving the MAF faults, we progressively reduced the number of possible faults by abstracting our model from real physical parameters to circuit elements, to an abstract concept of victim and aggressors, and finally to a subset of these victim and aggressors. In each case, the resulting error conditions, glitches and delays, are the same. In this manner, since each MAF fault excites one of the four possible errors, a set of crosstalk defects that lead to one of these errors is covered by the MAF fault.

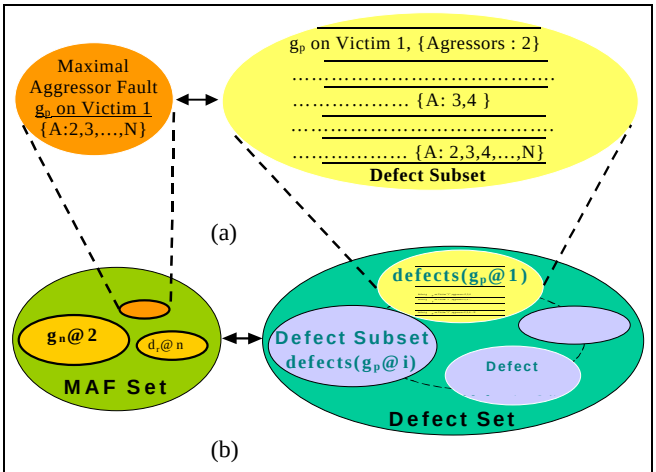

Figure 7 Mapping Relationship of MAFM and Defect Universe.

For example, Figure 7(a) shows that one MAF fault covers all the crosstalk defects that generate positive glitch errors on victim line 1, no matter what the underlying process is. As shown in Figure 7(b), the union of all the defect sets, each defect set generating one of the error types on bus line i, constitutes the crosstalk defect space. Since the set of MAF faults excite all possible glitch and delay errors, they cover all the crosstalk defects that may potentially cause any glitch or delay error on any of the bus lines.

3 Crosstalk simulation

To enable us to validate the proposed MAF model, and evaluate the crosstalk defect coverage obtained by a test set derived using the MAF model, we have developed a crosstalk simulation methodology. In this section, we describe the simulation methodology, which includes extraction of RC parameters from a given set of interconnects, injection of crosstalk defects, SPICE-level simulation of test vectors, and detection of errors. The conditions under which a crosstalk glitch or delayed transition can cause the circuit to malfunction depends upon the characteristics of the bus system and the receivers. Hence, we will describe how errors can be defined in terms of circuit characteristics. As described in Section 2, the number of possible crosstalk defects can be prohibitively large. We describe three key properties exhibited by crosstalk capacitance, which allows the selection of a small number of representative defects, and makes crosstalk defect simulation computationally feasible.

3.1 Simulation Methodology

Our simulation framework is shown in Figure 8. For a given interconnect system, a RC network is generated by using a parasitic extraction tool [14, 15]. A crosstalk defect is injected into the RC network by varying the RC parameters. Next, HSPICE [16] is used to simulate the RC network using test vector pairs from a test set under evaluation. The result of the HSPICE simulation is processed by the Error Monitor to see if the applied test pair has generated the required error condition on the chosen victim line, and thereby detected the defect being simulated. If the defect is not detected, new test pairs from the set are applied until either the defect is detected or all test pairs have been applied. The process of defect injection, SPICE simulation, and error monitoring is repeated for the other defects being simulated to produce the defect coverage for the given set of test vectors.

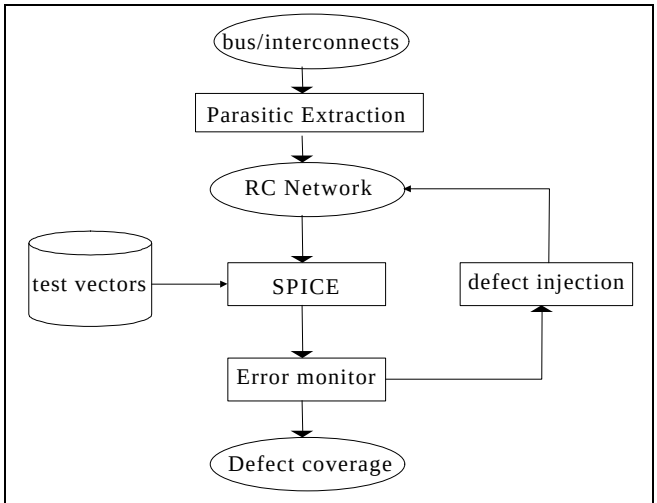

Figure 8 Crosstalk defect simulation.

Since the simulation is performed at the analog level, the error monitor needs to convert the analog output of SPICE to digital signals. Hence, it is necessary to define threshold voltages and time characteristics that will define errors. In addition, the variation of physical defects can be arbitrary and extensive, making it impossible to exhaustively simulate all physical defects

in the RC network. Hence, it is critical to identify a small but representative set of defects whose simulation covers all the defects. In the following sub-sections, we define errors, and propose a representative set of defects.

3.2 Definition of Errors

What constitutes an error is specific to the interconnect characteristics and receivers for a particular technology. The manner in which crosstalk defects cause errors can be formally quantified with the specification of a few signal parameters defined below.

1) $\mathbf{Vp_{th}}$ Threshold voltage above which a positive glitch may cause an error.
2) $\mathbf{Vn_{th}}$ Threshold voltage below which a negative glitch may cause an error.
3) $\mathbf{Vr_{th}}$ Voltage at which a rising delay may cause an error.
4) $\mathbf{Vf_{th}}$ Voltage at which a falling delay may cause an error.
5) $\mathbf{\Delta t_g}$ Minimum time duration for which a glitch amplitude must be beyond its voltage threshold to cause an error.
6) $\mathbf{\Delta t_d}$ Minimum time duration from launch of a signal on a bus to sampling it at the receiver for which a delay can cause an error.

With these parameters defined, we formalize the definition of errors as follows.

1) $\mathbf{g_p}$ *Positive glitch error*: a positive glitch at the receiver of a victim line that rises above Vp_{th} for a duration Δt_g .
2) $\mathbf{g_n}$ *Negative glitch error*: a negative glitch at the receiver of a victim that falls below Vn_{th} for a duration Δt_g .
3) $\mathbf{d_r}$ *Rising delay error*: a delay of Δt_d for which the voltage at the receiver of a victim fails to reach Vr_{th} during a rising transition.
4) $\mathbf{d_f}$ *Falling delay error*: a delay of Δt_d for which the voltage at the receiver of a victim fails to reach Vf_{th} during a falling transition.

3.3 Defect Selection for Simulation

Determining absolute defect coverage for vectors derived from the MAF model involves spice level simulation that incorporates all possible crosstalk defects. However, each of the errors, g_p, g_n, d_r, and d_f, on any victim line can be caused by a very large number of crosstalk defects, making it impossible to simulate all of them. To make crosstalk simulation feasible, we derive a representative subset of these defects that allow us to approximate behavior of the entire defect set and therefore approximate total defect coverage. Via simulation, we demonstrate, that when MAF tests are applied, three properties of signal behavior due to crosstalk defects that allow us to determine this set. These properties follow from the three cross-coupling capacitive / resistive effects, enumerated in the first part of section 3, that led to the MAF model.

Property 1: This property relates interconnect systems with equal totals of cross-coupling capacitance distributions between the victim and all aggressors but with different distributions of the total capacitance amongst the aggressors. *For different distributions of total capacitance among the aggressors, the arrangement that generates the smallest glitch is the one with the entire capacitance between just one aggressor and the victim.* This attribute follows directly from the fact that impedance between the voltage source and the victim decreases as parallel paths are added through additional aggressors. Simulation results of various distributions of the same total capacitance are illustrated in Figure 9a and Figure 9c. Note that the glitch generated by the single aggressor is smaller than the glitches produces by all other distributions of capacitance. Similarly, the single aggressor generates the least delay effect among all the capacitance distributions as shown in Figure 9c. In the figures of both delay and glitch, there is a point when all waveforms intersect and reverse in voltage order. However, as validated by our simulations, we assume that this point is below the error threshold voltage and hence property 1 holds.

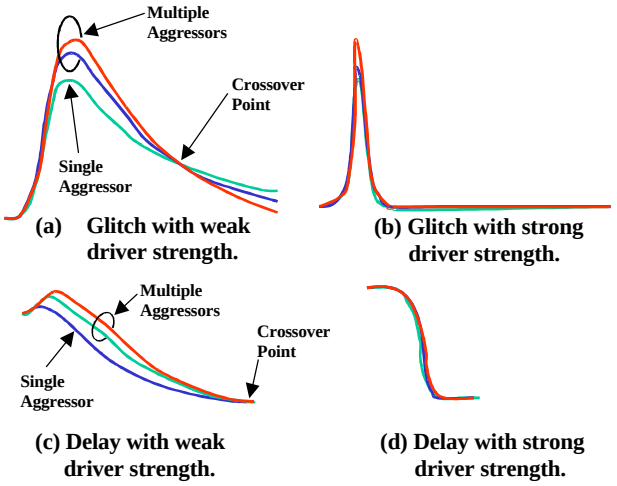

Figure 9 Glitch and delay effects for different driver strengths.

Property 2: *When driver strength is sufficiently high, (driver resistance sufficiently low), the difference in effects (glitch or delay) between different distributions with the same total capacitance, becomes negligible.* This can be attributed to the fact that in the ideal case with zero driver resistance, the resulting distribution is nearly a lumped sum equivalent of the parallel combination of all capacitance. Figure 9b and Figure 9d illustrate this property. The remaining difference between the waveforms can be attributed to line resistance.

Figure 10 plots the differences between glitches of different distributions versus drive strength (transistor width/length ratio). From the figure we see that the differences in the area under the various glitch curves decrease asymptotically as drive strength increases.

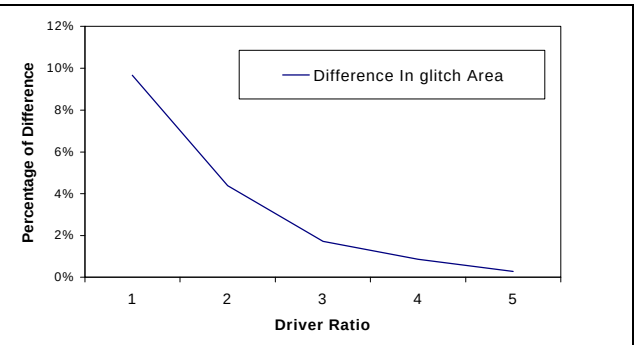

Figure 10 Glitch effect vs. Driver Strength.

Property 3: *Glitch and delay effects increase monotonically as the total cross coupling capacitance between the victim and all the aggressors increases monotonically while keeping the relative proportions from each aggressor constant.* Figure 11 shows the simulation results of a glitch response for increasing summation values of cross-coupled capacitance. A glitch due to lower total

capacitance is completely contained by a glitch due to greater total capacitance.

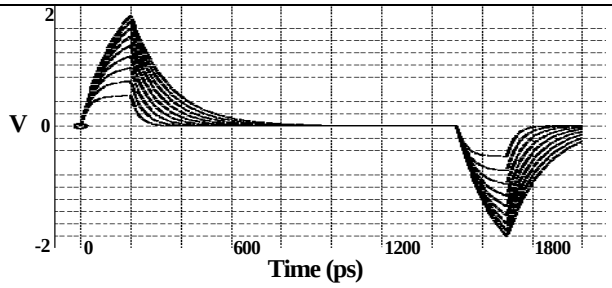

Figure 11 Monotonic increase of glitch effect.

We now relate the value of total cross coupling capacitance to defects and use this value to divide the defect space into subsets. Additionally we show that when MAF vectors are used, each subset can be accurately represented by one defect in the subset.

Consider an interconnect system with the total cross coupling capacitance distributed on only one aggressor. Additionally consider that the total capacitance is such that when the MAF vector for the error type g_p is applied, the glitch generated meets the minimum error thresholds, Vp_{th} and Δt_g, exactly, thus generating an error. The total capacitance for this distribution is denoted C_{th}, the threshold capacitance. From property 1, we deduce that different distributions with the same total capacitance, C_{th}, will also generate an error. Likewise, from property 3, we reason that all distributions with greater total capacitance will also generate an error. With C_{th} , we now have a single parameter to specify a significant population of the defect set.

Though this covers a large number of defects, there are other distributions with equal total capacitance less than C_{th}, that when an MAF test is applied, some distributions generate an error and some do not. If we make a reasonable assumption that the interconnect drivers are designed sufficiently large enough, from property 2, this group of distributions reduces to only those with total capacitance only negligibly less than C_{th}. We thus include these additional distributions in the set of defects covered by C_{th}.

Similarly, we use the same reasoning to show that for the negative glitch, rising delay and falling delay errors, there is a value of C_{th} that is representative for each defect set. Further, when using the MAF test vectors, the defect with the single line distribution and total coupling capacitance equal to C_{th} , covers all other defects.

To determine the threshold capacitance, C_{th}, for a given error type, we simulate a two-line bus using the MAF vectors, iteratively increasing cross-coupled capacitance until the glitch or delay effect meets the error requirements.

4 Experimental Results

Using an example 4-interconnect system, running for 1mm in parallel on a single layer, and in a .1µm process, we validate the MAF model by using the proposed simulation methodology given in Figure 8. For the validation, random crosstalk defects are injected, the interconnect is simulated using the MAFM test patterns and several randomly chosen test patterns, and then monitored for error conditions.

In the previous section, we defined a representative crosstalk defects in terms of a threshold capacitance, C_{th}. For selecting defects in our simulation, we demonstrate the process of determining C_{th}. Through a large number of simulations, we verify the glitches and delays generated using these values are consistent with the three properties we described.

Once C_{th} is determined for each error type, through exhaustive simulation using our methodology, we show that the MAF vectors are sufficient in generating an error for each defect. We also demonstrate the necessity of the MAF vector set by showing that the MAF vectors always generate an error while other vectors fail.

Table 1 shows the error thresholds for the four different error types used in the experiment.

Table 1. Threshold values used for simulation.

Error Type	Error Threshold		Defect Threshold
	V_{th} (mV)	ΔT (ps)	C_{th} (pf)
g_p	300	200	0.8
g_n	700	200	0.8
d_r	500	200	0.85
d_f	500	200	0.85

First, following the procedure in section 3.3, we determine C_{th} for each fault by simulating the 2 wire (single aggressor) model, incrementally increasing the coupling capacitance until the error conditions are met. As an example, selection of C_{th} for the g_p error is illustrated in Figure 12. Capacitance is incrementally increased, and consistent with property 3, the glitch increases monotonically to where it meets the error threshold conditions at 0.8pF. The threshold capacitance values are listed under the *Defect Threshold* column in Table 1.

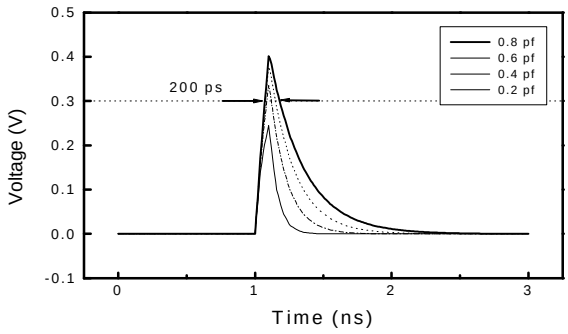

Figure 12 Determination of threshold capacitance.

Then, the circuit is simulated for different defects, which are distributions of capacitance between the victim and the aggressors, A1,A2, and A3, with the total capacitance equal to 0.8pF (C_{th}) in each case. A thousand distributions/defects are simulated with the corresponding MAF vectors. For a few example defects/distributions that were simulated, Table 2 tabulates the peak glitch values, while Figure 13 shows the corresponding glitches for distributions listed in Table 2.

Table 2. Positive glitch for different Cth Distributions.

Defect	C-distribution (pf)			test vector	glitch (mV)
	A1	A2	A3		
D1	0.8	0	0	0000-0111	400
D2	0.2	0.6	0	0000-0111	490
D3	0.3	0.5	0	0000-0111	510
D4	0.4	0.4	0	0000-0111	515
D5	0.3	0.2	0.3	0000-0111	557

As predicted by property 1, Table 2 and Figure 13 show that the smallest glitch value is produced by defect D1, the 2-line distribution, while all other multiple aggressor distributions produce higher glitch voltages, and hence, error conditions, when

triggered with the MAF vectors. Note also, as stated by property 2, that at the threshold voltage of 300mV, there is negligible difference in the duration of the glitches for the different distributions of the capacitance.

Finally, with Cth determined for each error type, we simulate 1000 different defects using our proposed methodology illustrated in (Figure 8). Figure 14 shows the result of applying the MAFM test and four other randomly chosen vector pairs on an arbitrarily chosen defect. This simulation, as well as the simulation of all other defects, shows two characteristics of the MAF tests. First, the MAF tests always generated glitch or delay effects worse than any other randomly selected tests, the effects always meeting the minimum threshold conditions for an error and thus, illustrating that *the MAF vectors were sufficient in covering all crosstalk defects*. Second, while the MAF tests always generated the corresponding error conditions, the other test vectors sometimes failed, demonstrating *the MAF vectors are also necessary for covering the defect*.

In a similar way, we also validated the Maximum Aggressor Fault Model for negative glitch (g_n), rising delay (d_r) and falling delay (d_f).

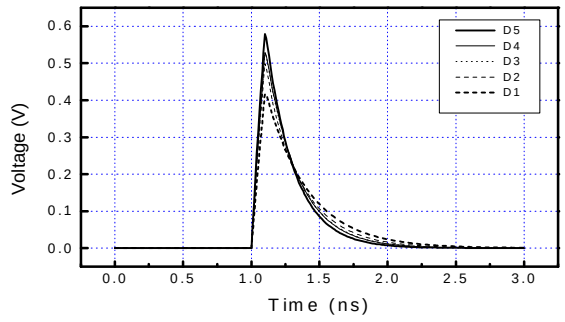

Figure 13 Glitch responses to MAFM vector for different Cth distributions.

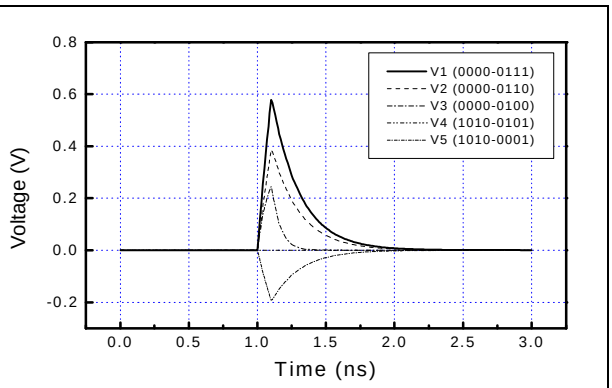

Figure 14 Glitch responses to various test vectors

5 Conclusion

In this paper, we presented the *Maximal Aggressor Fault Model* as a high level representation of physical defects that lead to crosstalk errors on SOC interconnects. Additionally, we developed a simulation methodology for validating our model and for determining coverage of test sets for crosstalk defects. In this process, we demonstrated that the entire crosstalk defect universe can be represented by a small subset of defects, thus making crosstalk defect simulation feasible. We subsequently showed the sufficiency and necessity of the MAF tests in detecting the crosstalk defects. Using the proposed crosstalk fault model and the related tests, we are currently developing a self-testing methodology to enable the at-speed test of SOC interconnects.

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