Embedded Tutorial

Formal Verification Meets Simulation

Presenters: Davil L. Dill,
Stanford University
Stanford, CA
Serdar Tasiran,
University of California
Berkeley, CA

Moderator: Ellen M. Sentovich, Cadence Berkeley Labs., Berkeley, CA

ABSTRACT

This embedded tutorial explores some of the options for verification in the territory between current methods based simulation and emulation, and formal verification. Topics covered will include: coverage metrics and their effectiveness at uncovering bugs, symbolic simulation for partial formal verification, and directed search of a design.