A Scalable Substrate Noise Coupling Model for Mixed-Signal ICs

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***Abstract*—A scalable macromodel for substrate noise coupling in heavily doped substrates has been developed. This model is simple since it requires only four parameters which can readily be extracted from a small number of device simulations or measurements. Once these parameters have been determined the model can be used for *any* spacing between the injection and sensing contacts and for different contact geometries. The scalability of the model with separation and width provides insight into substrate coupling and optimization issues prior to and during the layout phase. The model is validated for a 2μm and a 0.5μm CMOS process where it is shown that the simple model predicts the noise coupling accurately. Measurements from a chip fabricated in a 0.5μm CMOS process show good agreement with the model.**

I. Introduction

Substrate coupling in mixed-signal CMOS ICs can degrade the performance if it is not well characterized. To date, models for substrate coupling are used as part of the final layout extraction and simulation verification. Several techniques have been proposed for analyzing substrate coupling in integrated circuits [1-10]. The substrate models developed are based on finite difference methods [7,10], boundary element methods [3], and polynomial curve fitting methods [2,6]. Reduced-order macromodels can also be obtained using techniques based on AWE or Arnoldi methods [7,9]. These models are difficult to use intuitively as part of the design process.

In this paper, a substrate coupling macromodel is described that can be used during the early stages of design and simulation. For a given process, simple curve fitting is used to determine a few parameters used in the model. This model scales with the substrate contact separation distance and the area of the injector and sensor contacts. It can also be used to determine the substrate coupling between transistors. The paper begins with a description of the general model in Section II for a p-type substrate. In Section III, the scaling of the model with the contact size is described. Section IV extends the model to coupling between n+-p+ contacts. Experimental results are presented in Section V and conclusions are presented in Section VI.

II. Substrate Coupling Macromodels

Substrate coupling models are necessary to accurately predict the coupling between circuits sharing the same substrate. A substrate macromodel which scales directly with the separation, size and shape of the contacts on a die can be used to generate a netlist file for a circuit simulator given the layout and process information as shown in Fig. 1. Such a model can offer insight into the dependence of coupling on sizes, shapes and placement of different structures on the die and can cut down on the overall design time. Further, such models can be used to optimize the placement of structures for improved isolation.

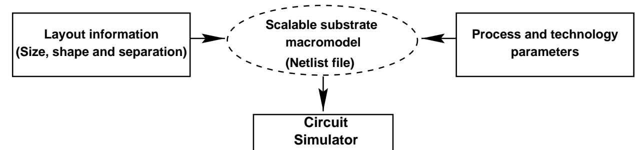

Fig. 1. Generation of a scalable substrate macromodel from layout to be used in a circuit simulator.

For frequencies of a few GHz and below, the substrate can be treated as a resistive network [7]. In Fig. 2(a), the cross section of a typical heavily doped substrate is shown. This structure can be simulated using the device simulator TMA-Medici [11] to determine the coupling between points A and B. The coupling is characterized in terms of Y-parameters whereby an AC voltage is applied at one port and the currents are measured with the other port connected to ground.

Simulations with Medici validate that below 2 GHz, the heavily-doped substrate can be modeled as a lumped resistive network. Simulations also show that for contact spacings of less than 10μm, nearly all the current flows on the surface between the two contacts. However, for a contact spacing greater than 100μm, nearly all the current flows down into the (very low resistive) substrate. This is illustrated in Fig. 2(b) where the current is shown to flow down into the substrate.

The macro model for the substrate for two point contacts on the substrate is shown in Fig. 3(a). Here G_{1_A}, G_{1_B} and G_2 are the conductances. The backplane contact of the substrate is connected to ground. If the contacts are of the same size and shape then $G_{1_A} = G_{1_B} = G_1$. The two port Y-parameters for the substrate macromodel are then given by,

$$Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_1 + G_2 \end{bmatrix} \quad (1)$$

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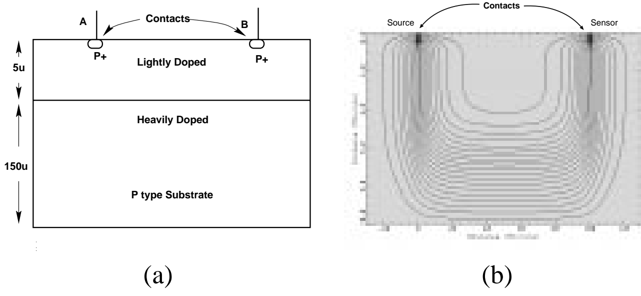

Fig. 2. (a) Cross section of a heavily doped CMOS substrate with point contacts and (b) current flow lines from device simulations for 100μm separation between the injection and sensor contacts.

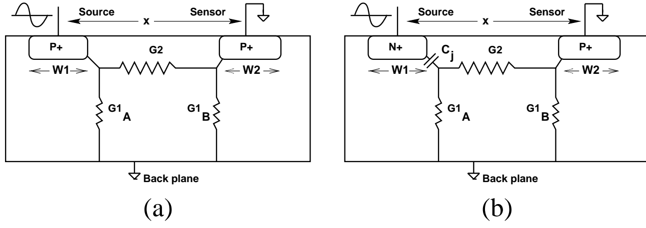

Fig. 3. (a) Macromodel for the substrate when the back plane is grounded. (b) Model for noise coupling between a N-source and P-sensor.

The Z-parameters can be computed by inverting the Y-matrix and are given by:

$$Z = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = Y^{-1} = \frac{1}{\Delta} \begin{bmatrix} G_1 + G_2 & G_2 \\ G_2 & G_1 + G_2 \end{bmatrix} \tag{2}$$

where Δ is the determinant of the two-port Y-matrix and is given by:

$$\Delta = G_1^2 + 2G_1G_2 \tag{3}$$

Solving for z_{11}

$$z_{11} = \frac{G_1 + G_2}{\Delta} = \xi \tag{4}$$

where ξ is a constant [6]. Rearranging this expression:

$$G_1^2 + 2G_1G_2 - \frac{1}{\xi}(G_1 + G_2) = 0 \tag{5}$$

If either G_1 or G_2 is given as a function of distance, the other can be obtained by solving the above equation. From device simulations, increasing the spacing between contacts increases (decreases) the value of $R_2(G_2)$. The actual values of G_1 and G_2 can be determined from 2-D device simulations or measurements. The value of G_2 determined from Medici simulations as a function of contact spacing is shown in Fig. 4(a) for a 0.5μm and a 2μm CMOS process, respectively. The linear dependence on the semilog plot of G_2 can be modeled by an exponential dependence on x:

$$G_2 = \alpha e^{-\beta x} \tag{6}$$

where α and β are constants determined from simulated or measured data. Only two points are needed to obtain relatively accurate results. The accuracy of α and β can be improved with more

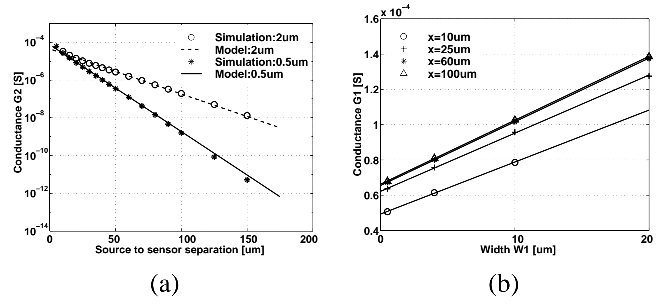

Fig. 4. Comparison of the model for conductance G2 with Medici-2D simulations for (a) 0.5μm CMOS process and for 2μm CMOS process. (b) Variation of conductance G1 with width (W1) for different distances where $W2 = 0.5\mu$m.

data and a nonlinear least-squares fit. This curve fit is shown in Fig. 4(a) and the model matches very well with the simulated data.

The quadratic equation in (5) can be solved for the admittance G_1 where

$$G_1(x) = \frac{1}{\xi} - \frac{1}{2\xi}\phi(x) \tag{7}$$

and

$$\phi(x) = (1 + 2\xi \cdot G_2(x)) - \sqrt{1 + 4\xi^2 \cdot G_2^2(x)} \tag{8}$$

When $x \to \infty$, $G_2(x) \to 0$, $\phi(x) \to 0$ and hence $G_1(x)$ tends to a constant value given by $\frac{1}{\xi}$. In other words, ξ can be extracted from the contact to bulk resitance with all other contacts floating. A comparison of the model with simulations for a 0.5μm and a 2μm CMOS process for G_1 are shown in Fig. 5(a). Additional validation is provided in Fig. 5(b) where y_{11} for the model and Medici-2D simulations have been compared.

Thus one requires the knowledge of α, β and ξ for characterizing the substrate. These three constants can be obtained from three device simulations or from experimental data.

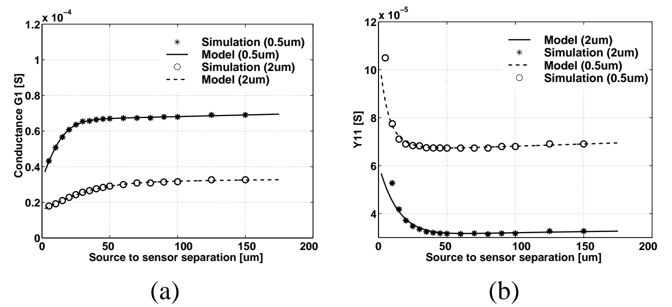

Fig. 5. (a) Comparison of the model for conductance G_1 for 0.5μm and 2μm CMOS processes with Medici-2D simulations. (b) Comparison of the model for admittance parameter y_{11} with Medici-2D simulations for a grounded back plane for 0.5μm and 2μm processes.

III. Scaling the model with contact size

The model described above can be extended to source and sensor contacts with any size. The width of the contacts are W1 and W2 as shown in Fig. 3(a). Simulation of the conductance G_1 with variations in the width W1 produces a linear relationship as seen in Fig. 4(b). For these simulations $W2 = 0.5\mu$m and the other dimension (perpendicular to the direction of the 2-D structure) is

1μm. The line fit to the data is a good prediction of the effect of the scaling. From this plot, it is clear that G_1 is a function of W1 and the spacing x.

G_1 for any contact width W1 is given as:

$$G_1(W1, x) = m(x)W1 + G_1(0, x) \tag{9}$$

where m(x) is the slope of the lines in Fig. 4(b) as a function of the separation distance x. $G_1(0, x)$ is the value of G_1 for a zero contact width.

Fig. 6(a) shows the plot of the slope $m(x)$ with the separation distance between the source and the sensor. It is seen that $m(x)$ has the same shape as G_1 and can actually be modeled in terms of G_1 by including a scaling factor. Therefore,

$$m(x) = \frac{1}{W0} G_1(0, x) \tag{10}$$

where W0 has the same dimensions as width. Fig. 6(b) shows the variation of W0 with the distance x of separation between the source and the sensor. It is clear that the variation in W0 is small and hence it can be assumed to be a constant.

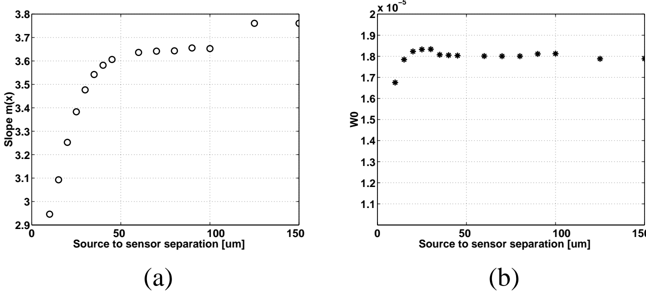

Fig. 6. (a) Plot of the slope *m(x)* of the lines in Fig. 4(b) and (b) W0 as a function of separation x between the source and sensor contacts.

Therefore (9) becomes

$$G_1(W1, x) = G_1(0, x)(1 + \frac{W1}{W0}) \tag{11}$$

Equation (11) indicates that even with a point contact (W1=0) there is a coupling through the substrate.

This result is compared with device simulations in Fig. 7(a). The width W1 is varied while W2 is held constant. The model and simulation data are in good agreement. The conductance G_2 is effectively independent of W1 and W2 as shown in Fig. 7(b) and depends only on the length of the contact (perpendicular to the plane of the 2-D device).

IV. Model for coupling from N+ to P+ contacts

Up to this point, only the coupling between p+ contacts has been modeled. In design, it is desirable to determine the coupling between transistors. Thus, we extend the model to n+-p+ contacts as shown in Fig. 3(b). The n+ in the p-substrate forms a diode, associated with which is a depletion capacitance represented by C_j. This capacitance is incorporated into the general model to accurately model the coupling. Conductances G_1 and G_2 can be extracted from device simulations and are plotted in Fig. 8(a) and (b). The values for G_1 and G_2 from the model for p+-p+ contacts

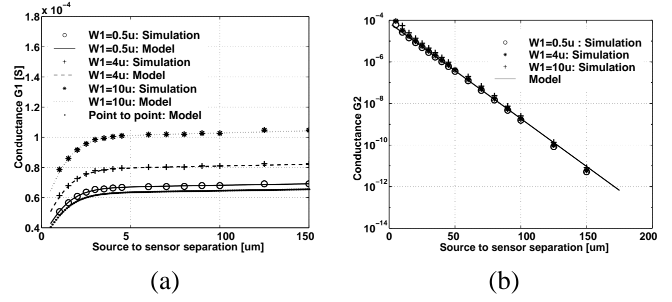

Fig. 7. (a) Comparison of the model with simulation results for conductance G1 for different widths (W1). (b) Comparison of the model with simulation results for conductance G2 for different widths (W1).

are also plotted and it is seen that both the plots are very close, thus validating the model in Fig. 3(b).

To use this model in design, the capacitance need not be explicitly modeled. A SPICE subcircuit can be constructed that models each of the conductances G_1 and G_2. This subcircuit, for example, is then connected to the bulk of an n-channel MOSFET. The junction capacitance of the n+ source node is part of the transistor model and is automatically included in the simulations.

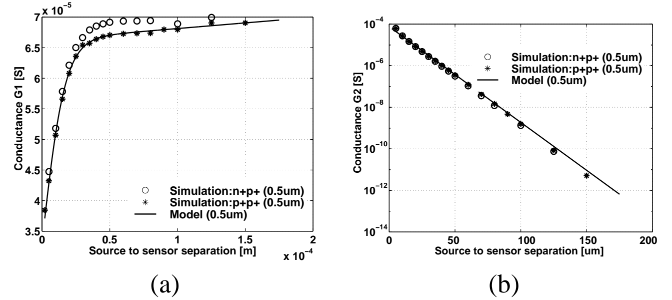

Fig. 8. (a) Comparison of G1 extracted from the n+-p+ case with the model in (7). (b) Comparison of G2 extracted from the n+-p+ case with the model in (6).

V. Experimental Results

The layout for the test chip fabricated in a 0.5μm CMOS process is shown in Fig. 9. It has many p+ contacts of different sizes on a p-substrate and connected to DC probe pads. The measurement results for G_1 for a small contact are shown in Fig. 10. It is seen that G_1 becomes a constant beyond a certain separation as expected. For large contacts, the conductance G_1 to the back plane can be modeled as a function of the area and the perimeter of the contact [4]. The model in (11) for a 2D structure can be extended to a 3D device. The width W1 of the 2D device in Fig. 3(a) corresponds to the area A. For a heavily doped substrate, the conductance G_{1_∞} is given by

$$G_{1_\infty} = \kappa A + \lambda P \tag{12}$$

where G_{1_∞} represents the conductance of the contact to the bulk with all other contacts floating and κ and λ are constants for a given process. The values of κ and λ can be determined from simulations or measurements using two contacts of different sizes. The ξ in (7) for a given area A and perimeter P is related

to κ and λ by

$$\frac{1}{\xi} = \kappa A + \lambda P \tag{13}$$

This relationship is compared with measurements for contact sizes of different areas and perimeters in Fig. 11. The close agreement between the model and the empirical results suggests the validity of the model.

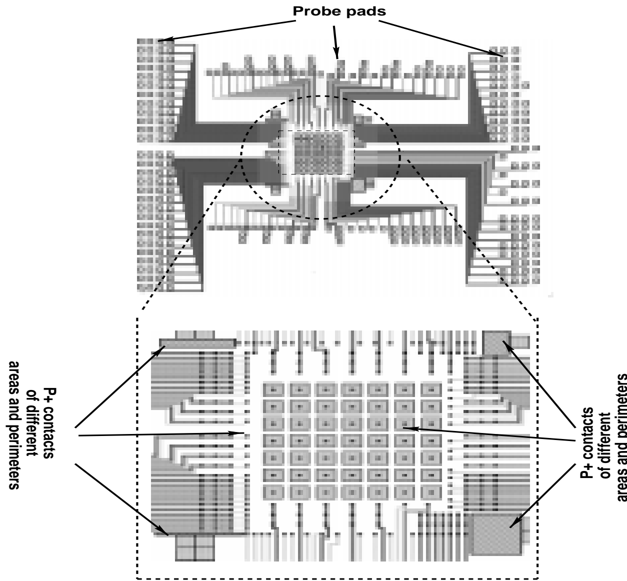

Fig. 9. Layout of the test chip

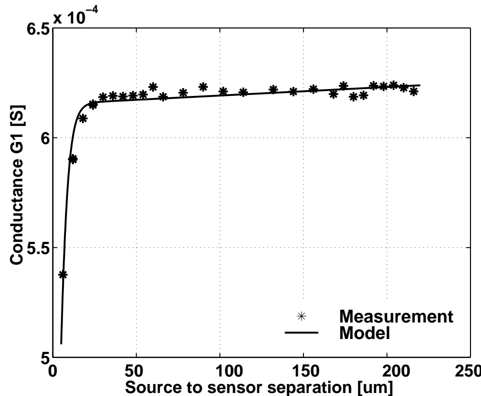

Fig. 10. Experimental results for conductance G_1.

Equation (12) suggests that for a given area or perimeter, it is possible to minimize or maximize G_1. For a given area A, the minimum for G_1 occurs for a minimum value of the perimeter P. This condition is satisfied for a circular shape contact.

VI. Conclusion

A simple resistive macromodel for substrate noise coupling in heavily doped substrates has been described. This model is valid up to a few GHz. It is based on curve fitting and requires the knowledge of a few parameters for completely and accurately determining the substrate model for any size of the contacts. This model is scalable with distance of separation between the injection and sensing ports on the substrate. A unique feature of the model is that the substrate can be readily characterized with a small number of measured data points. Furthermore, no precharacterized libraries are necessary. The model has been used to accurately predict the coupling for different CMOS processes. Future work will include extensions of this model to guard rings, lightly doped substrates and validation in realistic circuit examples.

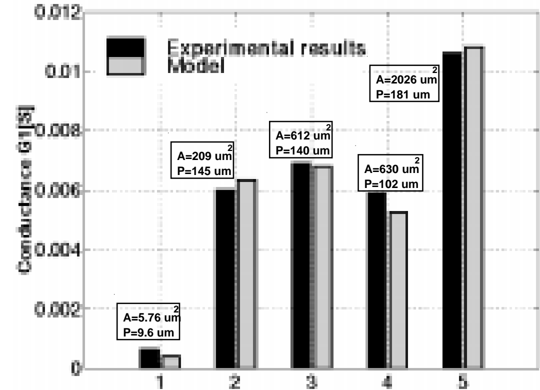

Fig. 11. Comparison of the model for G_1 as a function of area (A) and perimeter (P) with measurements.

VII. Acknowledgements

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