Transport in Split Gate MOS Quantum Dot Structures

Center for Solid State Electronic Research, Arizona State University, Tempe, AS 85287-6206, USA

Abstract

A novel technique has been developed for the fabrication of Si quantum dot structures with controllable electron number through both top and side gates. We have tested devices ranging in size from 40 to 200nm. By varying the density with the top gate, and controlling the input and output barriers of the dot with the side gates, conductance peaks are observed which map details of the energy level within the dot as well as the interaction of the electrons with one another.

Introduction

There is considerable interest in quantum dots, as they represent the ultimate reduction in the dimensionality of a semiconductor device. In addition, it is hoped that these devices can extend the observations of single-electron tunneling [1] into the semiconductor device realm where they can be coupled to normal transistors. While there have been several observations of single-electron behavior in GaAs heterostructures, efforts in Si-based devices have been limited to either lithographically defined dots [2][3], or devices which have relied upon accidental definition of dots [4][5]. Here, we describe the fabrication and measurements of a dual gate-defined quantum dot, which is embedded within aSi metal-oxide-semiconductor (MOS) field-effect transistor. The dot is formed in the inversion layer created by the top gate, with its lateral definition being provided by two side gates embedded within the gate oxide.

Fabrication

Quantum dots of differing geometry were fabricated by a split gate technique within a MOSFET structure as shown in Fig. 1. Basically, a channel-stop region is formed by implanting a P (100) Si wafer with boron. A thin gate oxide is grown over which narrow chromium gates are defined using e-beam lithography. A field oxide and top inversion gate is deposited for independent control of the dot occupancy.

In Fig. 2, we show a top view illustrating a typical gate geometry in which a small quantum dot is embedded within the structure. The dot itself is defined by the side gate pattern which depletes electrons under the side gates when they are negatively biased, leaving an island of electrons. A second quantum dot geometry is shown by the electronmicrograph in Fig. 3 in which the side gates are independently controlled, and offset from one another.

Fig. 1 Schematic of Si quantum dot structure.

Fig. 2 Top view of the quantum dot geometry defined by the side gate pattern.

Fig. 3 Electron micrograph of a second geometry investigated. The metal lines are 100 nm wide.
Characterization

Four-terminal DC Electrical measurements were performed at 4.2 K in a liquid-Helium cryostat. Equilibrium measurements are performed by applying a small source-drain excitation. Strong oscillations in the conductance are observed in structures with both normal and with overlapping constrictions. Typical oscillations are shown in the plot in Fig. 4, which are suggestive of Coloumb oscillations due to the filling of the dot one electron at a time. In the figure, the top gate bias was swept for fixed depletion gate. In all measurements, the device is operating within the tunneling regime, where the resistance of the input and output constrictions is much greater than 25 kΩ (the inverse of $G_0 = e^2/h$, the fundamental conductance). Splitting of conductance peaks is observed which appears to be due to breaking of the valley degeneracy in Si, although the actual cause is unknown at this time.

![Conductance vs Inversion Gate Bias](image)

Fig. 4 Coulomb blockade oscillations in the quantum dot structure of Fig. 3.

In Fig. 5, we plot the drain current through the device geometry shown in Fig. 2 for a drain bias of 0.2 mV. The family of curves is generated by changing the top gate voltage in 20 mV steps, in the range from 2.5-3.1 V, and sweeping the side-gate voltage from +100 mV to -500 mV. It was found that this measurement sequence was the best for eliminating hysteresis arising from a discrete change in the number of electrons in the dot from run to run. Measurements done with the side gate voltage swept in the opposite direction contained considerable hysteresis which made the interpretation more difficult. The choice of sweep direction does not alter the characteristic but only translates it to the left or right. From this figure, it is clear that the side gate voltage sweep is depleting the electrons from the dot, and that the current peaks correspond to single-electron events, with the dot being ultimately completely depleted for sufficiently negative side gate voltage. This threshold is dependent upon the top gate voltage as well. We may assume that the dot is pinched off at the largest negative side gate bias. There is a general linear trend in the position of the peaks. If we look at the first peak from the left, we observe at first a modulation of the peak amplitude with the top gate voltage. However, at higher top gate voltages, the peak splits into multiple peaks. We also observe peaks merging together and splitting apart at different top gate voltages. For example, if we track the shoulder indicated arrow “A”, we see that the peaks start to collapse into one large peak and later split up again at more positive gate biases. This is reminiscent of the crossings and anti-crossings in the magneto-electric band structure of a quantum dot, except that here the inversion gate is inducing this behavior. To the left of this shoulder, another series of peaks are marked by arrow “B”. These are observed to merge together at about the same top gate voltage where peak “A” collapsed, and split again at about the same higher top gate voltage.

We can extract the capacitance of the top and side-gates to the dot from the above figure. The linearity of the position of the first peak allows us to write $Q = C_dV_d = C_{sg}V_{sg}$, or $C_s = 2.4C_{sg}$. From the data, we estimate that $C_{sg} \approx 0.7$ aF and $C_s \approx 1.7$ aF. The capacitance can also be extracted from the Coulomb gap observed around zero volts. For $V_d = 2.9$ V and $V_{sg} = -400$ mV, $q/2C_{sg} = 13$ mV, and $C_{sg} = 6.2$ aF. If it is assumed that the equivalent capacitance is approximately the self-capacitance of a flat disc, then $d \approx 15$ nm. Clearly, energy level separation due to confinement can be observed at this dimension as well.
Summary

In summary we have fabricated quantum dot structures in Si MOS structures which have controllable dot density and lateral confinement. Cryogenic measurement of the dots reveal distinct conductance oscillations which are argued to arise from level filling of the discrete states in the dot coupled with the Coulomb charging energy of electrons interacting with themselves and the environment. Such dots are currently being investigated for possible hybrid single electron device/MOS transistor technology.

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References