Transistor Stuck-Open Fault Detection in Multilevel CMOS Circuits

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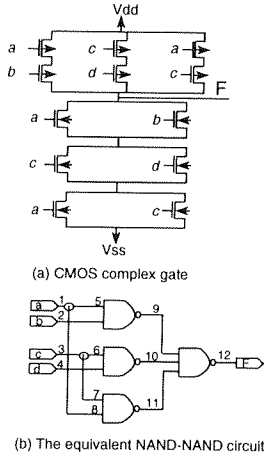
Abstract

The necessary and sufficient conditions for detecting transistor stuck-open faults in arbitrary multi-level CMOS circuits are shown. A method for representing a two-pattern test for detecting a single stuck-open fault using only one cube is presented. The relationship between the D-algorithm and the conditions for detecting transistor stuck-open faults in CMOS circuits is provided. The application of the proposed approach in robust test generation for transistor stuck-open faults in a number of benchmark circuits is demonstrated. The fault coverage achieved is as good as or better than those reported using existing techniques.

keywords: Transistor stuck-open fault, two-pattern test, test pattern generation, multi-level CMOS circuits testing, robust CMOS testing.



1 Introduction

Testability analysis of TSOP faults aims at investigating the necessary and sufficient conditions under which the TSOP faults are robustly testable by a sequence of test vectors [8], [10], [7], [3], [4], [2], [6], and [5]. This paper presents a new approach to investigate TSOP testability in arbitrary multi-level CMOS circuits, which uses the notation of the D-Algorithm [11] and the concept of *event propagation*. A one cube to represent a two-pattern test for a single TSOP fault is used. The notation $D(\overline{D})$ is used to indicate the bit transition event $0 \rightarrow 1 (1 \rightarrow 0)$ that occurs when applying the sequence of two patterns. A CMOS complex gate can be modeled as a combinational network of the primitive gates NAND, NOR, and NOT [10][9]. Figure 1 depicts a CMOS complex gate and its equivalent two-level NAND-NAND circuit. Two-pattern tests for TSOP faults in the pFET's of the first level NAND gates are also the tests for TSOP faults in the nFET's of the complex gate. The tests for TSOP faults in the pFET's of the complex gate are identical to the tests of TSOP faults in the pFET's of the output NAND gate [10]. A two-pattern test $< T_1, T_2 >$ is said to be *robust test* for a TSOP fault s if it detects s even in the presence of arbitrary time delays when the primary inputs change for T_1 to T_2 [8]. One of the necessary (but not sufficient) conditions for two patterns to robustly detect a stuck-open fault is that the two patterns differ in exactly one bit [10]. Consider the case of single TSOP fault on the pFET whose gate is connected to line 9 in Figure 2.

It is easy to see that $< \{0,1,0,0\}, \{1,1,0,0\} >$ is a robust two-pattern test for p_9 stuck-open.

2 TSOP Fault Detection in Primitive Gates

We detect TSOP faults by applying an event to primary inputs of the circuit and observing the primary out-

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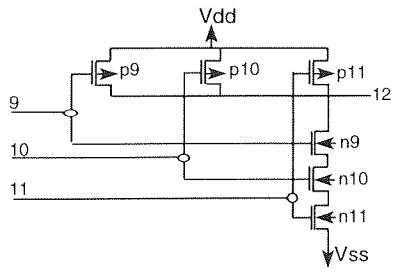
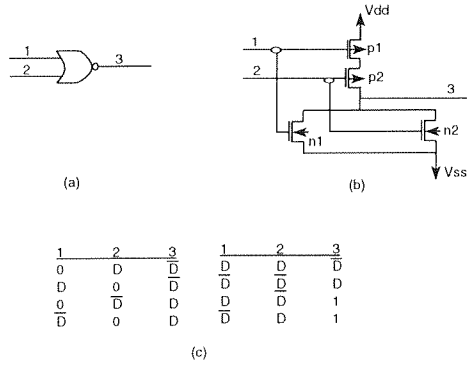


puts of the circuit to see whether the event can be properly propagated to one of the primary outputs. If T_1 and T_2 are two binary vectors, the transition cube from T_1 to T_2, denoted as $T_1 \rightarrow T_2$, is defined using the coordinate transition operation as follows: $0 \rightarrow 0 = 0, 1 \rightarrow 1 = 1$, $0 \rightarrow 1 = \overline{D}, 1 \rightarrow 0 = D$, where D and $\overline{D}$ are called *events*.

The meaning of the notation $\overline{D}$ or D is a signal transition event $0 \rightarrow 1$ or $1 \rightarrow 0$ that occurs on a line when two patterns are applied. This is different from the meaning of $\overline{D}$ or D in conventional stuck-at test. The reason for introducing the concept of transition cube is to represent two test patterns with one cube. Let $T = \{a_1, ..., a_n\}$ be a cube with its elements, $a_i \in \{0, 1, \overline{D}, D\}$ for $1 \leq i \leq n$, then two binary vectors T_1 and T_2 can be uniquely defined by T such that $T_1 \rightarrow T_2 = T$. For example, given $T = \{\overline{D}, 1, 0, D\}$, we have $T(1) = \{0, 1, 0, 1\}$ and $T(2) = \{1, 1, 0, 0\}$.

Consider the two-input NOR gate shown in Figure 3.



Let $T = \{\overline{D}, 0\}$ be a transition cube. Then, $T(1) = \{0, 0\}$, $T(2) = \{1, 0\}$. It is easy to see that $< T(1), T(2) >$ is a robust test for the n_1 stuck-open fault, and T (which is contained in the primitive D-cube $\{\overline{D}, 0, D\}$) is a robust test pattern for the fault. In a similar way, we can show that $\{0, \overline{D}\}$ (which is contained in the primitive D-cube $\{0, \overline{D}, D\}$) is the RTP for n_2 stuck-open fault. Also, $\{D, 0, \overline{D}\}$ (which is contained in the primitive D-cube $\{D, 0, \overline{D}\}$) is the RTP for p_1 or p_2 stuck-open faults. Similar arguments can be drawn about the NAND and NOT gates. Table 1 shows the FDT for two-input NAND and NOR gates.

To investigate which primitive D-cube contains a robust test pattern and which TSOP fault can be detected by it, we construct a *fault detection table* (FDT) for a primitive cube as follows. For each primitive D-cube $PD = \{a_1, ..., a_{n+1}\}$ of an n-input primitive gate, let $T = \{a_1, ..., a_n\}$ be the input cube applied to the gate. If a TSOP fault on pFET p_i (nFET n_i), where $1 \leq i \leq n$, can be robustly tested by $< T(1), T(2) >$, then $p_i(n_i)$ is listed as a detectable fault of PD and PD is called a *pFET (nFET) detection cube* of the gate. If $< T(1), T(2) >$ cannot detect any TSOP fault in the gate, then the detectable fault column is filled with a '-' and PD is said to be a *non-detection cube* of the gate. To simplify the presentation, we call the last element of a primitive D-cube as its output and the set of other values as its inputs, in which the ith element corresponds to the ith input line of the gate.

NAND		NOR	
Primitive D-cube	TSOP Faults	Primitive D-cube	TSOP Faults
$D\ 1\ \overline{D}$	p_1	$\overline{D}\ 0\ D$	n_1
$1\ D\ \overline{D}$	p_2	$0\ \overline{D}\ D$	n_2
$D\ D\ \overline{D}$	–	$\overline{D}\ \overline{D}\ D$	–
$\overline{D}\ D\ 1$	–	$D\ \overline{D}\ 0$	–
$\overline{D}\ 1\ D$	n_1, n_2	$D\ 0\ \overline{D}$	p_1, p_2
$1\ \overline{D}\ D$	n_1, n_2	$0\ D\ \overline{D}$	p_1, p_2
$\overline{D}\ \overline{D}\ D$	n_1, n_2	$D\ D\ \overline{D}$	p_1, p_2
$D\ \overline{D}\ 1$	–	$\overline{D}\ D\ 0$	–

Let $T = \{a_1, ..., a_n\}$ be a cube. The dual cube of T, denoted as $T\prime$, is defined as the cube $\{a_1\prime, ..., a_n\prime\}$ such that, for $1 \leq i \leq n$, if $a_i \in \{0, 1\}$ then $a_i\prime = a_i$; if $a_i = \overline{D}$ then $a_i\prime = D$; if $a_i = D$ then $a_i\prime = \overline{D}$.

Let T be a detection cube of gate G. If its dual cube $T\prime$ is also a detection cube of G, then T is said to be a strong detection cube (SDC), otherwise T is said to be a weak detection cube (WDC) of G. In Table 1, $\{D, 1, \overline{D}\}$ is a SDC for the two-input NAND gate since its dual cube $\{\overline{D}, 1, D\}$ is also a detection cube of the NAND gate. The detection cube $\{\overline{D}, \overline{D}, D\}$ is a WDC for the NAND gate because its dual cube $\{D, D, \overline{D}\}$ is not a detection cube of the the NAND gate. The following assertions are made in the paper.

1. Every strong detection cube of a primitive gate has exactly one event in its inputs and one event in its output.

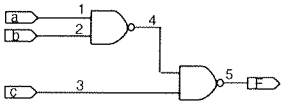
2. If T is a strong pFET (nFET) detection cube of a gate G, then $T\prime$ is a strong nFET (pFET) detection cube of G.
3. Let T be a SDC of gate G. If the ith input of T is an event, then we say the TSOP fault in p_i or n_i is strongly detected.
4. The weak detection cube of a NOR (NAND) gate has more than one $D(\overline{D})$ in its inputs and has $\overline{D}(D)$ as its output. Its dual cube is a non-detection cube with an event as its output.
5. If T is a pFET(nFET) detection cube of a NOR(NAND) it detects all of the pFET (nFET) stuck-open faults in the NOR (NAND) gate.

The above results for primitive gates pave a way to investigate the problem of robust TSOP fault test in a multi-level CMOS circuits. This is discussed in the next section.

3 TSOP Test in Multilevel CMOS Circuits

Let C be a multi-level CMOS circuit, G be a gate in C, and T be a test pattern represented as a transition cube. The test cube, TC, of a circuit under test patter T is computed by a forward implication procedure defined in [12]. A gate is called an active gate if and only if all the input lines of the gate have known values from the set $\{0, 1, \overline{D}, D\}$. When the test cube of a circuit is computed we say that T *is applied to the circuit.* The *test cube of a gate* under T is a vector of values on the input and output lines of the gate when T is applied to C.

Consider the two-level circuit shown in Figure 4. Suppose the test pattern is $T = \{\overline{D}, 1, 1\}$. Then the initial test cube of the circuit $TC = \{\overline{D}, 1, 1, X, X\}$ where X represents unknown value. Gate 4 is an active gate since all of its input lines have known logic values. D-intersect TC with the primitive D-cube $\{\overline{D}, 1, X, D, X\}$ of gate 4 to get $TC = \{\overline{D}, 1, 1, D, X\}$. Now gate 5 is an active gate. D-intersect TC with the primitive D-cube $\{X, X, 1, D, \overline{D}\}$ of gate 5 to get $TC = \{\overline{D}, 1, 1, D, \overline{D}\}$, which is the test cube implied by T, since all the lines in the circuit have known values. From this TC, we obtain the test cube of gate 4 $\{\overline{D}, 1, D\}$. The test cube of gate 5 under T is $\{1, D, \overline{D}\}$.



It should be useful to make the following observation. If G is a logic gate in a circuit C, s is a TSOP fault in G, and tc is the test cube of G under test pattern T, then a necessary condition for T to detect s in C is that tc be a detection cube of G which detects s in G.

Definition: *Let T be a test pattern for circuit C. A sequence of nodes $\{v_0, ..., v_n\}$ in C are said to form an event propagation path from v_0 to v_n iff an event is propagated from v_0 to v_n when T is applied to C.*

This definition implies that all the lines on an event propagation path have value $\overline{D}$ or D when T is applied to C. For example, let $T = \{\overline{D}, 1, 1\}$ be a test pattern applied to the circuit shown in Figure 4. An event propagation path is $P = \{a, 1, 4, 5, F\}$, where a is a primary input and F is a primary output node. Nodes 4,5 denote gates 4 and 5 respectively.

Lemma: *Let T be a test pattern applied to circuit C. Let s be a TSOP fault in gate $G \in C$. A necessary condition for T to detect s is that there is an event propagation path P from a primary input to a primary output such that $G \in P$.*

Definition: *Let C be a multi-level circuit. Let $P = \{v_0, ..., v_n\}$ be an event propagation path under test pattern T. Let $P_1 = \{v_i, ..., v_k\}$, $0 \leq i \leq k \leq n$, be a subpath of P such that there is another path P_2 which propagates an event from v_i to v_k. P_1 is said to be undetection region on P if the test cube of v_k under T is a nondetection cube of v_k. P_1 is said to be a weak detection region on P, if the test cube of v_k is a weak detection cube. Let gate $G \in P$, if G is not in any undetection or weak detection region of P, we say G is in the strong detection region of P.*

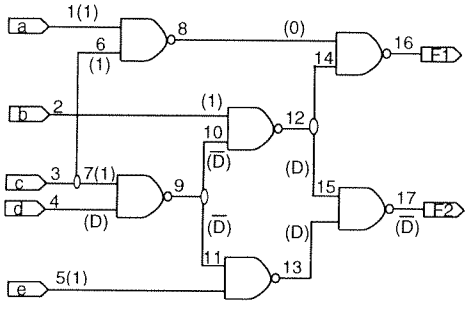


Figure 5 shows a multi-level circuit C. Assume that test pattern $T = \{1, 1, 1, D, 1\}$ is applied to C. The logic value carried by each line is shown in parentheses in the figure. It can be seen that an event propagation path $P = \{d, 4, 9, 10, 12, 15, 17, F2\}$ is formed, where 10 and 15 are branches of the two fan-out nodes with line 9 and line 12 as their stems respectively. Consider the subpath $P1 = \{9, 10, 12, 15, 17\}$ of P. The test cube gate 17 under T is $tc_{17} = \{D, D, \overline{D}\}$. Since tc_{17} is a non-detection cube of a two input NAND gate, and since there is a path $P2 = \{9, 11, 13, 17\}$ that propagates an event from 9 to gate 17, P1 is not a detection region on P. Similarly, we can show that $P2$ is not a detection region on the event propagation path $\{d, 9, 11, 13, 17, F2\}$. If $T\prime$ (the dual of T)

$= \{1, 1, 1, \overline{D}, 1\}$ is applied to C, the test cube of gate 17 will be $\{\overline{D}, \overline{D}, D\}$, which is a weak detection cube. In this case, P1 is a weak detection region on P. Whether T or T' is applied to C, gate 9 is in strong detection region of P.

Experiments were conducted to generate TSOP test patterns for the MCNC benchmark circuits [1]. Table 2 summarizes some of the results obtained using the above mentioned approach. We used the same set of 25 benchmark circuits as those used by Brayn et al. in [3].

Circuit Name	No. Inputs	No. Outputs	No. Faults	No. Patt.	TSOP Coverage	Coverage in [3]	CPU Time
Z7xpl	7	10	882	116	99.6	99.2	5
Zpsym	9	1	1234	263	99.9	99.5	20
addm4	9	8	2630	418	99.9	99.6	68
adr4	8	5	758	132	100.0	100.0	6
al2	16	47	462	92	99.8	100.0	9
bcd.div3	4	4	94	15	100.0	100.0	1
dist	8	5	1744	272	99.7	98.1	23
f51m	8	8	860	137	99.5	98.9	7
l8err	8	8	734	115	98.4	97.3	5
life	9	1	1060	226	100.0	100.0	23
log8mod	8	5	556	78	99.3	98.4	2
m181	15	9	520	97	99.0	100.0	4
m2	8	16	978	118	100.0	100.0	7
m3	8	16	1318	150	99.7	98.7	9
m4	8	16	2012	234	99.0	98.1	23
mlp4	9	8	1744	269	99.9	99.0	25
radd	8	5	804	129	99.9	100.0	5
rd53	5	3	382	59	100.0	100.0	1
rd73	7	3	1492	265	100.0	97.3	16
root	8	5	802	134	99.0	97.2	6
sqr6	6	12	602	76	100.0	100.0	2
sym10	10	1	2486	408	100.0	89.8	90
t3	12	8	468	77	99.8	100.0	3
x1dn	27	6	1208	232	100.0	100.0	89
z4	7	4	634	112	100.0	100.0	3

The achieved TSOP fault coverage using this approach and those reported by Bryan et al. in [3] are included in the table. Also included, are the CPU times in seconds required to generate test set for these benchmark circuits using our approach (CPU Time).

4 Conclusion

The necessary and sufficient conditions for robust testing of transistor stuck-open faults are investigated through the use of D-notations. This allows us to use one test cube to represent two test patterns, and the basic concepts of D-algorithm for testing of transistor stuck-open faults in multi-level CMOS circuits. Similar test conditions are observed for primitive gates and multi-level CMOS circuits with respect to the strong, weak, and non-detection testing of transistor stuck-open faults. As a result of these, a deductive fault simulator is presented for transistor stuck-open fault testing in multi-level CMOS circuits. Given a robust tow-pattern test $< T_1, T_2 >$, the simulator can derive all the transistor stuck-open faults that are testable by both $< T_1, T_2 >$ and $< T_2, T_1 >$ using one simulation run of the fault-free circuit. Experiments using the MCNC benchmark circuits show that these results can be used for test pattern generation purposes for transistor stuck-open faults in multi-level CMOS circuits. The resulting TSOP fault coverage is as high or higher than those reported in [3] and the CPU time required is quite low.

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