A 1.8V High Dynamic-Range CMOS High-Speed Four Quadrant Multiplier

Chi-Hung Lin and Mohammed Ismail

Department of Electrical Engineering , The Ohio State University, Columbus, OH 43210, USA

email: linc@ee.eng.ohio-state.edu

Abstract

A low-voltage ($\leq 3V$) CMOS four quadrant multiplier is introduced which has an almost rail-to-rail differential-input-swing with a low signal-distortion($\leq 1\%$ for 100kHz signal). The proposed circuit is composed of a pair of rail-to-rail differential-input V-I converters and a pair of voltage-followers. This topology of multiplier results in a high frequency capability with low power consumption. In a $1.2\mu m$ n-well CMOS process, the 3dB frequency of the multiplier is in a range of 103MHz. Measured total power consumption is around 0.52mW with supply voltage 2V. The multiplier can operate at a minimum supply voltage of 1.8V.

1. Introduction

The analog multiplier is one of the important building blocks in VLSI communication systems, which can be applied to frequency mixers, variable gain amplifiers, adaptive filters, phase-locked loops and many other signal processing circuits. The Gilbert cell is the most popular multiplier first implemented in bipolar technology. Low-voltage, low-power analog CMOS design solutions are necessary for high performance mixed-signal ICs. Restricted by the MOSFET characteristics, CMOS multipliers usually need extra linearization circuits which may degrade the performance. Therefore, some of CMOS multipliers [1]-[9] are not very optimal for low-voltage low-power applications. Other low-voltage multipliers [10]-[16] can operate at low supply voltage. The performances are however limited to small swing range, signal distortion and high power consumption.

This paper presents a low-voltage CMOS four quadrant multiplier capable of achieving linear rail-to-rail input swing and having low-signal distortion with low power dissipation. The operation of the circuit is introduced in Section 2, second-order effects, nonlinearity and frequency performance are discussed in Section 3.

2. Circuit Description

This multiplier is composed of a pair of V-I converters

and a pair of voltage follower. The V-I converter [17] is shown in Fig.1. Usually, a simple differential pair is used for voltage-current conversion, its large differential-input swing is limited by the threshold voltage of the core transistors and by the saturated drain-source voltage of current sinks or sources with lower power supply. While the amplitude of fully differential input signal increases to saturate either input transistors in a differential pair, the linear relation of $I_{out}=g_m V_d$ no longer exists because of cut off or weak inversion operation of either transistors. This results in a narrow window for large differential-input voltage in low supply voltages ($\leq 3V$). To resolve this problem, a novel voltage-to-current converter is shown in Fig.1. Considering high frequency signal processing, the core transistors, M1 and M1a, should be maintained in saturation region. Four transistors (M4, M4a, M5, M5a) are stacked with transistors M1, M1a. Assuming that M4, M4a, M5, M5a are biased in triode region, then V_{ds} of M1, M1a is kept very close to $V_{DD}-V_{SS}$. For instance, with $V_{DD}-V_{SS}=3V$, by setting common-mode input voltage properly, M1, M1a can operate in saturation region with $V_{ds,M1,M1a} \geq V_{cm} \pm 1.5 - V_{tn}$, as differential-input voltage increases or decreases by almost 1.5V. So the linear voltage-current relation can be kept within almost $\pm 1.5V$ differential input. A feedback loop M2, M3, (M2a, M3a) biases the gates of M4 to maintain triode operation of M4. M5 functions as a voltage-controlled resistor, the combination of M2, M3 is a voltage attenuator(see eq.1).

$$V_{sM2,M2a} = \frac{KV_{gM2,M2a} - (K-1)V_{tn}}{K+1} \quad (1)$$

where $K=\sqrt{Kn_{M2}/Kn_{M3}}$.

In common-mode signal processing, the triode operation of M4, M4a is established by the source voltages of M2, M2a and long channel length of the core transistors M1, M1a. So sizing the aspect ratio of M2, M3 can keep the gate voltages of M4, M4a high enough for triode operation with long channel length transistors of M1, M1a. Based on the same current flowing through triode M4 (M4a) and saturated M1 (M1a), source voltage of M1

(M1a) are pushed close to V_{SS}. Therefore, the source (drain) voltages of M1, M1a (M4, M4a) can be as low as tens of millivolt. So body effect can be reduced, even ignored.

In differential-mode signal processing, the feedback loop always keeps the source voltages of M1 to follow the input signal but attenuated, so assume $V_{sM1,M1a} = AV_{in+,in-} = A(V_{cm} + V_d/2, -V_d/2)$. A is an attenuation coefficient of feedback loop, $A \leq 1$[17]. The drain voltages of M5, M5a are very close to V_{DD} by triode-biasing of V_b and V_b tunes g_m of voltage-to-current conversion. V_{in+}, V_{in-} would deliver V_1, V_2 to generate a differential input voltage signal at the gate of M2, M2a and differential currents in their drains. By mirroring these differential currents through M3, M3a, M6, M6a and subtracting them, a linear $I_{out} = I_{o2} - I_{o1}$ can be obtained. So achieving almost rail-to-rail differential-input-swing is dependent on the common-mode input voltage setting and the threshold voltage.

The output current equation can be deduced as follows; of M5, M5a.

$$
\begin{aligned}
I_{out} &= I_{M2a} - I_{M2} \\
&= \frac{K_n K_n'((1-A)^2 V_{cm} - (1-A)V_{tn})(V_{nl} - 4V_{tn})}{2(K+1)^2(K_p(V_b' - V_{tp}) - V_{DD} + \frac{1}{2}V_{nl})} \\
&\quad \times V_d
\end{aligned} \tag{2}
$$

Assume threshold voltages of all NMOS are the same as V_{tn} without body effect, K_n, K_n' are transconductance parameter of NMOS for M1, M1a and M2, M2a, and K_p for M5, M5a, $V_{nl} = V_1 + V_2$ is nonlinear term. The term V_{nl} appearing in denominator can be combined with V_{DD} as $\frac{1}{2}(2V_{DD} - V_1 - V_2)$. This term can be ignored in eq.2 because of very small second-order term of triode region equation compared with the first-order term.

$$
\begin{aligned}
I_{out} &= I_{M2a} - I_{M2} \\
&= \frac{K_n K_n'((1-A)^2 V_{cm} - (1-A)V_{tn})(V_{nl} - 4V_{tn})}{2(K+1)^2(K_p(V_b' - V_{tp}))} \\
&\quad \times V_d
\end{aligned} \tag{3}
$$

The other nonlinear term appears in numerator of eq.3, this term can be minimized by a factor of $(1+K)^2$ by sizing the ratio of M2, M3(M2a, M3a). Also as V_1, V_2 are very close to positive supply voltage, the value of V1+V2 is approximately of $2(V_{DD} - V_{SS})$. So the nonlinear effect is weak with the attenuation coefficient $(1+K)^2$. For example, at 3V supply voltage, the variation of V_1+V_2 is below 0.8% within $2V_{DD}$ before dividing by $(1+K)^2$ in simulation. Later, experimental results also validate this assumption.

The proposed multiplier is shown in Fig.2. Two V-I converters are parallelly connected with a pair of voltage followers, M_{sf}, $M_{sf'}$. The sources of the voltage followers and the sources of the core transistors, M1, M1a, M1', M1a', are connected together.

Since $V_{ds,M1,M1a,M1',M1a'}$ are very close to $V_{DD}-V_{SS}$, $V_{ds,Msf,Msf'}$ can reach almost power-supply voltage. The output current can be easily derived. Assume that K_n, K_n' and K_n'' are the transconductance parameters of M1,1a,1',1a', M2,2a,2',2a' and Msf,sf', the threshold voltages of all NMOS are the same as V_{tn}

$$
V_1 - V_3 = V_{gs1} - V_{gs3} = \sqrt{\frac{2I_{M1}}{K_n}} - \sqrt{\frac{2I_{Msf}}{K_n''}} \tag{4}
$$

So, $\sqrt{I_{M1}} = \sqrt{\frac{K_n}{2}}(V_1 - V_3) + \sqrt{\frac{K_n I_{Msf}}{K_n''}}$.

Squaring this equation, I_{M1} can be derived as,

$$
I_{M1} = \frac{K_n}{2}(V_1 - V_3)^2 + K_n\sqrt{\frac{2I_{Msf}}{K_n''}}(V_1 - V_3) + \frac{K_n I_{Msf}}{K_n''} \tag{5}
$$

Similarly, I_{M1a} is expressed as,

$$
I_{M1a} = \frac{K_n}{2}(V_2 - V_3)^2 + K_n\sqrt{\frac{2I_{Msf}}{K_n''}}(V_2 - V_3) + \frac{K_n I_{Msf}}{K_n''} \tag{6}
$$

and $I_{M1} - I_{M1a}$ is thus given by,

$$
I_{M1} - I_{M1a} = \left[\frac{K_n}{2}(V_1 + V_2 - 2V_3) + K_n\sqrt{\frac{2I_{Msf}}{K_n''}}\right](V_1 - V_2) \tag{7}
$$

Since from triode mode equations of M5, M5a, $I_{M1} - I_{M1a} = (K_p(V_b' - V_{tp}) - V_{DD} + \frac{V_x + V_y}{2})(V_y - V_x)$,

$$
V_x - V_y = \frac{\frac{K_n}{2}(V_1 + V_2 - 2V_3) + K_n\sqrt{\frac{2I_{Msf}}{K_n''}}}{K_p(V_b' - V_{tp}) - V_{DD} + \frac{V_x + V_y}{2}}(V_1 - V_2) \tag{8}
$$

Realizing that $V_b' = V_{DD} - V_b$, $I_1 - I_2 = I_{M2} - I_{M2a} = \frac{K_n'}{2(1+K)^2}(V_{nl} - 4V_{tn})(V_x - V_y)$, $V_{nl} = V_x + V_y$ and from the equations of V-I converter, thus,

$$
\begin{aligned}
I_1 - I_2 &= \frac{K_n'[\frac{K_n}{2}(V_1 + V_2 - 2V_3) + K_n\sqrt{\frac{2I_{Msf}}{K_n''}}]}{2(1+K)^2[K_p(V_b' - V_{tp}) - V_{DD} + \frac{V_x + V_y}{2}]} \\
&\quad \times (V_{nl} - 4V_{tn})(V_2 - V_1)
\end{aligned} \tag{9}
$$

Similarly, $I_3 - I_4 = I_{M2a'} - I_{M2'}$ is obtained. Then the total output current, $(I_1 + I_3) - (I_2 + I_4)$, is obtained by the subtraction of I_{o1} and I_{o2}.

$$
\begin{aligned}
I_{out} &= \frac{K_n K_n'(V_{nl} - 4V_{tn})}{2(1+K)^2[K_p(V_b' - V_{tp}) - V_{DD} + \frac{V_x + V_y}{2}]} \\
&\quad \times (V_1 - V_2)(V_3 - V_4)
\end{aligned} \tag{10}
$$

As it can be observed from eq.10, the output current I_{out} is a multiplication function of two differential input voltage $V_1 - V_2$ and $V_3 - V_4$. The nonlinearity of the

V_{DD}	2V	3V
	0.52mW	3mW

multiplier is determined by that of the V-I converter and the minimization of nonlinearity can be achieved accordingly.

Fig.3, 4 show measured DC characteristics of the multiplier at a supply voltage of 3V, 2V. Measured Spectrum of the multiplier is shown in Fig.5 with setting one input of multiplier at constant DC value. In measurement, measured THD is around 0.9% with 1V 100kHz sinusoidal input signals at 3V power supply voltages. Table I specifies the consumed static power at different supply voltages.

3. Circuit Analysis :
Second-Order Effects and High-Frequency Analysis

In practical circuit implementations, linearity error could result from mobility reduction, channel-length modulation and body effect. The former two effects depend on the process quality, the last can be reduced by connecting sources and bulks of transistors. Since the source voltages of M1, M1a are very close to ground node, the body effect can be reduced without source-bulk connection. Theoretically, it is assumed that all NMOS devices have no body effect, practically, source-bulk connected M2,2a, M2',2a' can increase linearity. Nevertheless, a p-well fabrication technology is necessary for source-bulk connection.

The simulation result presents 3dB-frequencies at around 103MHz. The simulation shows that the output current mirrors would mainly dominate the high-frequency performance.

4. Conclusion

A 1.8V low-power CMOS high-speed multiplier has been presented. The multiplier can be used in an analog VLSI cell library for low-voltage, low-power high dynamic-range and high speed applications, such as IF variable gain amplifiers and adaptive filters.

REFERENCES

[1] K. Bult and H. Wallinga, "A CMOS Four-Quadrant Analog Multiplier," IEEE J. of Solid-State Circuits, vol. SC-21, No. 3, pp. 430-435, June, 1986.

[2] S.-I. Liu and C.-C. Chang, "CMOS Analog Divider and Four-Quadrant Multiplier Using Pool Circuits," IEEE J. of Solid-State Circuits, vol. 30, No. 9, pp. 1025-1029, September, 1995.

[3] J. S. Pena-Finol and J. A. Connelly, "A MOS Four-Quadrant Analog Multiplier Using the Quarter-Square Technique," IEEE J. of Solid-State Circuits, vol. SC-22, no. 6, pp. 1064-1073, December, 1987.

[4] S.-C. Quin and R. L. Geiger, "A ±5-V CMOS Analog Multiplier ," IEEE J. of Solid-State Circuits . vol. SC-22, no. 6, pp. 1143-1146, , December, 1987.
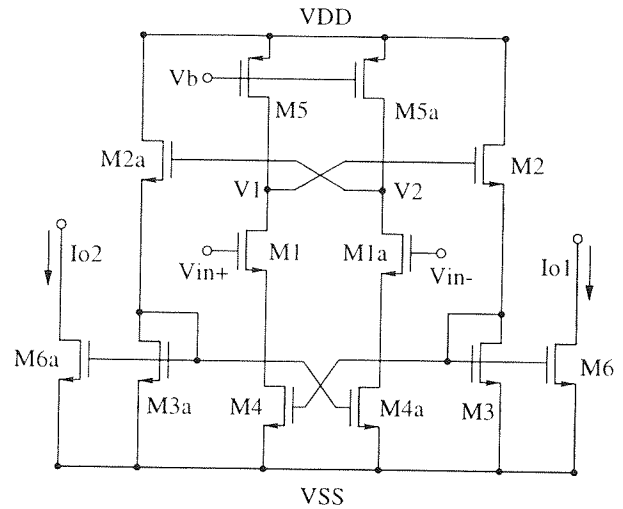
Fig. 1. A low-voltage low-power V-I converter

[5] S. Sakurai and M. Ismail, "A High Frequency Wide Range CMOS Analog Multiplier," Electronics Letters, vol. 28, no. 24, pp. 2228-2229, 19th November, 1992.

[6] C. Abel, S. Sakurai, F. Larson and M. Ismail, "Four-Quadrant CMOS/BiCMOS Multipliers Using Linear-Region MOS Transistors." Proc. of 1994 IEEE International Symposium on Circuits and Systems , pp. 273-276, 1994.

[7] S. C. Li. "A Very-High-Frequency CMOS Four-Quadrant Analogue Multiplier." Proc. of 1997 IEEE International Symposium on Circuits and Systems, pp. 233-236, Hong-Kong. June 9-12, 1997.

[8] M. Ismail, R. Brannen, S. Takagi, N. Fujii, N. I. Khachab, R. Khan and O. Aaserud, "Configurable CMOS Multiplier/Divider Circuits for Analog VLSI," J. of Analog Integrated Circuits and Signal Processing 5, pp. 219-234, 1994.

[9] S.-C. Huang and M. Ismail, "Design and Applications of a CMOS Analog Multiplier Cell Using the Differential Difference Amplifier," J. of Analog Integrated Circuits and Signal Processing 6, pp. 209-217, 1994.

[10] H.-J. Song and C.-K. Kim, "An MOS Four-Quadrant Analog Multiplier Using Simple Two-Input Squaring Circuits with Source Followers," IEEE J. of Solid-State Circuits, vol. 25, No. 3., pp. 841-847, June, 1990.

[11] Z. Wang, "A CMOS Four-Quadrant Analog Multiplier with Single-Ended Voltage Output and Improved Temperature Performance," IEEE J. of Solid-State Circuits , vol. 26, no. 9, pp. 1293-1301, September, 1991.

[12] C. W. Kim and S. B. Park, "Design and Implementation of a New Four-Quadrant MOS Analog Multiplier," J. of Analog Integrated Circuits and Signal Processing 2, pp. 95-103, 1992.

[13] M. Franciotta, G. Colli and R. Castello, "A 100-MHz 4-mW Four-Quadrant BiCMOS Analog Multiplier," IEEE J. of Solid-State Circuits, vol. 32, no. 10, pp. 1568-1572, October, 1997.

[14] J. Ramirez-Angulo, "HIGHLY LINEAR FOUR QUADRANT ANALOG BiCMOS MULTIPLIER FOR ±1.5V SUPPLY OPERATION," Proc. of 1993 IEEE International Symposium on Circuits and Systems, pp. 1467-1470, 1993.

[15] S.-Y. Hsiao and C.-Y. Wu, "A 1.2V CMOS Four-Quadrant Analog Multiplier," Proc. of 1997 IEEE International Symposium on Circuits and Systems, pp. 241-244, Hong-Kong, June 9-12, 1997.

[16] A. L. Coban and P. E. Allen, "Low-voltage, four-quadrant, analogue CMOS multiplier," Electronics Letters, vol. 30, no. 13, pp. 1044-1045, 23rd June, 1994.

[17] C.-H. Lin and M. Ismail, "Design and Analysis of An Ultra Low-Voltage CMOS Class-AB V-I Converter for Dynamic Range Enhancement," Proc. of 1999 IEEE International Symposium on Circuits and Systems , Orlando, Florida, June, 1999.
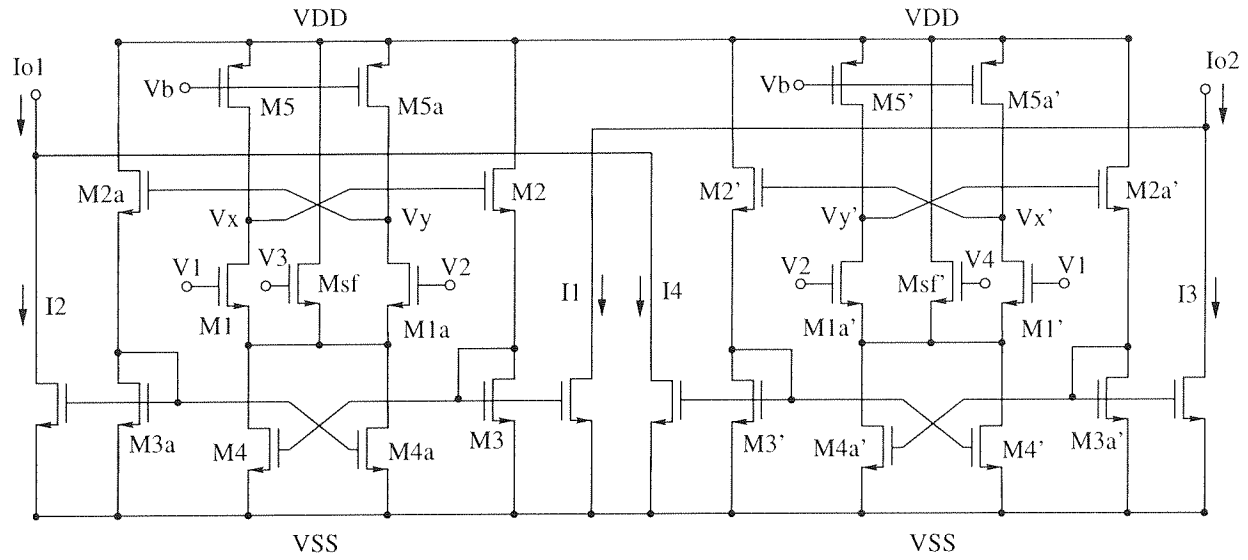
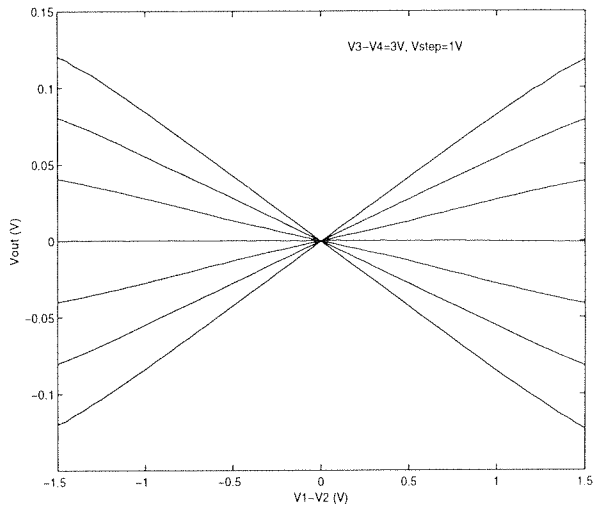Fig. 2. The proposed low-power high-speed multiplier

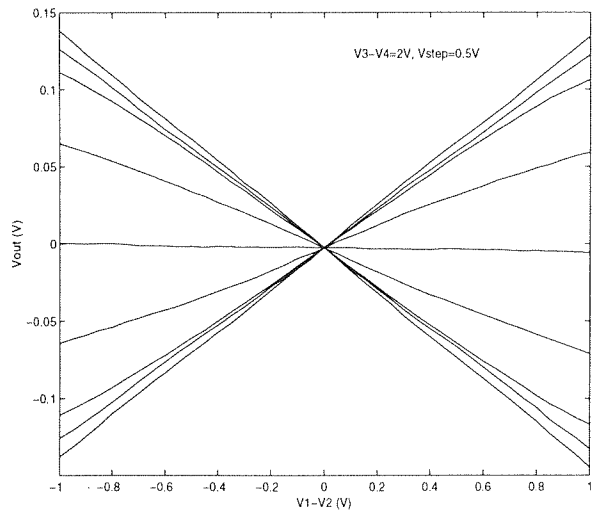Fig. 3. Measured DC characteristics of the multiplier @ 3V supply voltage

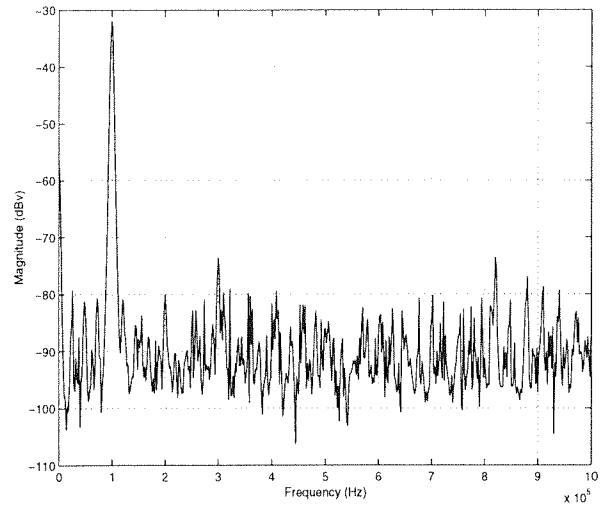Fig. 4. Measured DC characteristics of the multiplier @ 2V supply voltage

Fig. 5. Measured spectrum of the proposed multiplier