A 1.8V High Dynamic-Range CMOS High-Speed Four Quadrant Multiplier

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Abstract
A low-voltage (≤3V) CMOS four quadrant multiplier is introduced which has an almost rail-to-rail differential-input-swing with a low signal-distortion (≤1% for 100kHz signal). The proposed circuit is composed of a pair of rail-to-rail differential-input V-I converters and a pair of voltage-followers. This topology of multiplier results in a high frequency capability with low power consumption. In a 1.2μm n-well CMOS process, the 3dB frequency of the multiplier is in a range of 103MHz. Measured total power consumption is around 0.52mW with supply voltage 2V. The multiplier can operate at a minimum supply voltage of 1.8V.

1. Introduction
The analog multiplier is one of the important building blocks in VLSI communication systems, which can be applied to frequency mixers, variable gain amplifiers, adaptive filters, phase-locked loops and many other signal processing circuits. The Gilbert cell is the most popular multiplier first implemented in bipolar technology. Low-voltage, low-power analog CMOS design solutions are necessary for high performance mixed-signal ICs. Restricted by the MOSFET characteristics, CMOS multipliers usually need extra linearization circuits which may degrade the performance. Therefore, some of CMOS multipliers [1]-[9] are not very optimal for low-voltage low-power applications. Other low-voltage multipliers [10]-[16] can operate at low supply voltage. The performances are however limited to small swing range, signal distortion and high power consumption.

This paper presents a low-voltage CMOS four quadrant multiplier capable of achieving linear rail-to-rail input swing and having low-signal distortion with low power dissipation. The operation of the circuit is introduced in Section 2, second-order effects, nonlinearity and frequency performance are discussed in Section 3.

2. Circuit Description
This multiplier is composed of a pair of V-I converters and a pair of voltage follower. The V-I converter [17] is shown in Fig.1. Usually, a simple differential pair is used for voltage-current conversion, its large differential-input swing is limited by the threshold voltage of the core transistors and by the saturated drain-source voltage of current sinks or sources with lower power supply. While the amplitude of fully differential input signal increases to saturate either input transistors in a differential pair, the linear relation of $I_{out}=g_m V_I$ no longer exists because of cut off or weak inversion operation of either transistors. This results in a narrow window for large differential-input voltage in low supply voltages (≤3V). To resolve this problem, a novel voltage-to-current converter is shown in Fig.1. Considering high frequency signal processing, the core transistors, M1 and M1a, should be maintained in saturation region. Four transistors (M4, M4a, M5, M5a) are stacked with transistors M1, M1a. Assuming that M4, M4a, M5, M5a are biased in triode region, then $V_{ds}$ of M1, M1a is kept very close to $V_{DD}-V_{SS}$. For instance, with $V_{DD}-V_{SS}=3V$, by setting common-mode input voltage properly. M1, M1a can operate in saturation region with $V_{ds,M1,M1a} \geq V_{cm} \pm 1.5V_{tn}$, as differential-input voltage increases or decreases by almost 1.5V. So the linear voltage-current relation can be kept within almost ±1.5V differential input. A feedback loop M2, M3, (M2a, M3a) biases the gates of M4 to maintain triode operation of M4, M5 functions as a voltage-controlled resistor, the combination of M2, M3 is a voltage attenuator (see eq.1)

$$V_{i,M2,M2a} = \frac{KV_{2M2,M2a} - (K - 1)V_{tn}}{K + 1} \quad (1)$$

where $K = \sqrt{K_{M4}/K_{M4a}}$.

In common-mode signal processing, the triode operation of M4, M4a is established by the source voltages of M2, M2a and long channel length of the core transistors M1, M1a. So sizing the aspect ratio of M2, M3 can keep the gate voltages of M4, M4a high enough for triode operation with long channel length transistors of M1, M1a. Based on the same current flowing through triode M4 (M4a) and saturated M1 (M1a), source voltage of M1...
(M1a) are pushed close to $V_{SS}$. Therefore, the source (drain) voltages of M1, M1a (M1, M1a) can be as low as tens of millivolt. So body effect can be reduced, even ignored.

In differential-mode signal processing, the feedback loop always keeps the source voltages of M1 to follow the input signal but attenuated, so assume $V_{gs1,M1}=A(V_{cm}+V_d/2)-V_d/2$. $A$ is an attenuation coefficient of feedback loop, $A\leq 1$[17]. The drain voltages of M5, M5a are very close to $V_{DD}$ by triode-biasing of $V_d$ and $V_b$ turns $g_m$ of voltage-to-current conversion. $V_{in+},V_{in-}$ would deliver $V_1,V_2$ to generate a differential input voltage signal at the gate of M2, M2a and differential currents in their drains. By mirroring these differential currents through M3, M3a, M6, M6a and subtracting them, a linear $I_{out}=I_{ol2}$ can be obtained. So achieving almost rail-to-rail differential-input-swing is dependent on the common-mode input voltage setting and the threshold voltage.

The output current equation can be deduced as follows; of M5, M5a.

$$I_{out} = I_{M2a} - I_{M2} = \frac{K_nK'_n((1-A)^2V_{cm}-(1-A)V_{tn})(V_{ol} - 4V_{tn})}{2(K+1)^2(K_P(V_b'-V_{tp})-V_{DD} + \frac{1}{2}V_{tn})} \times V_d$$

(2)

Assume threshold voltages of all NMOS are the same as $V_{tn}$ without body effect, $K_n$, $K'_n$ are transconductance parameter of NMOS for M1, M1a and M2, M2a, and $K_P$ for M5, M5a, $V_{tn}=V_1+V_2$ is nonlinear term. The term $V_{tn}$ appearing in denominator can be combined with $V_{DD}$ as $\frac{1}{2}(2V_{DD} - V_1 - V_2)$. This term can be ignored in eq.2 because of very small second-order term of triode region equation compared with the first-order term.

$$I_{out} = I_{M2a} - I_{M2} = \frac{K_nK'_n((1-A)^2V_{cm}-(1-A)V_{tn})(V_{ol} - 4V_{tn})}{2(K+1)^2(K_P(V_b'-V_{tp})-V_{DD} + \frac{1}{2}V_{tn})} \times V_d$$

(3)

The other nonlinear term appears in numerator of eq.3, this term can be minimized by a factor of $(1+K)^2$ by sizing the ratio of M2, M3(M2a, M3a). Also as $V_1$, $V_2$ are very close to positive supply voltage, the value of $V_1+V_2$ is approximately of $2(V_{DD} - V_{SS})$. So the nonlinear effect is weak with the attenuation coefficient $(1+K)^2$. For example, at 3V supply voltage, the variation of $V_1+V_2$ is below 0.8% within 2V$_{DD}$ before dividing by $(1+K)^2$ in simulation. Later, experimental results also validate this assumption.

The proposed multiplier is shown in Fig.2. Two V-I converters are paralleled connected with a pair of voltage followers, $M_{sf}$, $M_{sp}$. The sources of the voltage followers and the sources of the core transistors, M1, M1a, M1', M1a', are connected together. Since $V_{ds,M1,M1a,M1',M1a'}$ are very close to $V_{DD}-V_{SS}$. $V_{ds,Msf,Msfp}$ can reach almost power-supply voltage. The output current can be easily derived. Assume that $K_n$, $K'_n$ are the transconductance parameters of M1, M1a, M1a', M2, M2a, M2a', Msfp, and $Msf$, the threshold voltages of all NMOS are the same as $V_{tn}$

$$V_1 - V_3 = V_{gs1} - V_{gs2} = \sqrt{\frac{2M_1}{K_n}} - \sqrt{\frac{2M_{sf}}{K'_n}}$$

(4)

So, $\sqrt{I_{M1}} = \sqrt{\frac{K_n}{2}}(V_1 - V_3) + \sqrt{\frac{K_{n,Msf}}{K'_n}}$. Squaring this equation, $I_{M1}$ can be derived as,

$$I_{M1} = \frac{K_n}{2}(V_1 - V_3)^2 + K_n\sqrt{\frac{2M_{sf}}{K'_n}}(V_1 - V_3) + \frac{K_nK_{msf}}{K'_n}$$

(5)

Similarly, $I_{M1a}$ is expressed as,

$$I_{M1a} = \frac{K_n}{2}(V_2 - V_3)^2 + K_n\sqrt{\frac{2M_{sf}}{K'_n}}(V_2 - V_3) + \frac{K_nK_{msf}}{K'_n}$$

(6)

and $I_{M1} - I_{M1a}$ is thus given by,

$$I_{M1} - I_{M1a} = \frac{K_n}{2}(V_1 - V_2 - 2V_3) + K_n\sqrt{\frac{2M_{sf}}{K'_n}}(V_1 - V_2)$$

(7)

Since from triode mode equations of M5, M5a, $I_{M1}$, $I_{M1a}$, $I_{M2a} = (K_P(V_b'-V_{tp}) - V_{DD} + \frac{V_1 + V_2}{2})(V_1 - V_2)$.

$$V_x - V_y = \frac{K_n}{2}(V_1 + V_2 - 2V_3) + K_n\sqrt{\frac{2M_{sf}}{K'_n}}(V_1 - V_2)$$

(8)

Realizing that $V_{ol} = V_{DD} - V_3$, $I_1 - I_2 = I_{M2a} - I_{M2b}$, $I_{M2a} = \frac{K_n}{2(1+K)^2}(V_{ol} - 4V_{tn})(V_x - V_y)$, $V_{ol} = V_x + V_y$ and from the equations of V-I converter, thus,

$$I_1 - I_2 = \frac{K_n}{2(1+K)^2}[K_P(V_b'-V_{tp}) - V_{DD} + \frac{V_1 + V_2}{2}] \times (V_{ol} - 4V_{tn})(V_x - V_y)$$

(9)

Similarly, $I_3$ - $I_4 = I_{M2a} - I_{M2b}$ is obtained. Then the total output current, $(I_1 + I_3) - (I_2 + I_4)$, is obtained by the subtraction of $I_{ol1}$ and $I_{ol2}$.

$$I_{out} = \frac{K_nK'_n(V_{ol} - 4V_{tn})}{2(1+K)^2}[K_P(V_b'-V_{tp}) - V_{DD} + \frac{V_1 + V_2}{2}] \times (V_1 - V_2)(V_3 - V_4)$$

(10)

As it can be observed from eq.10, the output current $I_{out}$ is a multiplication function of two differential input voltage $V_1 - V_2$ and $V_3 - V_4$. The nonlinearity of the
multiplier is determined by that of the V-I converter and the minimization of nonlinearity can be achieved accordingly.

Fig. 3, 4 show measured DC characteristics of the multiplier at a supply voltage of 3V, 2V. Measured Spectrum of the multiplier is shown in Fig. 5 with setting one input of multiplier at constant DC value. In measurement, measured THD is around 0.9% with 1V 10kHz sinusoidal input signals at 3V power supply voltages. Table I specifies the consumed static power at different supply voltages.

3. Circuit Analysis:
Second-Order Effects and High-Frequency Analysis
In practical circuit implementations, linearity error could result from mobility reduction, channel-length modulation and body effect. The former two effects depend on the process quality, the last one can be reduced by connecting sources and bulbs of transistors. Since the source voltages of M1, M1a are very close to ground node, the body effect can be reduced without source-bulk connection. Theoretically, it is assumed that all NMOS devices have no body effect, practically, source-bulk connected M2,2a, M2,2a can increase linearity. Nevertheless, a p-well fabrication technology is necessary for source-bulk connection.

The simulation result presents 3dB-frequencies at around 103MHz. The simulation shows that the output current mirrors would mainly dominate the high-frequency performance.

4. Conclusion
A 1.8V low-power CMOS high-speed multiplier has been presented. The multiplier can be used in an analog VLSI cell library for low-voltage, low-power high dynamic-range and high speed applications, such as IF variable gain amplifiers and adaptive filters.

REFERENCES
[13] M. Franciotta, G. Collin and R. Castello, “A 100-MHz 0.1-
Fig. 2. The proposed low-power high-speed multiplier

Fig. 3. Measured DC characteristics of the multiplier @ 3V supply voltage

Fig. 4. Measured DC characteristics of the multiplier @ 2V supply voltage

Fig. 5. Measured spectrum of the proposed multiplier