An all Digital BiCMOS Phase Lock Loop for VLSI Processors

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Abstract

A BiCMOS all digital phase lock loop is described. This design is suitable for applications such as clock recovery and frequency synthesis in VLSI processors where thermal stability is an important factor. The main block of the design consists of a digitally controlled oscillator with wide frequency range & high thermal stability compared to CMOS design. Improved BiCMOS adder/subtractor was also implemented to reduce worst-case propagation delay-time. A small test chip was fabricated using MOSIS Orbit 2\textmu m low-cost analog CMOS process technology that provides lateral NPN bipolar device option.

1: Introduction

Phase locked Loops are used for frequency synthesis, clock recovery, clock de-skewing and synchronization of I/O clocks in many VLSI processors. They are predominantly analog designs\textsuperscript{[1]} in integrated circuit implementation. However, with the rapid advancement in digital techniques, more PLL designs began to incorporate digital features. An all-digital PLL employing CMOS technology has been reported recently\textsuperscript{[2]}. However, BiCMOS circuit techniques are a favorable alternative in applications such as frequency synthesis & clock recovery where thermal stability is important. Also BiCMOS circuit techniques provide excellent driving capabilities. In this paper we report an All Digital BiCMOS Phase Lock Loop (ADBiPLL). In this design, essential logic blocks like adders, subtractors, registers, counters, comparators and oscillators were designed using BiCMOS circuit techniques to obtain a fast response even with a large fan-out. Auxiliary logics were designed to alleviate the involvement of the control block during specific modes of operations in order to increase the operating frequency of the ADBiPLL. A small test chip was fabricated using MOSIS Orbit 2\textmu m low-cost analog CMOS process technology that provides lateral NPN bipolar device option.

2: Architectural Implementation

The basic composition, orientation and operation modes of an ADPLL were given in [2]. Two main operations were identified: acquisition and maintenance. Both modes are further subdivided into frequency and phase acquisition or maintenance. A block diagram of the ADBiPLL is shown in Fig. 1.

In frequency acquisition, the reference clock is compared with 4X the period of the oscillator’s signal (dco\_out) using the comparator (FREQ\_CMP). The oscillator signal is generated by an unique BiCMOS digitally controlled oscillator (DCO). A precise comparison is most crucial in acquiring a highly accurate match to the ref\_clk. Comparison is done until the gain to be added/subtracted is about 0.1\% of the baseline frequency. The FGAIN register holds the gain values to be added to or subtracted from the control word in the DCONTROL register. The ADD16/SUB16 adds/subtracts the values from the multiplexers (ADDMUX/SUBMUX) to/from the control word in the DCONTROL register. The control word dictates the dco\_out’s frequency. At the end of this mode, the control block will generate a set of control signals to load the baseline frequency in the ANC register so as to initialize and enable the phase acquisition mode.

In phase acquisition mode, the ref\_clk is compared to the dco\_clk in terms of phase alignment. dco\_clk is the signal that is being fed back for phase-alignment. A phase detector (PD) is employed to generate an ahead/behind (a2/h2) signal. This signal is feed to the AUX2 logic block. The AUX2 will then generate a set of control signals to synchronize the operation of the ADD16/SUB16 and the DCONTROL register. When the phase polarity of dco\_clk relative to ref\_clk changes, the PD will generate a shift signal (s\_right) to reduce the value in the PGAIN register. The first instant when the s\_right signal is generated, phase acquisition mode is ended. A set of signals will be generated by the PD to reload the DCONTROL register.
with the baseline frequency, therefore restoring the correct frequency at the aligned phase.

Phase maintenance mode is then entered immediately and the control block is not involved during this transition, thus minimizing the delay associated with it. Besides the operations of the phase acquisition mode, this mode also has a smart shift readjustment feature to speed up the phase alignment process. Shift counters, (A1_SLEFT / B1_SLEFT) count for 8 consecutive ai/bi signals before generating a signal to shift the PGAIN register, increasing its values by one shift to the left. The purpose of this step is to increase the added/subtracted value in the register so as to reduce the no. of phase tracking cycles. For any change of phase polarity of the dco_clk relative to the ref_clk, a signal will be generated to reload the baseline frequency of the dco_clk. This mode operates continuously to track the phase alignment of the dco_clk to the ref_clk.

Frequency maintenance mode runs concurrently with the phase maintenance mode. The SLEFT counters counts for 4 consecutive events of ai/bi before generating a set of signals to add/subtract (AADD16 / ASUB16) the contents of the PGAIN register to/from the baseline control word held in the ANC register. This mode checks for frequency drift and always tracks in accordance with the ref_clk’s frequency.

3: BiCMOS Digitally Controlled Oscillator (BiDCO)

This ADBiPLL incorporates a 16-bit digitally controlled BiCMOS ring oscillator [4]. This BiDCO design provides improved frequency stability under thermal fluctuations compared to a CMOS DCO design of [2]. A 5-stage BiDCO was utilized as the heart of this chip. In [4], a 16-bit binary control vector provides a linear/quasi-linear DCO frequency range of 90-645 MHz using the 1μm BiCMOS process parameters. A tiny test chip was fabricated using the 2μm analog CMOS process technology and the fabricated BiDCO had a range of 34-200 MHz (performance degradation being mainly due to larger junction capacitances in this case). Worst case jitter due to digital control transitions at pathological control-word boundaries for the BiDCO was observed to be less than 50ps, which is lower than that for the CMOS DCO. Also the BiDCO was measured to have a thermal sensitivity of 2,000 ppm/°C compared to 4,500 ppm/°C for the CMOS DCO design.

4: Customized 16-Bit Adder (ADD16)

The bottleneck of the ADBiPLL design is the adder/subtractor. Besides the reduced logic associated with the implemented algorithm in [2], a customised BiCMOS CLA adder/subtractor with BiCMOS carry-bypass was employed. Taking the adder as an example, an enhanced BiCMOS design of [5] was implemented. The customised adder has a dynamic 16-bit BiCMOS Carry Look Ahead (CLA) as its core chain to reduce the time penalty normally associated with long CLA adders. 5 cells of BiCMOS carry-bypass were incorporated to reduce the worst case propagation delay significantly. CMOS pull-up/pull-down counterparts were utilized to pre-charge/pre-discharge instead of NPN bipolar devices as in [5]. This modification ensured a correct logic output during long clock pulses which inadvertently posses long validation periods. During this evaluation period, cells which are not switched tend to lose its accurate logic levels, causing erroneous results. With the carry-bypass implemented, this adder has a worst case propagation delay of less than 10ns for a MOSIS Orbit 2μm process technology.
The functionality of the design has been verified experimentally through a fabricated & tested prototype chip. The circuit technique is scalable and the performance would improve significantly for deep sub-micron & further miniaturized process technologies.

References


