A Multiple-Input Single-Phase Clock Flip-Flop Family

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Abstract

The design of a versatile CMOS semi-static true single-phase clock flip-flop family is presented. It naturally supports multiple, multiplexed, inputs. Asynchronous Set/Reset are easily implemented. Switching power is lower than for some other semi-static flip-flop techniques.

1 Introduction

Single phase-clock (SPC) storage devices have become very popular in recent years [3, 1, 4, 5]. Dynamic, semi-static, and fully-static designs have been presented. A variety of circuit styles including single-ended data, differential data, and pass gate data input structures have been introduced and compared [1, 5].

When a variety of logic paths have to be evaluated, ultimately some form of data selection is necessary. Quite often this selection occurs just before a register or latch structure. A popular style of state machine implementation discussed in most digital design text books makes heavy use of multiplexors just before the state FF's. Another type of alternate input to a register comes from a scan chain or built-in self-test structure.

Recent work on a processor for embedded applications led us to desire both level sensitive and edge triggered storage devices which were easy to use with multiplexed inputs and a modest clock load factor.

2 The Flip-Flop Family

For designs with pipelining or which use static registers, an edge triggered FF may be more useful than a transparent static latch. A possible approach here is to permit some dynamic operation during the (short) time that a new input is captured and output. Fully static storage is then provided.

Fig. 1 shows the two input version of a new edge triggered semi-static single-phase clock flip-flop (d2ff). From 1 to 4 inputs can be accommodated with layout area increasing gradually up to 20% for d4ff (over d1ff). Input

inverter I1 requires a low switching threshold to handle the weak pullup of N3. The static feedback inverter composed of P2, N1, and N2 must be a weak device. P2 is weak enough with about double the minimum gate length. N1 is added to weaken N2 without adding a large switching capacitance to Qz*. Alternative suggestions can be found in [2].

Note that the Q-in value is fed forward to the gate of N4 to help speed up the output transition when device P3 is trying to pull low. Also devices P4, P5 help with the output transition when P3 has trouble pulling low.

Fig. 2 shows a 2-bit shift register which can be used for comparison purposes. We use Hspice to initialize q1 to 0 and q2 to 1, then shift the bits continuously around the loop with a 4ns period. Table 1 shows some performance information for the designs being compared. Entries 1,2 both conserve power with minimum size devices. Nominal (small) device size increases were only made to make the output rise/fall times symmetrical. This is not possible for entry 3. Entry 1 appears to use less power than the other circuits, but this may be technology and application dependent.

3 Control of Multiple Input FF's

The single input version of Fig. 1 has nodes load1 and outz simply connected together. With a multiple input FF there is no longer a single clock connected to the input- and output-enable devices. In order to operate this device as a SPC ET FF, one has to guarantee that the outz signal goes off before one of the load signals goes on, and vice-versa. Fig. 3 shows a circuit which naturally accomplishes this objective.

The nand, n3, in Fig. 3 pulls down with 2 series N-devs., but pulls up with a single P-dev. Since inverters, i1,i2, pull down with a single N-dev., they can easily be designed to pull down faster than n3 pulls down. Similarly, by making the P-devs in i1,i2 weaker than the P-devs in n3, the load signals will rise slower than the outz signal falls.

An alternative control circuit for d2ff is shown in Fig. 4. In this case the outz signal is always clocked, even if there are no loads. This is simpler for the d2ff, d3ff, and d4ff versions of the FF, when it is desirable to have a load

operation on one of the inputs every clock cycle. Transistor sizing for edge control is natural for this circuit as well as the one in Fig. 3.

Clock loading in the new FF family is competitive with or lighter than in some earlier designs. Also, when a register stores multiple bits in parallel, interface circuits such as those in Figs 3,4 buffer the clock, thereby removing a high percentage of load from it.

4 Conclusion

A new family of semi-static SPC ET FF's has been introduced. The devices have versatility and layout efficiency due to their ability to support multiplexed inputs. Shift register power consumption is slightly lower than for some other reported semi-static FF's. Further power conservation is promoted by not having to drive the devices on each clock cycle. Clock to output delay and transistor count are also competitive with other FF's.

All 4 dxff's in this family have been fabricated as part of a 32-bit embedded processor in both 0.8 and 0.35 micron CMOS processes and tested up to 60MHz (the maximum speed of our tester).

References

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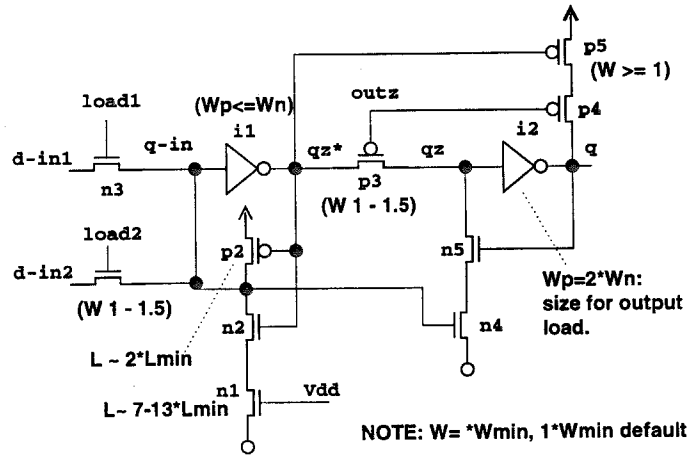
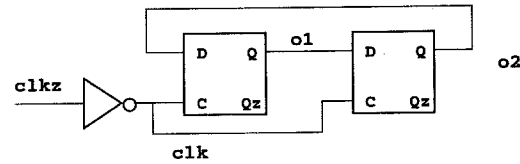Figure 1. A dual input edge triggered semi-static flip-flop (d2ff).

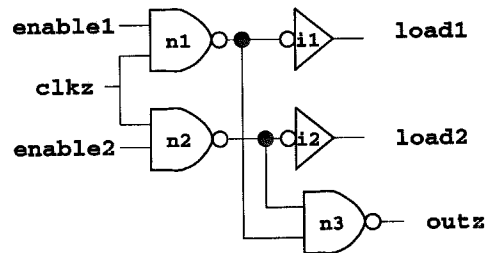Figure 2. A 2-bit shift register for various comparisons.
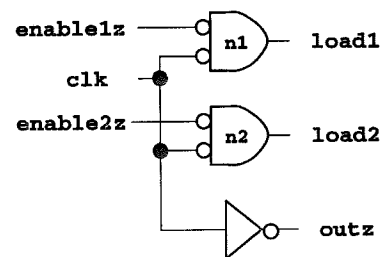

Figure 3. One possible control circuit for d2ff.

Figure 4. An alternative d2ff control circuit.