A Low Power Charge-Recycling CMOS Clock Buffer

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Abstract

A low power CMOS clock buffer based on charge recycling technique is presented. To accomplish the charge recycling process and avoid introducing the extra short circuit current during the recycling phase, an extra switching circuit and control signal are utilized to keep inverters momentarily tri-state. The feasibility of this design and its improved power efficiency are demonstrated by simulations.

1. Introduction

Design for low power is an important area in microelectronics, especially in view of the increasing demand for portable battery-powered products and the need for thermal management. Particular attention has been paid to driver circuits with large capacitive loads, as in the case of clock and bus lines, particularly due to the increasingly large clock/bus load in currently high performance VLSI CMOS chips [1]. The wherewithal for the low power design of such drivers has been scrutinized by several researchers, with proposals for either eliminating the short circuit current [2], or reducing the dynamic component by reducing the voltage swing, or by charge recycling techniques.

The most significant source of power dissipation in CMOS circuits is the charging and discharging of capacitances. Even though, the circuit might not contain intentionally-fabricated capacitances, there always are parasitic capacitances which can not be avoided and they have a significant impact on the power dissipation of the circuit. Charging and discharging a capacitance C requires an energy of CV2 (V is the supply voltage); half of this energy is dissipated when the capacitor is charged, and the other half during the discharging phase when the charges are drained to ground. One idea for low power design is to use the discharging phase of one capacitor to charge another capacitor. In other words, charge is recycled instead of being drained to ground.

In this paper, we propose and describe a charge recycling CMOS clock buffer circuit, which not only uses charge recycling between the output capacitor and the previous stage in the inverter chain, but which also eliminates the short circuit current through a momentarily tri-state output. This is achieved by an extra switching circuit and control signal, which controls the charge transfer process between the two capacitors. Section 2 of this paper explains the method to eliminate the short circuit current and discusses the principle of the charge recycling operation in tapered buffers. In section 3, we compare our charge recycling circuit with the conventional buffer and the short-circuit-current elimination approach, and we discuss the advantages of our proposed design.

2. Charge Recycling Clock Buffer

The total power dissipation of a clock buffer consists of the short circuit current power and the dynamic power components, caused by the charging and discharging of capacitances in the inverter chain. We describe here a method of eliminating the short circuit current which is a modification of the one proposed in reference [2].

Figure 1 schematically illustrates a charge recycling clock buffer. First, it reduces power dissipation due to elimination of the short circuit current in the output

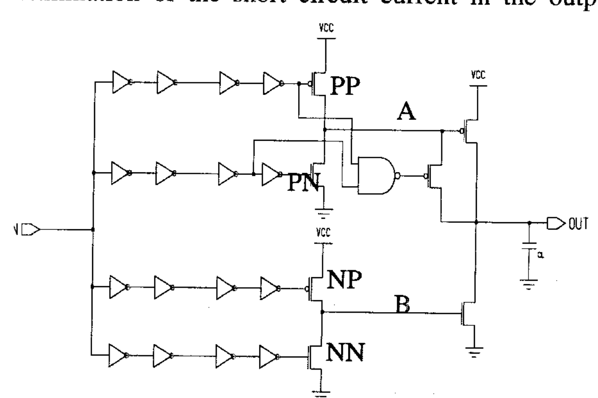

Figure 1. Charge recycling clock buffer circuit

inverter and the previous two; this is accomplished by momentarily tri-stating the output and nodes A and B just before the signals switch. This circuit consists of three stages. The fist stage is a wave-form shaper, in which very unequal pull-up or pull-down inverters are followed by a regular inverter. The second stage consists of four inverter chains (i.e., regular CMOS tapered buffers) that individually buffer the four signals from the waveform shapers, giving them enough strength to drive the output transistors. The output load capacitor determines the length of the inverter chains. The phase relation of these signals guarantees that the three PMOS's (P, PP, NP) are always turned off before the three NMOS's (N, PN, NN) are turned on, and *vice versa*.

To achieve the charge recycling, We introduced a PMOS transistor as a switch between the output and node A. We chose PMOS instead of NMOS since the transferred charge is positive, and SPICE simulations confirm the efficiency of this choice. A NAND gate is used to create the control signal for the transistor switch, which guarantees that the bridge switch is only turned on when both PP and PN are turned off (i.e., node A is tri-state). Charge will then flow from the output capacitor to node A, or from node A to the output capacitor. The NMOS transistor in the output stage is also off during the charge recycling phase.

3. Simulation and Results

In order to evaluate the performance of the charge-recycling circuit proposed in this paper, we simulated a CMOS clock buffer circuit using MOSIS 2.0-um technology with a 5 V power supply. The power dissipation was measured using the power meter design presented in reference [3]. A conventional buffer circuit and a short-circuit elimination (SCE) buffer circuit were also simulated for purposes of comparison. In addition to the power consumption, we compared the output-signal transition time and the total silicon area to evaluate the merit of our design.

Reference [2] found that the short circuit current elimination clock buffer dissipates about 10% less power as compared to the conventional CMOS buffer design. Depending upon the output load capacitance, we find power savings of up to 7% for the SCE circuit, while our design consumes about 15% less power than the conventional tapered buffer. Table 1 compares the power consumption for our charge-recycling design and the SCE design to the conventional clock buffer. Our design has a power savings of about 10% over the SCE design of Ref. [2].

The total transistor sizes for the three design are compared in Table 2. Even though our design is 10% larger in transistor size than the conventional clock buffer, it consumes less power instead. Table 3 compares the output rise and fall times for an output load capacitance of 1.5nf. Our proposed design has somewaht longer rise and fall times due to the charge recycling phase.

TABLE 1. Power Dissipation (50MHz and 5V)

	Total Power (w)				
Load Capacitor	Conven-tional	SCE	%	Our Design	%
0.6nf	1.86	1.73	6.8%	1.53	17.7%
1.0nf	2.34	2.26	3.6%	2.00	14.8%
1.5nf	2.96	2.90	2.1%	2.60	12.4%

TABLE 2. Total transistor size

Buffer	PMOS	NMOS
Conventional	195.9mm	65.7mm
SCE	205.1mm	70.0mm
Our Design	219.0mm	68.0mm

TABLE 3. Transition times

	Rise	Fall
Conventional	2.60ns	1.87ns
SCE	2.67ns	1.89ns
Our Design	3.33ns	2.07ns

4. Conclusion

We have proposed a design for a CMOS clock buffer circuit based on a charge recycling technique. In addition, our proposed design also avoids extra short circuit current. SPICE simulation results show that our design consumes about 15% less power than a conventional clock buffer, but with some performance sacrifice in the switching speed.

5. References

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