Current Sensor on the Base of Permanent Pre-chargeable Amplifier

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Abstract

The sensitivity and delay of the amplifier the key problems in the performance of Current Sensors(CS). For large devices which consist of several cells, for example 32bit, the amplifier must react to 10-20mV. The previous type of highly sensitive amplifier which is based on cascade and reference voltage[dill] can react to this level of voltage. But this model is not stable in respect to technological and parametric variation. In this paper, we suggest a tripple cascade inverters feedbacked by a un-symmetrical pass transistor which amplifies 1mV without reference voltage. Monte-Calro SPICE simulation shows the stableness of this model for parametric variation. We prepare the schematic of CS which includes control unit with shunt transistors and evaluate the delay.

1 Introduction

Current Sensor(CS) is a module of current detector that probes a node of a CMOS circuit. As a character of CMOS logic circuit, current flows through both sources only when its output logically changes. So by probing source nodes, CS detects the change of output value of a CMOS logic circuit. To use this trait, CS is used not only to verify CMOS circuits[1], but also to detect the transient process completion(TPC)[3].

The advantage of CS for handshaking is that a synchronous device can be directly used for asynchronous implementation. To produce the signal of TPC, we don't have to change the logic circuit itself, but only attach a CS at both its source nodes. So, the library of inherent synchronous proto-types can be shared for asynchronous design.

There is a drawback of using CS for TPC, which is the occupied area. CS consists of current sensing part and logical control part(fig.1.a). If the area of CMOS circuit is not so large, the use of CS cannot be reasonable. A large CMOS circuit consisting of several cells is preferable to use CS.

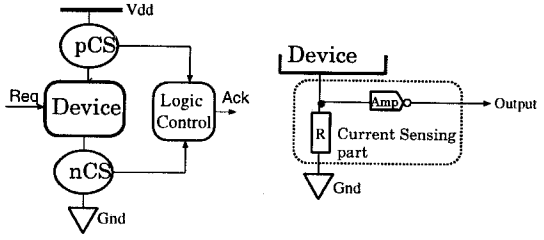

Figure 1. Current Sensor.

But when the number of cells increases, the variation of current to detect also increases. The current sensing part consists of a resistance and voltage amplifier. The resistance is scaled so that the voltage drop at the resistance node does not exceed 500mV-800mV for flowing maximum current, otherwise, this voltage drop affects the performance of CMOS circuit. This means that the voltage drop at the flowing minimum current is determined by the variation of current. If the variation is $1 \div 20$, the minimum voltage dropped by the flowing current is 25mV-40mV, which the amplifier must response. To apply the CS for CMOS circuit consisting of a large number of cells, a highly sensitive amplifier is needed. The result we consider the best were obtained in [4]. This model used a cascade amplifier with reference voltage. But cascade amplifier with reference voltage is not stable in respect to physical and technological parametric variation. a more stable and more sensitive amplifier is crucial for the performance of CS.

2 Amplifier

Fig2 shows a basic CMOS amplifier which is based on CMOS inverter's I-O characteristic. For appropriate performance, a very high resistance is needed (Mega ohm level).

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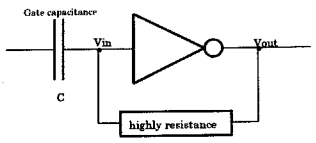

Figure 2. Basic CMOS amplifier.

There is a difficulty to fabricate such a resistance element. Some papers suggest the use of a pass transistor as a substitution of the resistance element. But pass transistor needs a periodic pulse to re-charge the input capacitance, otherwise the input capacitance is discharged by the leak current from the body of the pass transistor(fig.3).

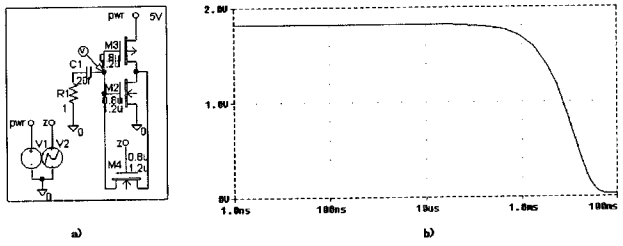

Figure 3. Discharged by leak current.

So, we suggest to use un-symmetric pass transistors, whose gate node is connected to its drain node. The voltage of capacitance is permanently pre-charged by leak current from the body and current from drain to source of the pass transistor. Under the condition of rising (falling) type of input pulse, the gate-source voltage of n-MOS(p-MOS) is lower than the threshold voltage, so this element works at high resistance. Fig.4 shows the circuit of permanent pre-

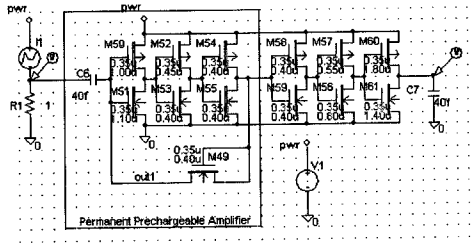

Figure 4. Permanent Pre-chargeable amplifier.

chargeable amplifier with n-type pass transistor. For appropriate amplification, we introduce triple cascade inverters which have a feedbacke connection by the pass transistor.

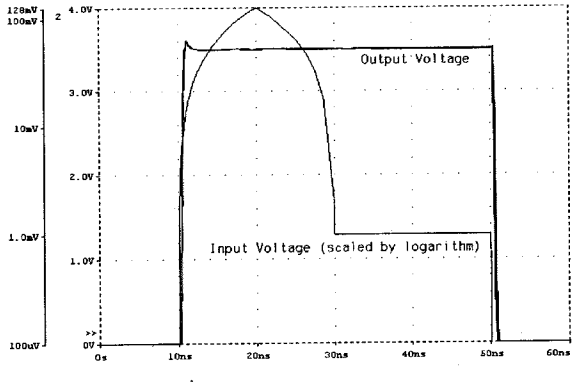

Figure 5. Wave form of Monte-Carlo simulation.

This model can amplify the variation of $1mV \div 200mV$ input voltage. We must note that this structure is stable in respect to parametric variation because each node is naturally charged at the balanced voltage, without reference voltage. Fig.5 shows the Monte-Carlo SPICE simulation(BSIM3V3) with 5% parametric dispersion for 100 times for MOSIS $0.35\mu m$ technology. The delay of amplification is less than 0.5ns.

3 Control unit with Current Shunt

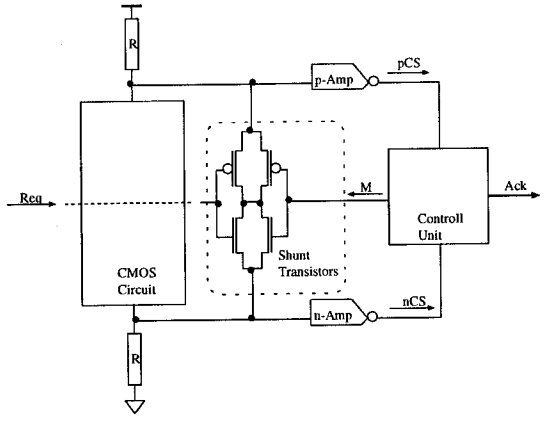

Figure 6. Control unit with Current Shunt

There are problems to produce the acknowledge signal with the amplifier. For handshaking, the acknowledge signal must keep the same value until the request signal changes, but the amplifier's output is pulse form and its period depends on the input data. Second, if the output value is the same though a new input data has come or if the period

of the transient process completion is much smaller than the amplifier's delay, the amplifier cannot produce the signal. So, Control Unit with Current Shunt is suggested in [5]. Fig6 shows its diagram. The shunt transistor is controlled by the request signal, Req and signal from the control unit, M. When Req changes, the shunt transistor opens to produce a current from the sources compelling amplifier to work. After the amplifier produces the signal, the control unit produces M to cease the shunting current.

The change diagram of this control unit is shown in fig7. Note that signal m1, m2, a1 are internal signal. From this change diagram, the following equations can be produced:

$m1 = \overline{nCS * Ack + m2 * (pCs + Ack)};$
$m2 = \overline{nCS * m1 + M * (pCS + m1)}; \quad M = \overline{m2};$
$a1 = \overline{m1 * pCs + Ack * (M + nCS)};$
$Ack = \overline{pCS * a1 + Req(nCS + a1)};$

If $\tau_{amp} + 2\tau_{CSh} + 2\tau_{gate} + \tau_{inv} \leq \tau_{dev}$, the delay in this circuit does not affect the performance[5]. The circuit of the current sensor is shown in Fig8. As a substitution of CMOS device, we use an inverter with load capacitance whose input gate is connected to the request signal. By the change of the capacitance parameter, the delay of the CMOS device can be controlled. In this simulation, MOSIS $0.35\mu m$ is used. Fig9 shows the delay from rising Req up to reacting M, is 1.4ns, which corresponds to $\tau_{amp} + 2\tau_{CSh} + 2\tau_{gate} + \tau_{inv}$.

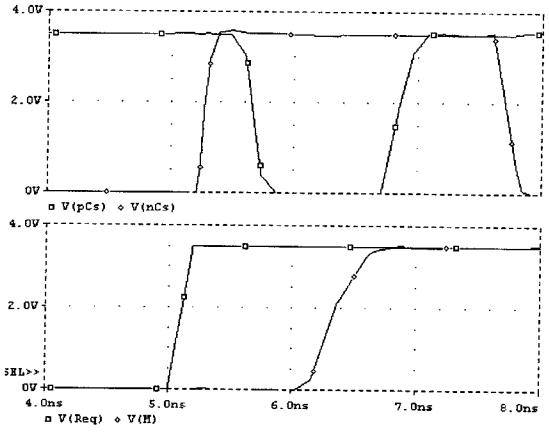

Figure 9. Wave form of control unit signals

4 Conclusion

A triple cascade of inverters with feedback connection provides stable and radically higher sensitivity. For the sake of high sensitivity, the capacitance for input node can be minimized, down to 0.04pF. Using such amplifiers would essentially improve such parameters as current multiplicity and performance. There are tasks besides that. First, creating 2Ω resistance requires significant area and poses additional questions. Second, continual use of amplifier and precharged voltage might slightly shift because of subthreshold current from the output node, and the high sensitivity is spoiled. Of course, this shift will cease when the voltage difference between the source and drain pass transistor approaching the threshold voltage. It is acceptable for current variation $1 \div 128$. But in the future, a wider variation is needed, we must coupe with this problem.

References

[1] Felthan D.B., Nigh P., Maly W., *Current Sensing for Built-in Testing of CMOS Circuits*, Proceedings of International Conference on Computer Design, 1988, pp. 454–457.

[2] Maly W., Nigh P., *Built-In Current Testing Feasibility Study*, In Proceeding of the International Conference on Computer-Aided Design, CA,November 1988, pp. 340-343.

[3] Izosimov O.A., Shagurin I.I., Tsylyov V.V., *Physical Approach to CMOS Module Self-Timing*, Electronics Letters, Vol. 26, No 22, 1990, pp. 1835–1836.

[4] Dean M.E., Dill D.L., Horowiz M., *Self-Timed Logic Using Current-Sensing Completion Detection (CSCD)*, Proceedings of International Conference on Computer Design, 1991, pp. 187–191.

[5] Varshavsky V., Marakhovsky V., Lashevsky R., *Asynchronous Interaction in Massively Parallel Computing Systems*, Proceedings of the IEEE First ICA^{3}PP, Vol. 2,April 1995, pp. 481–492.

[6] Varshavsky V., Marakhovsky V., Lashevsky R., *Critical View on the Current Sensor Application for Self-Timing in VLSI Systems*, Proceedings of the ASP-DAC'95/CHDL'95/VLSI'95, 1995, pp. 342–750.

[7] N.H.E.Weste, K.Eshraghian, Principles of CMOS VLSI Design, Addison-Wesley, Second Edition, 1993.

[8] Varshavsky V., *Does Current Sensor Make Sense?*, 7th International Symposium on IC Technology, Systems & Applications (ISIC-97), Sigapore, Sept. 1997, pp.471-473.

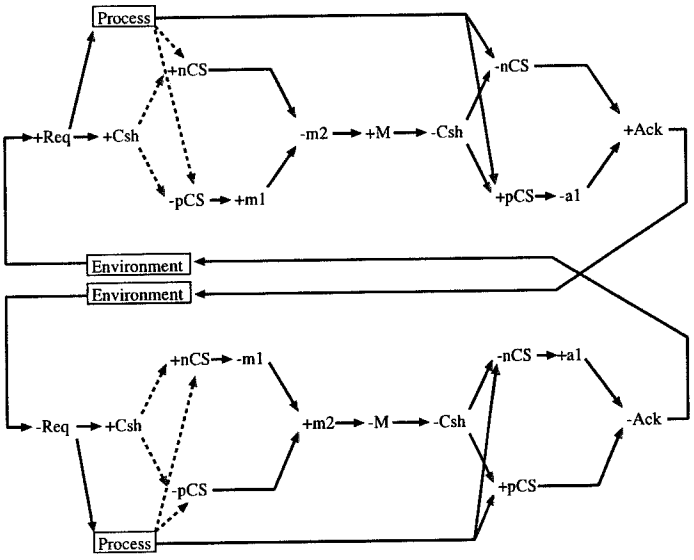

Figure 7. Change diagram of Control unit signals

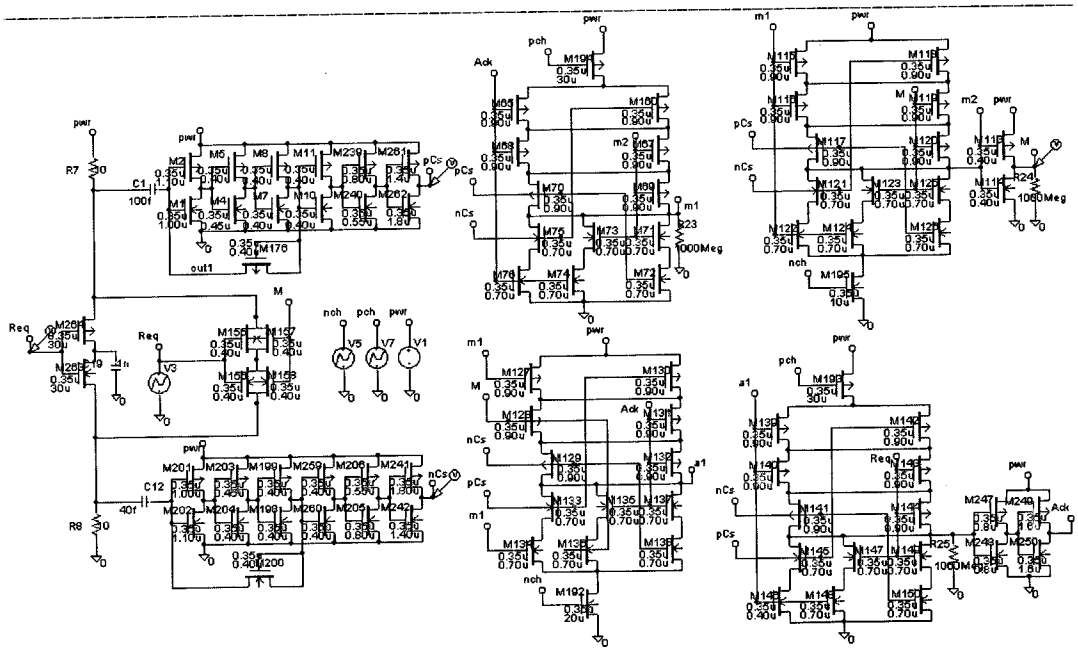

Figure 8. CMOS implementaiton of Control unit