LINEAR TRANSCONDUCTORS USING LOW VOLTAGE LOW POWER SQUARE-LAW CMOS CELLS

Tuna B. Tarım[1] *and Mohammed Ismail*[2]

[1] Ph.D. student in Department of Electronics Engineering, Istanbul Technical University, Istanbul, Turkey, and currently on leave at The Ohio State University, Columbus, Ohio, USA
Phone: (614) 688 4329, Fax: (614) 292 7596, e-mail: tarim@ee.eng.ohio-state.edu
[2] Department of Electrical Engineering , The Ohio State University, Columbus, OH 43210, USA
Phone: (614) 292 0351, Fax: (614) 292 7596, e-mail: ismail@ee.eng.ohio-state.edu

Abstract: Two transconductors composed of two square-law CMOS cells are introduced in this paper. The analysis of the cells is given. The transconductors operate in the saturation region with a fully balanced input signal. Simulations were done for 0.8μm n-well process using BSIM3 model parameters. The first circuit has a trade-off between low voltage operation and low power dissipation. The circuit has a cutoff frequency of 170MHz and P_{dis}=1.17mW for a bias current of 120μA. The second transconductor has aimed to overcome the trade-off and to improve the performance; the circuit has a cutoff frequency of 236MHz and P_{dis}=1.74mW for the same bias current, however, it is possible to reduce the bias current, since the trade-off The transconductors have a THD of less then -56dB and -60dB, respectively, for 1MHz, 0.5V peak-to-peak sinusoidal input. A comparison between the two circuit performances is given.

1. Introduction

The need for robust low voltage low power CMOS analog VLSI circuits is tremendously growing. The major driving force for this growth is the need for one-chip solution for systems with combined analog and digital circuitry. Many applications which require reduced supply voltage and low power consumption are based on analog/digital mixed mode signal processing VLSIs, such as low voltage low power transconductors.

An elegant way to achieve a linear transconductor, starting with transistors in strong inversion and having a square-law behavior, is to use the difference of squares principle [1]. This principle states that given the variables A and B, the difference of the squares $(A+B)^2$ and $(A-B)^2$ is linear in A or B, that is

$$(A+B)^2-(A-B)^2=4AB \qquad (1)$$

This principle can be used to obtain a linear relationship between the difference in the gate-source voltages of two transistors and the difference in their output currents. The realizations given in [2-5] are based on using MOS transistors operating in the saturation region.

A certain class of analog/digital mixed mode signal processing VLSI circuits are basicly composed of several cells which have a square-law characteristic. Recently, several new low voltage low power CMOS square-law composite cells with two high impedance input terminals were proposed [6, 7] to achieve accurate signal processing with low power dissipation. Understanding the basic principles of the low voltage low power cells will lead to a better understanding of the circuits built with these cells.

Two new transconductors using the above mentioned principle are introduced in this paper. The operation of the linear transconductors and the CMOS square-law cells that are used to build the circuits are described in Section 2. Section 3 provides initial results of the circuits. Section 4 concludes the work.

2. Description of the Circuits

The low input impedance at the source limits the applicability of a single MOS transistor. A solution would be to use the CMOS composite cell [2], given in Figure 1(a). However, it is not suitable for low voltage designs due to its high equivalent threshold voltage, $V_{Teq}=\mid V_{Tp}\mid +V_{Tn}$. Also, the necessity of the twin-well process to eliminate the body effect is a drawback from the process point of view, because it is not a standard CMOS process.

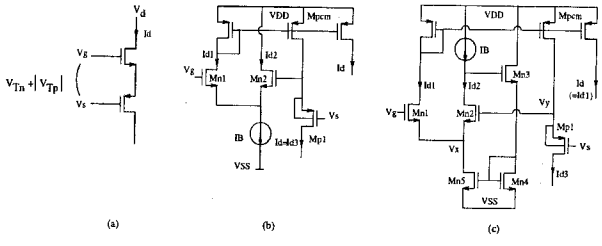


Fig. 1. a) Conventional composite transistor, b) Low voltage composite cell, c) Low power composite cell

The low voltage cell given in Figure 1(b) [6] has been presented in order to overcome the drawbacks of the composite transistor. The cell requires only an n-well process. Transistors M_{n1} and M_{p1} are the basic CMOS pair transistors. M_{n2} and I_B form a level shifter circuit to decrease the value of the threshold voltage. M_{pcm}

0-7695-0104-4/99 $10.00 © 1999 IEEE

is the group of PMOS transistors forming the current mirror to ensure that the currents flowing through transistors M_{n1} and M_{p1} are equal. by taking the current through M_{n1} and pushing it through M_{p1}.
The drain currents I_{d1} through I_{d3} shown in Figure 1(b) are expressed as

$$I_{d1} = \frac{K_{n1}}{2}(V_g - V_x - V_{Tn})^2 \quad (2)$$

$$I_{d2} = \frac{K_{n2}}{2}(V_y - V_x - V_{Tn})^2 \quad (3)$$

$$I_{d3} = \frac{K_{p1}}{2}(V_y - V_s - \mid V_{Tp} \mid)^2 \quad (4)$$

Using the fact that $I_{d1} = I_{d3}$ and $I_{d1} + I_{d2} = I_B$, equations (2) through (4) can be rewritten in the form of

$$V_g - V_x = \sqrt{\frac{2I_d}{K_{n1}}} + V_{Tn} \quad (5)$$

$$V_y - V_x = \sqrt{\frac{2(I_B - I_d)}{K_{n2}}} + V_{Tn} \quad (6)$$

$$V_y - V_s = \sqrt{\frac{2I_d}{K_{p1}}} + \mid V_{Tp} \mid \quad (7)$$

The drain current equation for the low voltage CMOS square-law composite cell can be written as

$$I_d = \frac{K_{eq}}{2}(V_{gs} - V_{Teq})^2 \quad (8)$$

where K_{eq} and V_{Teq} are the equivalent transconductance parameter and the equivalent threshold voltage, respectively, expressed as

$$K_{eq} = \left(\frac{1}{\sqrt{K_{n1}}} + \frac{1}{\sqrt{K_{p1}}}\right)^{-2} \quad (9)$$

$$V_{Teq} = \mid V_{Tp} \mid - \sqrt{\frac{2(I_B - I_d)}{K_{n2}}} \quad (10)$$

It is clear that the threshold voltage is the function of the drain current, I_d. Hence, the threshold voltage is varying with the input voltage causing distortion. In the case where $I_B \gg I_d$, the threshold voltage equation can be simplified as

$$V_{Teq} = \mid V_{Tp} \mid - \sqrt{\frac{2I_B}{K_{n2}}} \quad (11)$$

which is now a constant value and much less than the equivalent threshold voltage of the conventional composite transistor. Thus, the cell is suitable for low voltage applications. However, I_B is set to a much larger value than I_d to minimize the dependence of V_{Teq} on the drain current I_d. This causes high power dissipation at quiescent conditions. Thus, the cell has a trade-off n-well between low voltage operation and low power dissipation. Note, however, that the circuit no longer needs a twin-well process.
The low voltage low power CMOS square-law composite cell [7] illustrated in Figure 1(c) has been designed to overcome the trade-off of the low voltage cell.
Transistors M_{n1} and M_{p1} are the basic CMOS pair transistors. The feedback loop formed by transistors M_{n2}, M_{n3}, M_{n4} and M_{n5}, and the bias current I_B always keeps the drain current of transistor M_{n2} equal to I_B. This makes the voltage drop V_{g2} (or $V_{gs2} - V_{Tn}$) of transistor M_{n2} constant.
The drain currents I_{d1} through I_{d3} shown in Figure 1(c) are expressed as

$$I_{d1} = \frac{K_{n1}}{2}(V_g - V_x - V_{Tn})^2 \quad (12)$$

$$I_{d2} = \frac{K_{n2}}{2}(V_y - V_x - V_{Tn})^2 \quad (13)$$

$$I_{d3} = \frac{K_{p1}}{2}(V_y - V_s - \mid V_{Tp} \mid)^2 \quad (14)$$

Since $I_{d1} = I_{d3} = I_d$ and $I_{d2} = I_B$, the above equations can be rewritten as

$$V_g - V_x = \sqrt{\frac{2I_d}{K_{n1}}} + V_{Tn} \quad (15)$$

$$V_y - V_x = \sqrt{\frac{2I_B}{K_{n2}}} + V_{Tn} \quad (16)$$

$$V_y - V_s = \sqrt{\frac{2I_d}{K_{p1}}} + \mid V_{Tp} \mid \quad (17)$$

Substituting equations (15) and (17) in equation (16) will yield the drain current equation given in equation (8) where V_{Teq} is expressed as

$$V_{Teq} = \mid V_{Tp} \mid - \sqrt{\frac{2I_B}{K_{n2}}} \quad (18)$$

Equation (18) shows that the circuit no longer has to satisfy $I_B \gg I_d$, as I_d can be increased regardless of I_B. The trade-off between low voltage operation and low power dissipation for the previous cell has been overcome in this circuit.
The transconductors introduced in this paper are built with the parallel connection of two of these cells. The low voltage transconductor and the low power transconductor will have the same drawbacks and/or achievements of their source cells. Hence, the trade-off between

low voltage operation and low power dissipation will remain for the transconductor built with the low voltage cell, as well as the transconductor built with the low power cell overcomes this drawback.
The transconductors are described next.

2.1 The Linear Transconductors

The transconductor using the low voltage cell is illustrated in Figure 2.

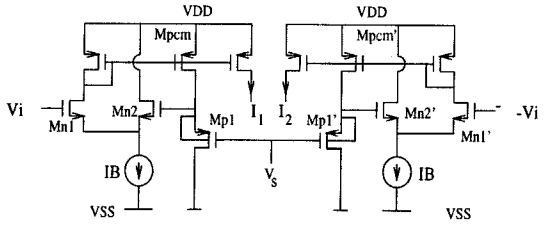


Fig. 2. Transconductor using the low voltage CMOS square-law composite cell

The circuit operates in the saturation region with a fully balanced input signal. It is preferable that analog circuits operate in the fully balanced mode, mainly because fully balanced circuits ensure high power supply rejection, improve linearity and increase dynamic range. The input voltages and the control voltage are applied to the NMOS and PMOS pair, respectively. The output differential current equation is derived by using the difference of squares principle:

$$\begin{aligned} I_1 - I_2 &= K_{eq}(V_{gs1} - V_{Teq})^2 - K_{eq}(V_{gs2} - V_{Teq})^2 \\ I_1 - I_2 &= K_{eq}(V_i + V_{CM} - V_s - V_{Teq})^2 \\ &- K_{eq}(V_i - V_{CM} - V_s - V_{Teq})^2 \\ I_1 - I_2 &= 4K_{eq}(V_{CM} - V_s - V_{Teq})V_i \end{aligned} \quad (19)$$

Hence, the transconductance is given by

$$G_m = 4K_{eq}(V_{CM} - V_s - V_{Teq}) \quad (20)$$

where K_{eq} and V_{Teq} are the equivalent transconductance parameter and the equivalent threshold voltage, respectively, V_{CM} is the common mode voltage and V_s is the control voltage. Note that, having the control voltage V_s in equation (20) allows the transconductance of the circuit to be electronically tuned.
As mentioned above, the circuit has a trade-off between low voltage operation and low power dissipation, as in the original cell. The transconductor described next overcomes this drawback.
Figure 3 shows the transconductor built with the low power square-law cell.

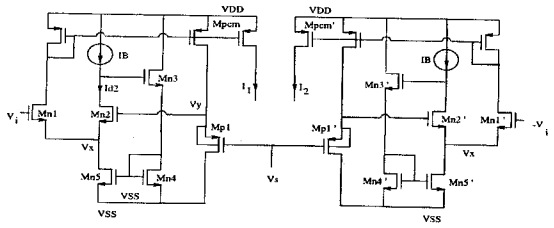


Fig. 3. Transconductor using the low voltage low power CMOS square-law composite cell

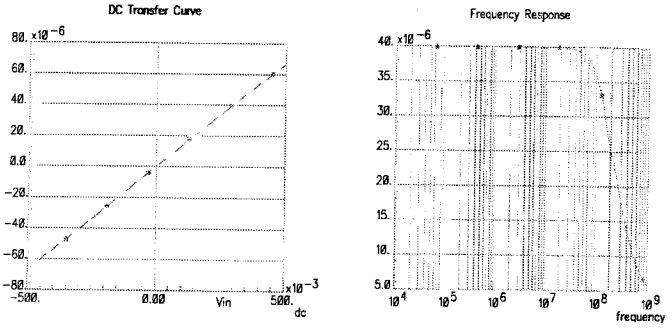
The circuit operates in the saturation region with a fully balanced input signal. The transconductance of the circuit is derived by taking the difference of the output currents of each cell, as given for the previous transconductor. The transconductance is given by

$$G_m = 4K_{eq}(V_{CM} - V_s - V_{Teq}) \quad (21)$$

which is similar to equation (20). However, the threshold voltage equation written as $V_{Teq} = \mid V_{Tp} \mid -\sqrt{2I_B/K_{n2}}$ no longer includes the drain current, hence, the drawback of the previous transconductor no longer exists.

3. Results

Both circuits have been simulated using 0.8μm n-well process BSIM3 model parameters. The DC transfer curve and the frequency response of the transconductor using the low voltage cell is given in Figure 4(a) and Figure 4(b).

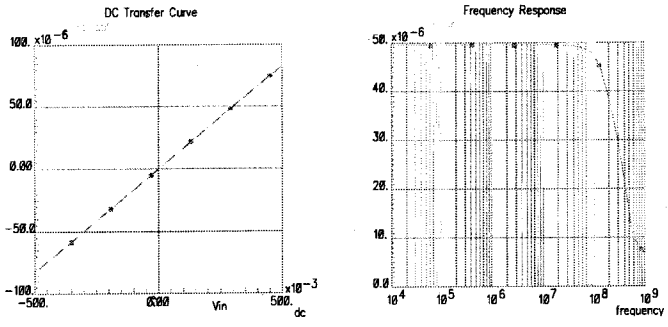


(a) (b)

Fig. 4. a) DC transfer curve, b) Frequency response of the transconductor using the low voltage CMOS square-law composite cell

For a bias current of 120μA, the cutoff frequency is 170MHz with a power dissipation of P_{dis}=1.17mW. The transconductance value is $g_m = 133.38\mu A/V$. The circuit has a THD of less than -56dB for 1MHz, 0.5V peak-to-peak sinusoidal input, without considering statistical process variations.

The results of the transconductor using the low power cell is shown in Figure 5.



(a) (b)

Fig. 5. a) DC transfer curve, b) Frequency response of the transconductor using the low power CMOS square-law composite cell

For a bias current of 120μA, the cutoff frequency is 236MHz with a power dissipation of P_{dis}=1.740mW, however, it is possible to reduce the bias current, thus, to reduce the power dissipation. The transconductance value is $g_m = 165.16\mu A/V$ and the THD is less than -60dB for 1MHz, 0.5V peak-to-peak sinusoidal input. Figure 6 shows the power dissipation versus frequency response for the two transconductors. As mentioned above, the low power transconductor can accomplish a higher bandwidth, yet have a less power dissipation since it is possible to reduce the bias current. It can also be seen from Figure 6 that for the frequency range of up to 180MHz, it will be advantageos to use the low voltage low power transconductor, however, for higher frequencies both circuits do not differ too much in terms of power dissipation. The comparison of the THD of both circuits result as expected. The first transconductor uses the approximation of $I_B \gg I_d$; this will effect the THD of the circuit and make it higher, while this approximation no longer exists for the low power transconductor.

4. Conclusion

Two transconductors composed of two square-law cells have been introduced in this paper. The transconductors operate in the saturation region with a fully balanced input signal. The first circuit has a trade-off between low voltage operation and low power dissipation, with a cutoff frequency of 127MHz and P_{dis}=1.17mW for a bias current of 120μA. The second transconductor overcomes this trade-off and improves the performance; the circuit has a cutoff frequency of 236MHz and P_{dis}=1.740mW, for a bias current of 120μA. It is also possible to reduce the bias current, since the trade-off between low voltage operation and low power dissipation no longer exists. The low voltage and low power circuits have a THD of -56dB and -60dB, respectively, for 1MHz, 0.5V peak-to-peak sinusoidal input. A comparison between the two circuit performances is given.

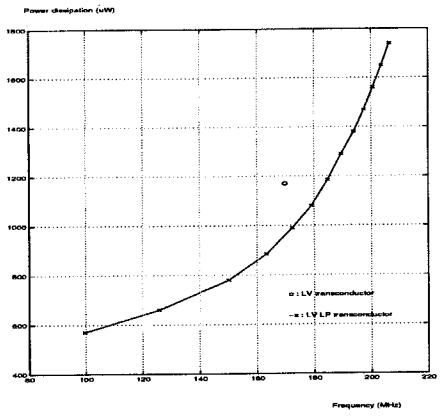


Fig. 6. Power dissipation versus frequency response for both transconductors

5. Acknowledgment

Financial support from TÜBITAK (The Scientific and Technical Research Council of Turkey) and from Texas Instruments, Inc. are gratefully acknowledged.

6. References

[1] R.F. Wassenaar, Analysis of Analog CMOS Circuits, Oxford University Press, 1996

[2] E. Seevinck and R.F. Wassenaar, "A versatile CMOS linear transconductor/square-law function circuit", IEEE Journal of Solid-State Circuits, Vol.SC-22, pp. 366-377, June 1987

[3] A. Nedungadi and T.R. Viswanathan, "Design of linear CMOS transconductance elements", IEEE Transactions on Circuits and Systems, Vol.CAS-31, No. 10, pp. 891-894, October 1984

[4] J.S. Martinez, M.J. Steyaert and W.M.C. Sansen, "A large-signal very low-distortion transconductor for high-frequency continuous-time filters", IEEE Journal of Solid-State Circuits, Vol.26, No. 7, pp. 946-955, 1991

[5] F. Krummenacher and N. Joehl, "A 4MHz CMOS continuous-time filter with on-chip automatic tuning", IEEE Journal of Solid-State Circuits, Vol.SC-23, pp. 750-758, 1988

[6] A. Motamed, Low-Voltage Analog VLSI Circuits and Signal Processing, Ph.D. Dissertation, The Ohio State University, Columbus, 1996

[7] A. Hyogo, C. Hwang, M. Ismail and K. Sekine, "LV/LP CMOS square-law composite transistors for analog VLSI applications", IEEJ 1'st International Analog VLSI Workshop, ECT-97-59, pp. 139-143, USA, May 1997